MB90V520/F523/F523A/523/523A
(Different part about specification notes.)

MB90V520 is same as document at Hardware Manual.

Modified specification for MB90F523.

1. Corrective of LCD SEG/COM output current leak at stop mode.
   SEPCIFICATION:
   Explanation of LCD controller driver part.

(1)About LCDCMR register

Address	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit09	Bit08
00000Bh	-	-	-	-	COM3	COM2	COM1	COM0

COM3-0:
0:P73-P70 Port function.
But When COM0=1 P70-P73 can not input form terminal.
(When COM0 bit value =1, can not use input port)
1:COM3-0 function.

(2)About LCR1 register (LCDC control register)

Address	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit09	Bit08
00000Bh	Resv	SEG5	SEG4	Resv	SEG3	SEG2	SEG1	SEG0

SEG5:PA7/SEG15-PA3/SEG12 select bit.
0:PA7-PA0 Port function.
1:SEG15-SEG12 SEGMENT output mode.
Caution : When This bit setup "1" and SEG4 bit setup "0",
PA3-PA0 can not use input port.

SEG4:PA7/SEG15-PA3/SEG12 select bit.
0:PA3-PA0 Port function.
1:SEG11-SEG08 SEGMENT output mode.
Caution : When This bit setup "1" and SEG5 bit setup "0",
PA7-PA4 can not use input port.

SEG3:P97/SEG31-P93/SEG28 select bit.
0:P97-P94 Port function.
1:SEG31-SEG28 SEGMENT output mode.
Caution : When This bit setup "1" and SEG2 bit setup "0",
P93-P90 can not use input port.

SEG2:P93/SEG27-P90/SEG24 select bit.
0:P93-P90 Port function.
1:SEG27-SEG24 SEGMENT output mode.
Caution : When This bit setup "1" and SEG3 bit setup "0",
P97-P94 can not use input port.

SEG1:P87/SEG23-P83/SEG20 select bit.
0:P87-P84 Port function.
1:SEG23-SEG20 SEGMENT output mode.
Caution : When This bit setup "1" and SEG0 bit setup "0",
P83-P80 can not use input port.

SEG0:P83/SEG19-P80/SEG16 select bit.
0:P83-P80 Port function.
1:SEG19-SEG16 SEGMENT output mode.
Caution : When This bit setup "1" and SEG1 bit setup "0",
P87-P84 can not use input port.

Hardware Manual of MB90520 series is preliminary version 1.2.

Correction information as follows:

Revised Hardware Manual of MB90520 series

- Chapter 21 : LCD Controller/Driver.
  Fig.21.7 Rectified internal sprit resistor. (Page 21-13)
    Between Vcc and V3: Logic of 2R resistor with switch ==> nothing
    (The logic of 2R resistor with switch between Vcc and V3 was deleted.)

- Chapter 21 : LCD Controller/Driver.
  21.3.3 LCD/COM pin switch register (LCDCMR)
    No information ==>> It is the information as follows.

    - General/COM port selecting register.

	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
Address:00000Bh	---	---	---	---	COM3	COM2	COM1	COM0	LCDCMR
Read / Write:	(-)	(-)	(-)	(-)	(R/W)	(R/W)	(R/W)	(R/W)	
Initial Value:	(-)	(-)	(-)	(-)	(0)	(0)	(0)	(0)	

      COM3 to COM0
       0 : The port operate a general port.
       1 : The port operate a COM port.

- Table A-1 I/O Map (Page App-6)
    Address 8ch Port-0 resistance register PDR0
  ==>Address 8ch Port-0 resistance register RDR0
    Address 8dh Port-1 resistance register PDR1
  ==>Address 8dh Port-1 resistance register RDR1
    Address 8eh Port-4 resistance register PDR4
  ==>Address 8eh Port-4 resistance register RDR4

- Table A-1 I/O Map (Page App-6)
    Address 100h to #h ROM area
  ==>Address 100h to #h RAM area

- Capter5.1 (Page 5-3)(Page 5-7)
    Watch timer control register:Bit0 WWC0
  ==>Watch timer control register:Bit0 WTC0

- 21.1.1 PORT/COM Pin Switch Register (Page 21-4)
    PORT/COM Pin Switch Register
  ==>PORT/COM Pin Switch Register (LCDCMR)

- 18.1 Register List (Page 18-4)
  Timer data register 1 and 2 ==> Timer count data register 1 and 2
  Control status register 1 and 2 ==> Timer count control status register 1 and 2
  OCCP0 to OCCP7 ==> OCP0 to OCP7
  Compare register ==> Output compare register 0 to 7
  Control status register ==> Output compare control status register
  Capture register ==> Input capture data register 0 and 1
  Control status register ==> Input capture control status register 0 & 1

- 18.2 Block Diagram (Page 18-5)
  16-bit timer1 ==> 16-bit free-run timer 1 [Timer count data register(TCDS1)]
  16-bit timer2 ==> 16-bit free-run timer 2 [Timer count data register(TCDS2)]
  Compare register 0 ==> Output compare register 0
  Compare register 1 ==> Output compare register 1
  Compare register 2 ==> Output compare register 2
  Compare register 3 ==> Output compare register 3
  Compare register 4 ==> Output compare register 4
  Compare register 5 ==> Output compare register 5
  Compare register 6 ==> Output compare register 6
  Compare register 7 ==> Output compare register 7
  Capture register 0 ==> Input capture data register 0
  Capture register 1 ==> Input capture data register 1

- 18.3.1 Register List (Page 18-6)
     Timer data register 1 and 2
  ==>Timer count data register 1 and 2
     Control status register 1 and 2
  ==>Timer count control status register 1 and 2

- 18.3.2 Block Diagram (Page 18-6)
  [Data register(TCDS)] ==> [Timer count data register(TCDS1,TCDS2)]

- 18.3.3 Detailed Description of Registers (Page 18-7)
     (1)Data register
  ==>(1)Timer count data register (TCDT1,TCDT2)
     (2)Control status register
  ==>(2)Timer count control status register (TCCS1,TCCS2)

- 18.4.1 Block Diagram
  Compare regisret 0/2 ==> Output compare register 0/2, 4/6
  Compare regisret 1/3 ==> Output compare register 1/3, 5/7
  OUT 0/2 ==> OUT 0/2,4/6
  OUT 1/3 ==> OUT 1/3,5/7
     The count values are output (T15 to T00)
  ==>The count values are output from TCDT1,TCDT2 (T15 to T00)
  Compare intrrupt 1/3 ==> Compare intrrupt 1/3,5/7
  Compare intrrupt 0/2 ==> Compare intrrupt 0/2,4/6

- 18.4.2 Register List (Page 18-11)
  Compare register, X=0 to 7 ==> Output compare register, X=0 to 7
  Control status register X= 0 to 7 ==> Output compare control status register

- 18.4.3 Detailed Description of Registers (Page 18-11)
  (1)Compare register ==> Output compare register (OCP0 to OCP7)

- (2)Control status register (Page 18-12)
     (2)Control status register
  ==>(2)Output compare control status register (OCS01, OCS23, OCS45, OCS67)

- 18.5.1 Block Diagram (Page 18-14)
  Capture data register 0 ==> Input capture data register 0
  Capture data register 1 ==> Input capture data register 1

- 18.5.2 Register list (Page 18-14)

Capture register ==>Input capture data register
Control status register ==>Input capture control status register 0 and 1
ICSx x=0 to 1 ==> ICS01

- 18.5.3 Detailed Description of Registers (Page 18-15)
(1)Input capture data register
==> (1)Input capture data register 0 and 1 (IPC0, IPC1)
(2)Control status register
==> (2)Input capture control status register 0 & 1(ICS01)

- APPENDIX A I/O Map (Page App.-3 to 5)
0Ch 0Dh, Compare register (ch.4) ==> 0Ch 0Dh, Output compare register (ch.4)
1Ch 1Dh, Compare register (ch.5) ==> 1Ch 1Dh, Output compare register (ch.5)
2Ch 2Dh, Compare control status register (ch.45) ==> 2Ch 2Dh, Output compare control status register (ch.45)
2Eh 2Fh, Compare control status register (ch.67) ==> 2Eh 2Fh, Output compare control status register (ch.67)
34h 35h, Compare register (ch.6) ==> 34h 35h, Output compare register (ch.6)
50h 51h, Input capture register (ch.0),IPCP0 ==> 50h 51h, Input capture data register (ch.0),IPCP0
52h 53h, Input capture register (ch.1),IPCP0 ==> 52h 53h, Input capture data register (ch.1),IPCP1
56h 57h, Timer data register,TCDT ==> 56h 57h,Timer count data register 1,TCDT1
58h, Timer control status register 1 ==> 58h, Timer count control status register 1
5Ah 5Bh, Compare register (ch.0) ==> 5Ah 5Bh, Output compare register (ch.0)
5Ch 5Dh, Compare register (ch.1) ==> 5Ch 5Dh, Output compare register (ch.1)
5Eh 5Fh, Compare register (ch.2) ==> 5Eh 5Fh, Output compare register (ch.2)
60h 61h, Compare register (ch.3) ==> 60h 61h, Output compare register (ch.3)
62h 63h, Compare control status register(ch.01) ==> 62h 63h, Output compare control status register(ch.01)
64h 65h, Compare control status register(ch.23) ==> 64h 65h, Output compare control status register(ch.23)
66h,Timer data register(Low),TCDTL2,..,67h,Timer data register(High),TCDTH2
==>66h 67h, Timer count data register 2,TCDT2
68h, Timer control status register 2 ==> 68h, Timer count control status register 2
6Ch 6Dh, Compare register (ch.7) ==> 6Ch 6Dh, Output compare register (ch.7)

- APPENDIX A I/O Map (Page App.-3)
36h 37h, Control Status register,ADCS1,ADCS2 ==> 36h 37h, A/D Control Status register ADCS0,ADCS1
38h 39h, Data register,ADCR1,ADCR2 ==> 36h 37h, A/D Data register ADCR0,ADCR1

- Capter5.1 (Page 5-3)(Page 5-7)
Watch timer control register:Bit3 WTR, (R)
==>Watch timer control register:Bit3 WTR, (R/W)

- 5.3.2 Tame-based timer control register (TBTC) (Page 5-6)
  Added information
  ==> Note: Please don't use read-modify-write instruction for TBTC register.
  Because read-modify-write instruction make miss operation at TBTC..

- 5.3.3 Watch Timer Control Register (WTC) (Page 5-7)
  WTC, Bit3, WTR,(R),(0) ==> WTC, Bit3, WTR,(R/W),(0)

- (4)Switching machine clock (Page 6-3)
  (2^13 machine clock) ==> (2^12 machine clock)

- [Bit 10] MCS (Page 6-8)
  wait time is fixed in 2^13 cycles of the main clock. ==> wait time is fixed in 2^12 cycles of the main clock.

- 26.4 FLASH Memory Control Status Register (FMCS) (Page 26-5)
  [Bit7] INTE(INTerrupt Enable)
  0:Interrupt allowed at end of programming and erasing ==> 0:Intrrupt disallowed at end of programming and erasing
  1:Intrrupt disallowed at end of programming and erasing ==> 1:Interrupt allowed at end of programming and erasing

- Subclock
  A Subclock crystal must be used even a subclock it is not needed in the
  application. Otherwise it may happen that the reset function does not work
  correctly. This also includes power-on reset.

1. Watchmode Problem

Condition: Watch Mode Subclock connected(normal operation) or Watchmode, No subclock connected

Description: If MCU has entered the Watch Mode and only the RST Reset signal
is asserted, it could happen, that the CPU does not restart correctly.

Workaraound: RST and HST reset must be asserted simultaneously.
Also a power-on reset will restart the CPU correctly again.

2. Voltage Drop down Problem

Condition: Voltage Drop on Vcc, No Subclock connected

Description: If no subclock is connected, it possibly may happen, that after a voltage drop on Vcc, the MCU does not restart correctly, even if RST and HST is asserted simultaneously.

Details:
If a voltage drop on Vcc occurs, there is no power-on reset executed, if the voltage Vcc does not drop below under 0.2V for a certain time

(toff), which is specified in the DS. See details on Vcc in the corresponding Datasheet. Normally, if HST & RST is asserted afterwards, the MCU would restart correctly. If no subclock is connected, it possibly may happen, that the CPU does not start/work correctly even after RST & HST reset.

Workaround:
a) The usage of a Subclock is highly recommended. If a Subclock is connected and a RST & HST Reset is asserted (RST = HST, reset simultaneously) the CPU will restart correctly.
b) Perform a correct power-on Reset (corresponding to Vcc timing specified in Datasheet)

Power On Reset:

Output “unknown value” , when the power supply Is turned on If F^2MC-16LX is used. (Note)

1.Device covered

- Flash products.

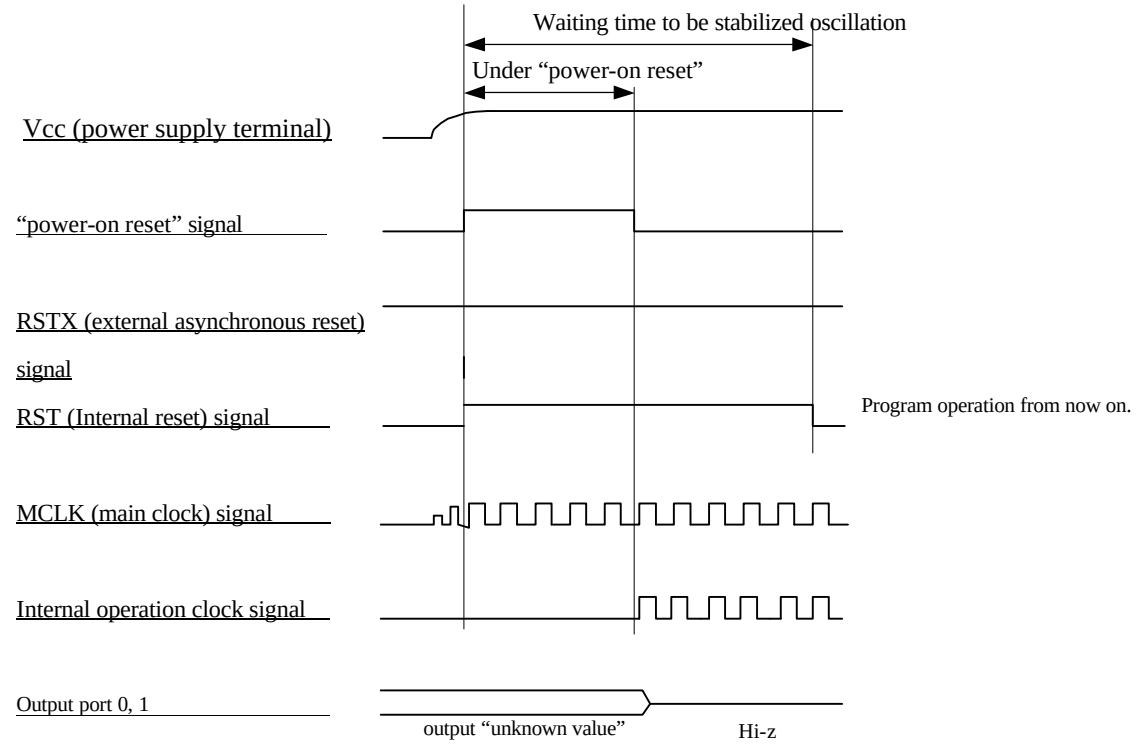
  MB90F523B

- Mask products.

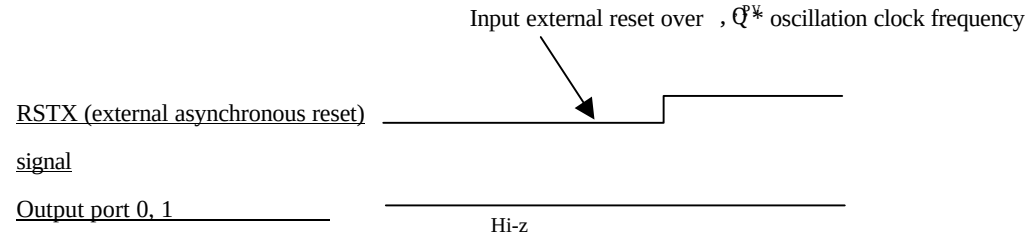
  MB90523

2. Note:
Output “unknown value” of pin 00 to pin 7 and pin 10 to pin 17 terminal, when the power supply Is turned on.

Pin 00 to pin 07 and pin 10 to pin 17 terminal become “unknown value” (output “H”, “L” level or output “Hi-z”) under “power-on reset” (stabilized times (2^{18} * oscillation clock frequency) of clamping circuit for internal power supply), when the power supply is turned on, and when “power-on reset” function operates and RSTX terminal is “H” level.
If you want to output “Hi-z” under “power-on reset”, it is applied reset input “ “L” level “ from external and so pin 00 to pin 07 and pin 10 to pin 17 terminal become “Hi-z” condition during the time.
It shows timing chart in detail the next page.
Note:
This workaround will work for Mode pin setting 011 (Single chip, Internal ROM external bus), 110 (Burn_In ROM), 111 (EPROM mode)



How to output “Hi-z” under “power-on reset”



Timing chart

Under “power-on reset” * oscillation clock frequency
(8.192ms in case of oscillation clock frequency = 16MHz)

Waiting time to be stabilized oscillation * oscillation clock frequency
(16.384ms in case of oscillation clock frequency = 16MHz)

Update 12 December 2000.