FUJITSU

Corrections of Hardware Manual

MB90540 -

HM90540_add_V100

Addendum, MB90540 Hardware Manual (CM44-10108-2E)

This is the Addendum for the Hardware Manual CM44-10108-2E microcontroller series. It describes all known discrepancies of the MB90540 microcontroller series Hardware Manual.

Ref. Number (Text Link)	Date dd.mm.yy	Version No.	Chapter/Page	Description/Correction
HWM90540001	01.06.01	1.00	Chapter 1.8	Info about power-on pin-state behaviour of MB90F54x, MB9054x added
HWM90540002	01.06.01		Chapter 11	Release from Watch Mode
HWM90540003	01.06.01		Chapter 1.8	Voltage drop down
HWM90540004	01.06.01		Chapter 5.1	Wrong PLL oscillation Stabilisation Time mentioned

Chapter 1.8 Handling the Device

MB90F54X, MB9054X: power-on pin-state behaviour

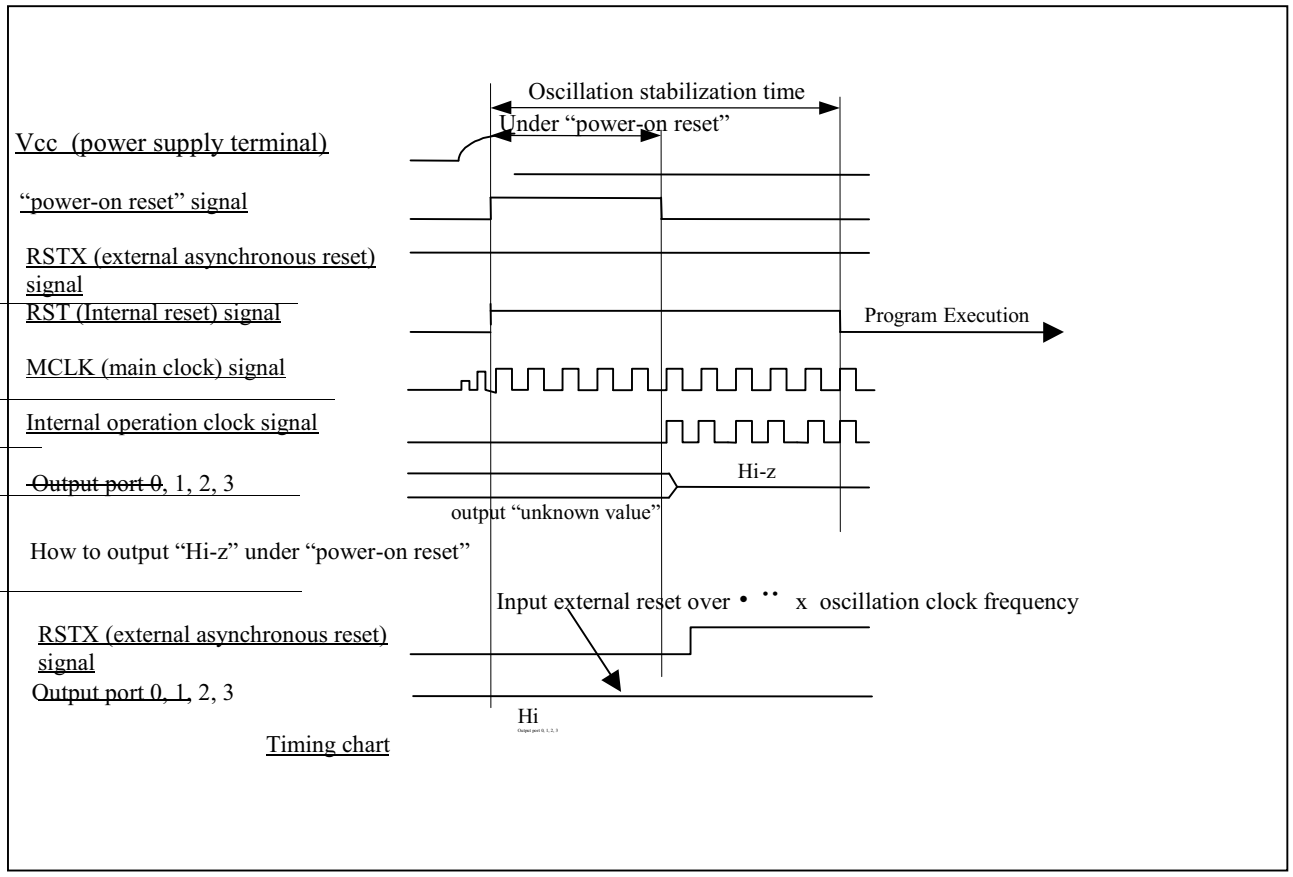
Conditions:
Mode pins = 011 (single chip mode), RSTX and HSTX = 1 during power-on

P00 to P37 = "X" (external bus)
P46, P47 = "X" (Serial IO outputs)
P76 to P84 = "X" (PPG, Output compare)
all other ports "Z"

P means Port, not pin. "X" can be anything (high, low, Z)

Asserting RSTX instantly sets all ports to "Z", even if the oscillation didn't start yet.

If RSTX is NOT asserted, the ports mentioned above remain "X" until the end of the power on reset time which is 2^17 oscillation cycles (32ms for 4MHz crystal). At the end of this time, the internal clock starts and ALL ports will be set to "Z".



Under "power-on reset" 2^{17} x oscillation clock frequency
(8.192ms in case of oscillation clock frequency = 16MHz)

Waiting time to be stabilized oscillation 2^{18} x oscillation clock frequency
(16.384ms in case of oscillation clock frequency = 16MHz).

HWM90540002

Chapter 11:

Watchmode

Condition: Watch Mode Subclock connected(normal operation) or Watchmode, No subclock connected

Description: If MCU has entered the Watch Mode and only the RST Reset signal is asserted, it could happen, that the CPU does not restart correctly.

Workaround: RST and HST reset must be asserted simultaneously.
Also a power-on reset will restart the CPU correctly again.

HWM90540003

Chapter 1.8 Handling the Device

Voltage Drop down

Condition: Voltage Drop on Vcc, No Subclock connected

Description: If no subclock is connected, it possibly may happen, that after a voltage drop on Vcc, the MCU does not restart correctly, even if RST and HST is asserted simultaneously.

Details:
If a voltage drop on Vcc occurs, there is no power-on reset executed, if the voltage Vcc does not drop below under 0.2V for a certain time (toff), which is specified in the DS. See details on Vcc in the corresponding Datasheet. Normally, if HST & RST is asserted afterwards, the MCU would restart correctly. If no subclock is connected, it possibly may happen, that the CPU does not start/work correctly even after RST & HST reset.

Workaround:

a) The usage of a Subclock is highly recommended. If a Subclock is connected and a RST & HST Reset is asserted (RST = HST, reset simultaneously) the CPU will restart correctly.
b) Perform a correct power-on Reset (corresponding to Vcc timing specified in Datasheet)

c) Usage of: MB90F543GS*, MB90F546GS*, MB90F548GS*, MB90F549GS*

***Note**: GS version is a **single clock** version and therefore not affected.
When using GS version: connect X0A to GND and leave X1A open.

Chapter 5: Low Power Control Circuits

Chapter 5.1: Overview

- Switching between main clock and PLL clock

Wrong PLL Oscillation stabilisation time mentioned.

Old:

When the MCS bit is changed from ‘1’ to ‘0’, the PLL clock takes over from the main clockafter the PLL clock stabilization wait time (2^{12} machine clock cycles).

New:

When the MCS bit is changed from ‘1’ to ‘0’, the PLL clock takes over from the main clock after the PLL clock stabilization wait time (2^{13} machine clock cycles).