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* New HW90550A New Number CM-44-10103-3E !!!!!!!!!!!!!!!! 24.11.99 *
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Correctiojn of Hardware Manual of MB90550A series

- Data register (Page 229+235)

Upper Bit15 Bit14 Bit13 Bit12 Bit11 Bit10 Bit9 Bit8

Address:00003Fh	S10	ST1	ST0	CT1	CT0	---	D9	D8	ADCR1
Read / Write:	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(-)	(R/W)	(R/W)	
Inital Value:	(0)	(0)	(0)	(0)	(1)	(-)	(X)	(X)	

(Page 235)

Lower Bit7 Bit6 Bit5 Bit4 Bit3 Bit2 Bit1 Bit0

- Address:00003Eh	D7	D6	D5	D4	D3	D2	D1	D0	ADCR0
Read / Write:	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	
Inital Value:	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)	

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- (2) External address output control register
All bits of these registers are write-only bits and their read value is aways 1.
==> All bits of these registers are write-only bits and their read value is aways 1.
Don't use read-modify-write instruction for this register.
If you use address output, you have to clear the DDR2 register.

- Fig.6.3-2 Read Timing Chart (Page 125)
Bottom Figure:
Even address word read ==> Even address word write
Even address word write ==> Even address word read

- Table 5.4-3 Page (103) Each Pin States in External Bus 16-bit Mode (Page 6-13)
P17 to P10 (AD07 to AD00), Input impossible/Output Hi-z (@Sleep, Stop SPL=0, Reset)
==> P17 to P10 (AD07 to AD00), OUTput state*1 (@Sleep, Stop SPL=0, Reset)
P33(WRH), High output (@Sleep, Stop SPL=1), Input impossible/Output Hi-z (@Hold)
==> P33(---), Immediately-preceding state hold (@Sleep, Hold),
Input cut off/immediately-preceding state hold (@Stop SPL=0)

- 13.1 Register List
(1)Upper of serial mode control status register (Page 13-3)
Address,ch0 000025h, ch1 000029h ==> Address,ch0 000024h, ch1 000028h
(2)Lower of serial mode control status register
Address,ch0 000024h, ch1 000028h ==> Address,ch0 000025h, ch1 000029h

- 13.3.1Serial Mode Control Status Register (SMCS) (Page 13-5)
(1)Upper of serial mode control status register (Page 13-3)
Address,ch0 000025h, ch1 000029h ==> Address,ch0 000024h, ch1 000028h

(2)Lower of serial mode control status register
Address,ch0 000024h, ch1 000028h ==> Address,ch0 000025h, ch1 000029h

- (1)16-bit free-run timer (x 1) (Page 6-3)
Four internal clocks (phi/4, phi/16, phi/32, phi/64) ==> Four internal clocks (phi/4, phi/16, phi/64, phi/128)

- Figure 21.2.2 (Page 319) Program Address Detect Control Status Register (PACSR) (Page 319)
Address 009Eh(R/W,0), AD1E(R/W,0), AD1D(R/W,0), AD0E(R/W,0), AD0D(R/W,0), PACSR
==>Address 009Eh(R/W,0), AD1E(R/W,0), Reserved(-,-), AD0E(R/W,0),Reserved(-,-) , PACSR
[Bit 2, Bit 0] These are reserved bits. if you have access this register, have to clear bit2 and bit0 only.

- 1.1 Feature (Page 3)
Internal ROM (EPROM 128 KB) ==> Internal ROM (OTP device:128 KB, FRASH device:128KB)
Internal RAM (EPROM 4KB) ==> Internal RAM (OTP device:4KB, FRASH device:4KB)

- Additional Data Sheet information
- minimum value of AVRH is AVRL + 2.7V.
- maximum value of AVRL is AVRH - 2.7V.

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