FUJITSU

Corrections of Hardware Manual

MB90560/5 -

HM90560_add_V101

Addendum, MB90560/5 Hardware Manual (CM42-10107-4E)

This is the Addendum for the Hardware Manual CM42-10107-4E of the MB90560/5 microcontroller series. It describes all known discrepancies of the MB90560/5 microcontroller series Hardware Manual.

Ref. Number (Internal ref. number) (Text Link)	**Date** dd.mm.yy	**Version No.**	**Chapter/Page**	**Description/Correction**
HWM90560001	11.06.01	1.00	6.4.5	Interrupt Processing time
HWM90560002	11.06.01	1.00	1.8	Power On Reset
HWM90560003	11.06.01	1.00	19	Flash Security Feature
HWM90560004	11.06.01	1.00	1.8	Handling the Device, Information about reserved memory area
HWM90560005	28.06.01	1.01	1.8	RTO Port behaviour during Reset

HWM90560001

Chapter 6.4.5 Interrupt processing Time

The correct interrupt processing time is calculated with:
When returning from an interrupt : o = 15 + 6 * z machine cycles

HWM90560002

Power-On Reset
==========

Output "unknown value" , when the power supply Is turned on If F^2MC-16LX is used. (Note)

1.Device covered

MB90V560, MB90F562, MB90F568,
MB90561, MB90562, MB90567, MB90568

2. Note:

During testing it has been found that some port pins may enter an undefined state during power on. By asserting RSTx during the power on reset (2^{17} cycles of main clock) port pins can be forced to high impedance.

The following Ports will output a High Impedance (Hi-z) at the terminal when the power supply is turned on when PONR and RSTX = 1:

P40 - P67

The following ports will output High Impedance (High-Z) on RSTX or with the End of PONR and Start of internal clocks:

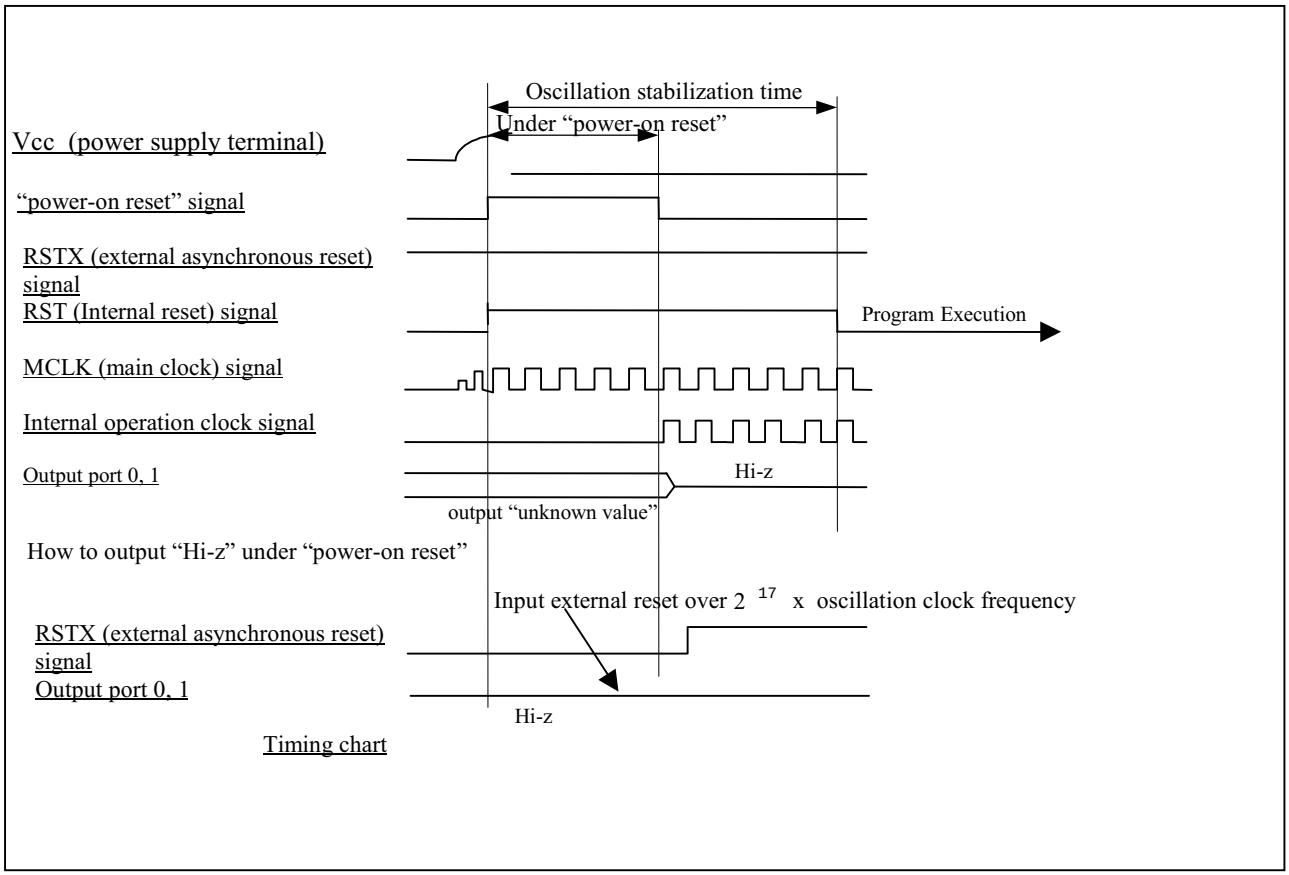
P00 - P17

The following Ports will output High Impedance (high-Z) with the End of PONR and Start of the internal Clock. RSTX does not force the pins to high-Z during power on.

P20 - P37

Note:
This workaround will work for Mode pin setting 011 (Single chip, Internal ROM external bus), 110 (Burn_In ROM), 111 (EPROM mode)

The following diagram shows the timing chart in detail.



Under "power-on reset" 2^{17} x oscillation clock frequency
(8.192ms in case of oscillation clock frequency = 16MHz)

Waiting time to be stabilized oscillation 2^{18} x oscillation clock frequency
(16.384ms in case of oscillation clock frequency = 16MHz).

HWM90560003

CHAPTER 19 512K-BIT (64 KB) FLASH MEMORY

Flash Security Feature
==========

Correction:

The Flash Security Feature is not inside MB90F562 Series, these Feature is **only** inside **MB90F562B** Series!

19.7 Flash Security Feature

The Flash Security Controller provides possibilities to protect the content of the flash memory from being read from external pins.

One predefined address of the flash memory is assigned to the Flash Security Controller (MB90F562B: FF0001H). If the protection code of "01H" is written in this address, access to the flash memory is restricted. Once the flash memory is protected, performing the chip erase operation only can unlock the function otherwise read/write access to the flash memory from any external pins is not generally possible.
This function is suitable for applications requiring security of self-containing program and data stored in the flash memory. If the target application requires any part of the program to locate outside the microcontroller, the Flash Security Controller cannot offer the intended features. For this reason, the External Vector Fetch mode should not be used when the protection code is set.
Programming of the flash microcontroller by standard parallel programmer may require unique set-up. For example, with the programmer from Minato Electronics the device checking should be turned off. Writing the protection code is generally recommended to take place at the end of the flash programming. This is to avoid unnecessary protection during the programming. In order to re-program the once protected flash memory, the chip erase operation should be performed.
For further information, please contact Fujitsu.

HWM90560004

Chapter 1.8 Handling the Device

Reserved Area
==========
Last Word of Memory (FFFFFE – FFFFFF) is reserved AREA. Do not use this last WORD.

Chapter 1.8 Handling the device

RTO Port pin (P30-P35) behaviour during Reset

When using RTO port Function or the port pins P30-P35, the following behaviour occurs if the external RST Reset pin is asserted:

When asserting RST low, the RTO Ports (P30-P35) will drive active ‘High’ Level about 400 ns, starting with the falling edge of the RST signal. This might cause problems in some kind of applications.

Especially in case of IGBT drivers, a workaround could be used to disable the output drivers during reset. This could be done e.g by using an additional I/O port, which is tristate during RST. With a corresonding pull-up/down resistance at this port, the level on this pin can be hold high/low during reset in order to keep the driver disabled. After the reset the drivers could be enabled by initialising the port pin correspondingly by software.