FUJITSU

Corrections of Hardware Manual

MB90570/A -

HM90570/A_add_V100

Addendum, MB90570/A Hardware Manual (CM-44-10102-7E)

This is the Addendum for the Hardware Manual CM-44-10102-7E of the MB90570/A microcontroller series. It describes all known discrepancies of the MB90570/A microcontroller series Hardware Manual.

Ref. Number (Text Link)	Date dd.mm.yy	Version No.	Chapter/Page	Description/Correction
HWM90570001	20.04.01	V1.00		Differences between MB90570 and MB90574A series
HWM90570002	20.04.01		Chapter 14.1	Up/Down Counter, incorrect count clock time
HWM90570003	20.04.01		Chapter 1.2	Product Lineup, wrong RAM size of MB90573 mentioned
HWM90570004	20.04.01		Chapter 10	Conditions when release from Watchmode
HWM90570005	20.04.01		Chapter 1	Condition when Voltage drop down
HWM90570006	20.04.01		Chapter 1	Information about Pinstate behaviour during Power-on
HWM90570007	20.04.01		Chapter 19	UART, SCR Register bit definition of PEN-bit exchanged

HWM90570001

Differences between MB90570 and MB90574A series:

Reset behaviour:

MB90F574, MB90573,MB90574, MB90V570:
Connect always main clock and subclock

MB90F574A, MB90574A, MB90V570A:
When subclock is not used, it must not connect

Request of return from Stop mode:

MB90F574, MB90573,MB90574, MB90V570:
The request of return from STOP mode is High level.
MB90F574A, MB90574A, MB90V570A:
Edge detection (high/low) for return from STOP mode.

Leakage current of DAC:

MB90573, MB90574: (other O.K.)
Use DVcc =>3,3V

MB90574A:
Fixed

HWM90570002

Chapter 14.1 Functions of 8/16-Bit Up/Down Counter/Timer

Count clock (for 16-MHz operation)

Old:
1.0us (2MHz: divided by 8)
Correct:
0.5us (2MHz: divided by 8)

HWM90570003

Chapter 1.2 Product Line-up

Typo in the table, incorrect RAM size mentioned. See correction below.

Table 1.2-1

	MB90573
ROM size	128Kbyte
RAM size	5 Kbyte
Others	MASK products

HWM90570004

Chapter 10: Watchdog Timer, Time base timer an Watch timer

Watchmode Problem

Condition: Watch Mode Subclock connected(normal operation) or Watchmode, No subclock connected

Description:
If MCU has entered the Watch Mode and only the RST Reset signal is asserted, it could happen, that the CPU does not restart correctly.

Workaround:
RST and HST reset must be asserted simultaneously. Also a power-on reset will restart the CPU correctly again.

HWM90570005

Voltage Drop down Problem

Condition: Voltage Drop on Vcc, No Subclock connected

Description:
If no subclock is connected, it possibly may happen, that after a voltage drop on Vcc, the MCU does not restart correctly, even if RST and HST is asserted simultaneously.

Details:
If a voltage drop on Vcc occurs, there is no power-on reset executed, if the voltage Vcc does not drop below under 0.2V for a certain time (toff), which is specified in the DS. See details on Vcc in the corresponding Datasheet. Normally, if HST & RST is asserted afterwards, the MCU would restart correctly. If no subclock is connected, it possibly may happen, that the CPU does not start/work correctly even after RST & HST reset.

Workaround:
a) The usage of a Subclock is highly recommended. If a Subclock is connected and a RST & HST Reset is asserted (RST = HST, reset simultaneously) the CPU will restart correctly.
b) Perform a correct power-on Reset (corresponding to Vcc timing specified in Datasheet)

Power-On Reset

Output “unknown value” , when the power supply Is turned on If F^{2}MC-16LX is used. (Note)

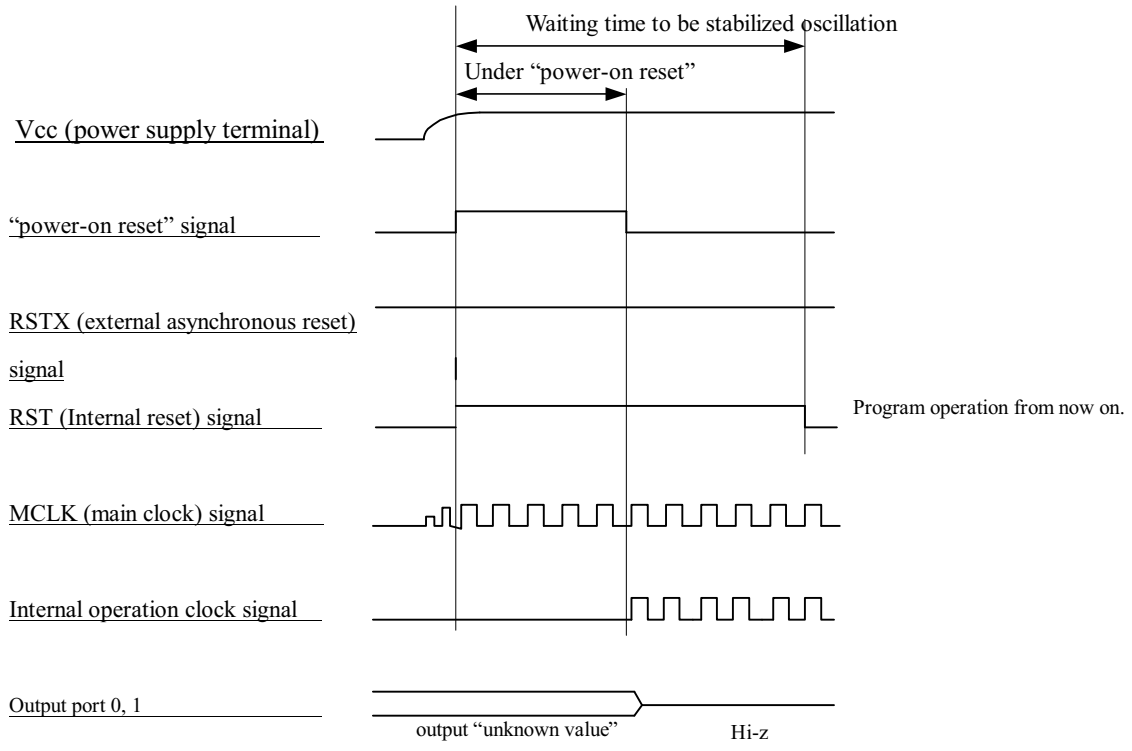
1.Device covered

MB90574

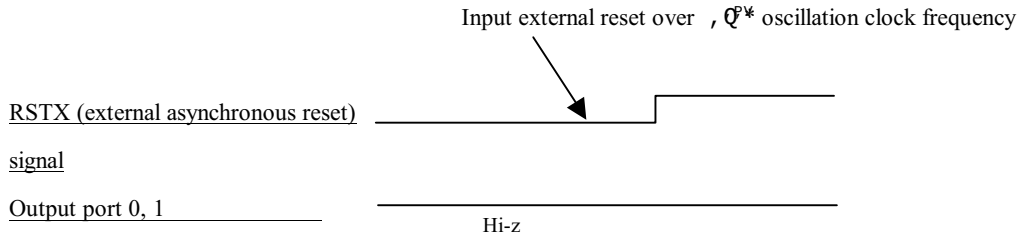
2. Note:
Output “unknown value” of pin 00 to pin 7 and pin 10 to pin 17 terminal, when the power supply Is turned on.

Pin 00 to pin 07 and pin 10 to pin 17 terminal become “unknown value” (output “H”, “L” level or output “Hi-z”) under “power-on reset” (stabilized times (2¨ * oscillation clock frequency) of clamping circuit for internal power supply), when the power supply is turned on, and when “power-on reset” function operates and RSTX terminal is “H” level.
If you want to output “Hi-z” under “power-on reset”, it is applied reset input “ “L” level “ from external and so pin 00 to pin 07 and pin 10 to pin 17 terminal become “Hi-z” condition during the time.
It shows timing chart in detail the next page.

Note:
This workaround will work for Mode pin setting 011 (Single chip, Internal ROM external bus), 110 (Burn_In ROM), 111 (EPROM mode)



How to output “Hi-z” under “power-on reset”



Timing chart

Under “power-on reset” •¨ * oscillation clock frequency
(8.192ms in case of oscillation clock frequency = 16MHz)

Waiting time to be stabilized oscillation •¨ * oscillation clock frequency
(16.384ms in case of oscillation clock frequency = 16MHz)

Chapter 19 UART

Chapter 19.3 Serial Control Register (SCR)

[bit 15] PEN (Parity Enable)

Bit definition exchanged

See correction below:

0	Parity not added
1	Parity added