FUJITSU

Corrections of Hardware Manual

MB90595 -

HM905595_add_V106

Addendum, MB90595 Hardware Manual (CM44-10106-2E)

This is the Addendum for the Hardware Manual CM44-10106-2E of the MB90595 microcontroller series. It describes all known discrepancies of the MB90595 microcontroller series Hardware Manual.

Ref. Number (Text Link)	Date dd.mm.yy	Version No.	Chapter/Page	Description/Correction
HWM90595001	04.04.00	1.0	Chapter 23	Important information about Reset Vector addresses for Flash and Mask versions
HWM90595002	04.04.00		Chapter 15.5.1	Wrong ICR register for A/DC mentioned
HWM90595003	04.04.00		Chapter 13.3.3	PPG Count clock selection bit: wrong time scales, wrong bit identifier
HWM90595004	04.04.00		Chapter 22.2	ROM Mirroring Function Selection Register: wrong Memory area mentioned
HWM90595005	29.05.00	1.01	Chapter 5.1 Chapter 6.2 Chapter 6.6 Chapter 24	External Clock frequency
HWM90595006	29.05.00		Chapter 23	Chapter 23.8 and 23.9 added
HWM90595007	29.05.00		Chapter 1.8	Handling unused pins, further description added
HWM90595008	19.09.00	1.03	Chapter 19	CAN, difference G and none-G series
HWM90595009	06.10.00	1.04	Chapter 20	Stepper Motor, information about Zero Detect register added
HWM90595010	18.01.01	1.05	Chapter 8	Information about Pinstate behaviour during Power-on

HWM90595011	17.05.01	1.06	Chapter 23	Flash sector size have been changed for non G-Version

HWM90595001

Chapter 23 Flash Programming:

Reset Vector Addresses in Flash Memory

The MB90595 Series devices with Flash memory (e.g. MB90F598) supports the Hard-wired Reset Vector.
Any read access in the internal vector mode to the addresses from FFFFDC H to FFFFDF H
results in reading the predetermined value by the hard-wired logic. However in the
Flash Memory mode, these addresses can be accessed as described in the previous sections.
Therefore writing to these addresses has no meaning. Especially when programming the
Flash Memory with the CPU access (not in the Flash Memory mode), pay attention not
to read these addresses by soft-ware polling. Otherwise the Flash Memory returns the
fixed reset vector value instead of the hardware sequence flag values.
The following table shows the predetermined values for the reset vector and mode data.

Reset Vector FFA000 H
Mode Data 00 H

Note: For mask version no hardwired reset vector is used. So for mask version an accurate
reset vector must be defined and the mode data must be set to 00 H (single chip mode).

Chapter 5.2: Reset Cause Occurence

WARNING: For the MB90595 Series devices with Flash memory, the reset vector is hard-wired to FFA000H and the mode data is hard-wired to 00H (refer to 23.9 Reset Vector Address in Flash Memory). If a reset vector other than FFA000H or mode data other than 00H are used in a software code, then this code will behave differently between Mask ROM and Flash devices.

Chapter 7.3 Mode Data:

WARNING: For the MB90590 Series devices with Flash memory, the mode data is hard-wired to 00H (refer to 23.9 Reset Vector Address in Flash Memory). If a mode data other than 00H is used in a software code, then this code will behave differently between Mask ROM and Flash devices.

HWM90595002

Chapter 15.5.1 Example of EI2OS Activation in single Mode:

Wrong comment below the table:
A/D Converter is located to ICR3 instead of ICR2

HWM90595003

Chapter 13.3.3 PPG0,1 Output Pin Control Register (PPG01)

Incorrect time scales in table, see correction below:

PCS2	PCS1	PCS0	Operation mode
0	0	0	Periphal clock (62,5 ns machine clock, 16MHz)
0	0	1	Periphal clock/2 (125 ns machine clock, 16MHz)
0	1	0	Periphal clock/4 (250 ns machine clock, 16MHz)
0	1	1	Periphal clock/8 (500 ns machine clock, 16MHz)
1	0	0	Periphal clock/16 (1 µs machine clock, 16MHz)
1	0	1	Clock input from the time base timer (128 µs, 4MHz)

This bit is initialised to ‘000‘ upon a reset. This bit is readable and writable.

Incorrect time scales and wrong bit definition in table, see correction below:

PCM2	PCM1	PCM0	Operation mode
0	0	0	Periphal clock (62,5 ns machine clock, 16MHz)
0	0	1	Periphal clock/2 (125 ns machine clock, 16MHz)
0	1	0	Periphal clock/4 (250 ns machine clock, 16MHz)
0	1	1	Periphal clock/8 (500 ns machine clock, 16MHz)
1	0	0	Periphal clock/16 (1 µs machine clock, 16MHz)
1	0	1	Clock input from the time base timer (128 µs, 4MHz)

This bit is initialised to ‘000‘ upon a reset. This bit is readable and writable.

HWM90595004

Chapter 22.2 ROM Mirroring Function Selection Register (ROMM)

Wrong memory area mentioned, see following correction:

Note:
Only FF4000 to FFFFFF is mirrored to 004000 to 00FFFF when ROM mirroring function is activated. Therefore, addresses FF0000 to FF3FFF will not be mirrored to 00 bank.

HWM90595005

Chapter 5.1 Clock Generator

Typo in the external clock frequency range description:

old:
"When the operating voltage is 5 V, the OSC source oscillation can be between 3 MHz and 16 MHz."

new:
"When the operating voltage is 5 V, the OSC source oscillation can be between 3 MHz and 5 MHz. When an external clock source is used, its frequency can be between 3 MHz and 16 MHz."

old:
"For example, if the source oscillation is 16 MHz, only 1 can be specified as the multiplication factor."
new:
"For example, if the external clock frequency is 16 MHz, only 1 can be specified as the multiplication factor."

Chapter 6.2.2 Clock selection Register:

Wrong external clock frequency range mentiend in the Notes of these chapter:

old:
"When the operating voltage is 5 V, the OSC source oscillation can be between 3 MHz and 16 MHz."
new:
"When the operating voltage is 5 V, the OSC source oscillation can be between 3 MHz and 5 MHz. When an external clock source is used, its frequency can be between 3 MHz and 16 MHz."

old:
"For example, if the source oscillation is 16 MHz, only 1 can be specified as the multiplication factor."
new:
"For example, if the external clock frequency is 16 MHz, only 1 can be specified as the multiplication factor."

Chapter 6.6 Status Transition Clock Selection

Source oscillation range changed:
old:
"When the operating voltage is 5 V, the OSC source oscillation can be between 3 MHz and 16 MHz."
new:
"When the operating voltage is 5 V, the OSC source oscillation can be between 3 MHz and 5 MHz. When an external clock source is used, its frequency can be between 3 MHz and 16 MHz."

Chapter 24 Examples of F²MC-16LX MB90F598 serial write connection

There is also wrong external clock frequency mentioned:

Change Table 24.1-1 and Figures 24.2-1, 24.3-1, 24.4-1, 24.5-1

old: "1 MHz to 16 MHz"
new: "3 MHz to 5 MHz"

HWM90595006

Chapter 23 1M-Bit Flash Memory

Chapter 23.8 and 23.9 added

23.8 Notes on using 1M-Bit Flash Memory

This section contains notes on using 1M-bit flash memory.

❑ **Notes on using flash memory**

- **Input of a hardware reset (RST)**

To input a hardware reset when the automatic algorithm has not been started and reading is in progress, a minimum low-level width of 500 ns must be maintained. In this case, a maximum of 500 ns is required until data can be read from the flash memory after a hardware reset has been activated. Similarly, to input a hardware reset when the automatic algorithm has been activated and writing or erasing is in progress, a minimum low-level width of 50 ns must be maintained. In this case, 20 (s are required until data can be read after the operation for initializing the flash memory has terminated. A hardware reset during writing the data being written to be undefined. A hardware reset during erasing may make the sector being erased unusable.

- **Canceling of a software reset, watchdog timer reset, and hardware standby**

When the flash memory is being written to or erased with CPU access and if reset conditions occur while the automatic algorithm is active, the CPU may run out of control. This occurs because these reset conditions cause the automatic algorithm to continue without initializing the flash memory unit, possibly preventing the flash memory unit from entering the read state when the CPU starts the sequence after the reset has been deasserted. These reset conditions must be disabled during writing to or erasing of the flash memory.

- **Program access to flash memory**

When the automatic algorithm is operating, read access to the flash memory is disabled. With the memory access mode of the CPU set to internal ROM mode, writing or erasing must be started after the program area is switched to another area such as RAM. In this case, when sectors (SA6) containing interrupt vectors are erased, writing or erasing interrupt processing cannot be executed. For the same reason, all interrupt sources other than the flash memory are disabled while the automatic algorithm is operating. Also, while the automatic algorithm is being executed, all interrupt sources except flash memory are disabled.

- **Hold function**

When the CPU accepts a hold request, the Write signal WE of the flash memory unit may be skewed, causing erroneous writing or erasing due to an erroneous write. When the acceptance of a hold request is enabled (HDE bit of EPCR set to 1), ensure that the WE bit of the control status register (FMCS) is 0.

- **Extended intelligent I/O service (EI 2 OS)**

Because write and erase interrupts issued to the CPU from the flash memory interface circuit
cannot be accepted by the EI 2 OS, they should not be used.

- **Applying V ID**

Applying V ID required for the sector protect operation should always be started and terminated
when the supply voltage is on.

23.9 Reset Vector Address in Flash Memory

The MB90F598 supports a hard-wired reset vector.
When the addresses FFFFDC H to FFFFDF H are accessed for reading data in internal vector mode, the values that have been determined by the hard-wired logic in advance are read. However, in flash memory mode, as mentioned in the previous chapter, all addresses can be accessed.
Consequently, it is meaningless to write data to these addresses. Especially when programming flash memory from the CPU (that is, not in flash memory mode), do not read these addresses for software polling. Otherwise, the flash memory returns a fixed reset vector instead of the hardware sequence flag value.

- Reset vector address in flash memory

The following table shows the reset vector and mode data values determined in advance.

Reset vector	FFA000 H
Mode data	00 H

WARNING: Even though the Reset Vector is hard-wired to FFA000H and the mode data is hard-wired to 00H, always make sure that the same values are used in your software code. If different values for reset vector and mode data are used in your code, then this code will behave differently between Mask ROM and Flash devices.

HWM90595007

Chapter 1.8 Handling Device

"Handling unused input pins" paragraph is changed to following"

Handling unused input pins

Leaving unused input pins open may result in misbehaviour or latch up and possible permanent damage of the device. Therefore they must be tied to VCC or Ground through resistors. In this case those resitors should be more than 2Kohm.
Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

Chapter 19 CAN

Chapter 19.6.5 Bit Timing Register (BTR)

Old:

For correct operation, the following conditions should be met.

BT >= 8TQ
TSEG2 >= RSJW + 2TQ*1
TSEG1 >= delay time*2 + RSJW

*1) 2TQ: Data processing time
*2) Delay time: Twice as long as the sum of the bus propagation, input comparator and output driver delay

New:

For correct operation of the CAN controller, the following conditions should be met:

Devices with "G" suffix:

    For 1 <= PSC <= 63:
        TSEG1 >= 2TQ
        TSEG1 >= RSJW
        TSEG2 >= 2TQ
        TSEG2 >= RSJW

    For PSC = 0:
        TSEG1 >= 5TQ
        TSEG2 >= 2TQ
        TSEG2 >= RSJW

Devices without "G" suffix:

    For 1 <= PSC <= 63:
        TSEG1 >= RSJW
        TSEG2 >= RSJW + 2TQ

    For PSC = 0:
        TSEG1 >= 5TQ
        TSEG2 >= RSJW + 2TQ

In order to meet the Bit Timing requirements defined in the CAN Specification, additional conditions have to be met, e.g. the propagation delay has to be considered.

Chapter 20.1 Outline of Stepping Motor Controller

Old:

The Stepping Motor Controller consists of two PWM Pulse Generators, four motor drivers and the Selector Logic.
The four motor drivers have high output drive capabilities and they can be directly
connected to the four ends of two motor coils. The combination of the PWM Pulse
Generators and Selector Logic is designed to control the rotation of the motor. A
synchronization mechanism assures the synchronous operations of the two PWMs.
The following sections describe the Stepping Motor Controller 0 only. The other
controllers have the same function. The register addresses are found in the I/O map.

New:

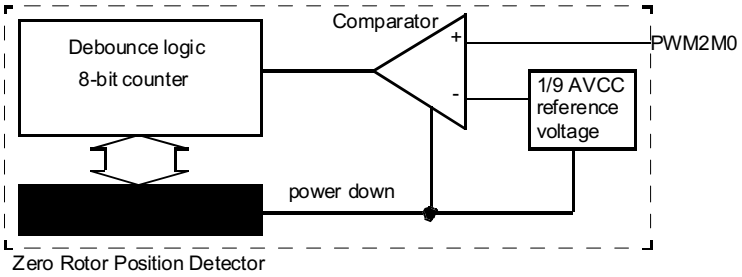
This Chapter provides an overview of the Stepper Motor Control Module, describe the register structure and functions, and described the operation of the Stepper Motor Control Module.

The Stepping Motor Controller consists of two PWM Pulse Generators, four motor drivers, Selector Logic and the Zero Rotor Position Detector. The four motor drivers have high output drive capabilities and they can be directly connected to the four ends of two motor coils. The combination of the PWM Pulse Generators and Selector Logic is designed to control the rotation of the motor. A Synchronization mechanism assures the synchronous operaitons of the two PWMs. The Zero Rotor Position Detector helps CPU obtain feed back information of the rotor movements. The following sections describe the Stepping Motor Controller 0 only. The other controllers have the same functions. The register addresses are found in the I/O map.

<Note> The Rotor Zero Position Detection capability is protected by a patent from Mannesmann VDO and may only be used with VDO’s prior approval.

- Stepping Motor Control Block

Additionally Diagram:



Chapter 20.2 Stepping Motor Control Registers:

Additionally Register ZPDC:

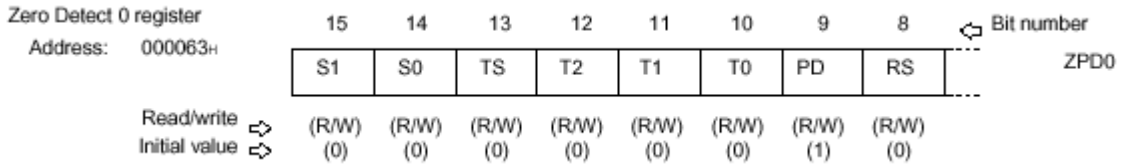
Zero Detect 0 register
Address: 000063H

15	14	13	12	11	10	9	8	⇦ Bit number
S1	S0	TS	T2	T1	T0	PD	RS	ZPD0
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	⇦ Read/write
(0)	(0)	(0)	(0)	(0)	(0)	(1)	(0)	⇦ Initial value

I/O MAP:

62 H	PWM Control 0	PWC0	R/W	Stepping Motor Controller 0	00000__0
63 H	Zero Detect 0	ZPD0	R/W		00000010
64 H	PWM Control 1	PWC1	R/W	Stepping Motor Controller 1	00000__0
65 H	Zero Detect 1	ZPD1	R/W		00000010
66 H	PWM Control 2	PWC2	R/W	Stepping Motor Controller 2	00000__0
67 H	Zero Detect 2	ZPD2	R/W		00000010
68 H	PWM Control 3	PWC3	R/W	Stepping Motor Controller 3	00000__0
69 H	Zero Detect 3	ZPD3	R/W		00000010

Chapter 20.2.4 Zero Detect Register



[bits 15 to 14] S1 to S0 : Debounce clock select bit

These bits specify the clock frequency used for the Debounce logic. The Debounce logic samples the output of the comparator with the specified clock frequency.

S1	S0	Clock input
0	0	Machine clock
0	1	½ Machine clock
1	0	¼ Machine clock
1	1	1/8 Machine clock

[bits 13] TS : Time slice bit

This bit enables the operation of the Zero Rotor Position Detector. While this bit is "1", the Zero Rotor Position Detector compares the input voltage at the PWM2M0 pin with the reference voltage and sets the RS bit if the input voltage exceed the reference voltage.

[bits 12 to 10] T2 to T0 : Number of samples

These bits specifies the number of samples for the Debounce logic. The Debounce logic samples the output of the comparator the specified number of times. The output of the Debounce logic becomes "1" when all the sampled values are "1"

T2	T1	T0	Number of samples
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	1	1	5

[bits 9] PD : Power down bit

When this bit is set to "1", the power supply to the analog components (comparator and reference voltage source) is switched off.

age source) is switched off.

[bits 8] RS : Result bit

The RS bit indicates whether the input voltage at the PWM2M0 pin exceeded the reference voltage.

The RS bit is set to "1" if the output of the Debounce logic becomes "1". While TS bit is "0", the RS bit always indicates "0".

Power-On Reset

Output "unknown value" , when the power supply Is turned on If F^2MC-16LX is used. (Note)

1.Device covered

MB90V595G, MB90598, MB90F598, MB90F598G

2. Note:

During testing it has been found that some port pins may enter an undefined state during power on. By asserting RSTx during the power on reset (2^{17} cycles of main clock) port pins can be forced to high impedance.

1. The following Ports will output a High Impedance (Hi-z) at the terminal when the power supply is turned on when PONR and RSTX = 1 (RSTx not asserted):

P20 – P45, P50 – P67, P90 – P95

2. The following ports can be forced to high impedance state (Hi-z) during PONR if RSTX is asserted during power on (2^{17} cycles of main clock) or with the End of POMR and the Start of the internal clock

P00 – P03, P16 – P17, P46 – P47, P70 – P87

3. The following Ports will output an High-Z with the End of PONR and the Start of internal clocks. RSTx does not force the pins to High-Z during power on.

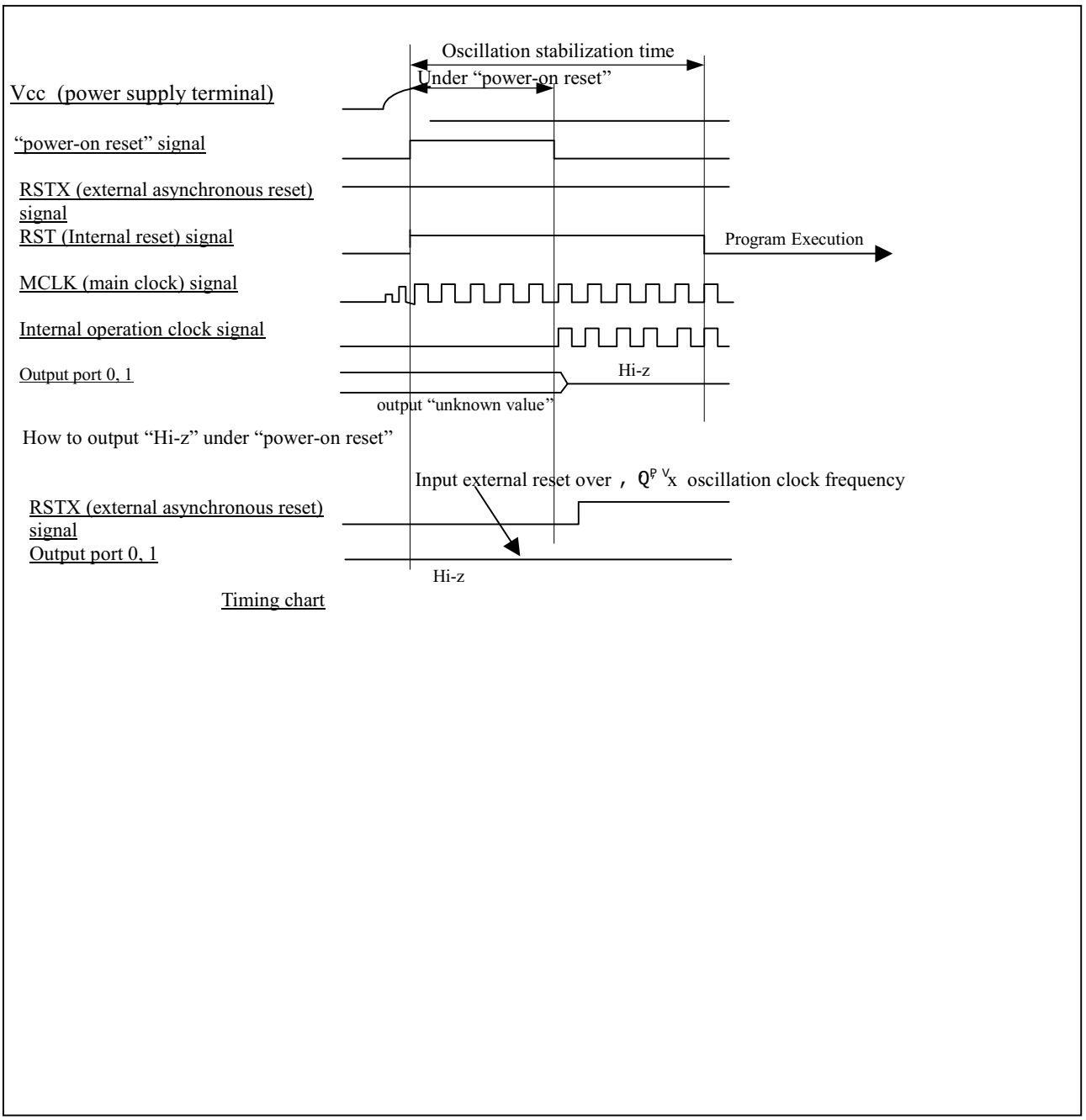
P04 – P15

Note:
This workaround will work for Mode pin setting 011 (Single chip, Internal ROM external bus), 110 (Burn_In ROM), 111 (EPROM mode)

The following diagram shows the timing chart in detail.

See also Datasheet of MB90595/595G series (DS07-13705-2E)

HANDLING DEVICES, (11) Indeterminate outputs from port 0 and 1



Under “power-on reset” □□□ x oscillation clock frequency
(8.192ms in case of oscillation clock frequency = 16MHz)

Waiting time to be stabilized oscillation □□□ x oscillation clock frequency
(16.384ms in case of oscillation clock frequency = 16MHz)

In the G-Version of the MB90F598G the Flash sectors size have been changed. The Table below shows the sector size of the non G-Version.

CHAPTER 23 1M-Bit Flash Memory

Figure 23.2-2 Sector Configuration of the 1M-bit Flash Memory

Flash memory	CPU address	Writer address (*1)
SA 6 SA6 (16K bytes)	FFFFFFh FFC000h	7FFFFh 7C000h
SA 5 SA5 (512 bytes)	FFBFFFh FFBE00h	7BFFFh 7BE00h
SA 4 SA4 (512 bytes)	FFBDFFh FFBC00h	7BDFFh 7BC00h
SA 3 SA3 (7K bytes)	FFBBFFh FFA000h	7BBFFh 7A000h
SA 2 SA2 (8K bytes)	FF9FFFh FF8000h	79FFFh 78000h
SA 1 SA1 (32K bytes)	FF7FFFh FF0000h	77FFFh 70000h
SA 0 SA0 (64K bytes)	FEFFFFh FE0000h	6FFFFh 60000h

*1 Use the writer address for writing/erasing with a parallel writer.

The sectors SA5 and SA4 are merged together with the sector SA3. The sector size for the G-Version are as followed:

128k = 64k + 32k + 8k + 8k + 16k