FUJITSU

Corrections of Hardware Manual

MB90595 -

HM905595_add_V100

Addendum, MB90595 Hardware Manual (CM44-10106-3E)

This is the Addendum for the Hardware Manual CM44-10106-3E of the MB90595 microcontroller series. It describes all known discrepancies of the MB90595 microcontroller series Hardware Manual.

Ref. Number (Text Link)	Date dd.mm.yy	Version No.	Chapter/Page	Description/Correction
HWM90595001	08.08.01	1.00	Chapter 15.5.1	Wrong ICR register for A/DC mentioned
HWM90595002	08.08.01		Chapter 13.3.3	PPG Count clock selection bit: wrong time scales, wrong bit identifier
HWM90595003	08.08.01		Chapter 20	Stepper Motor, information about Zero Detect register added
HWM90595004	08.08.01		Chapter 1.8	Information about Pinstate behaviour during Power-on

HWM90595001

Chapter 15.5.1 Example of EI2OS Activation in single Mode:

Wrong comment below the table:
A/D Converter is located to ICR3 instead of ICR2

HWM90595002

Chapter 13.3.3 PPG0,1 Output Pin Control Register (PPG01)

Incorrect time scales in table, see correction below:

PCS2	PCS1	PCS0	Operation mode
0	0	0	Periphal clock (62,5 ns machine clock, 16MHz)
0	0	1	Periphal clock/2 (125 ns machine clock, 16MHz)
0	1	0	Periphal clock/4 (250 ns machine clock, 16MHz)
0	1	1	Periphal clock/8 (500 ns machine clock, 16MHz)
1	0	0	Periphal clock/16 (1 µs machine clock, 16MHz)
1	0	1	Clock input from the time base timer (128 µs, 4MHz)

This bit is initialised to ‘000‘ upon a reset. This bit is readable and writable.

Incorrect time scales and wrong bit definition in table, see correction below:

PCM2	PCM1	PCM0	Operation mode
0	0	0	Periphal clock (62,5 ns machine clock, 16MHz)
0	0	1	Periphal clock/2 (125 ns machine clock, 16MHz)
0	1	0	Periphal clock/4 (250 ns machine clock, 16MHz)
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1	0	1	Clock input from the time base timer (128 µs, 4MHz)

This bit is initialised to ‘000‘ upon a reset. This bit is readable and writable.

Chapter 20.1 Outline of Stepping Motor Controller

Old:

The Stepping Motor Controller consists of two PWM Pulse Generators, four motor drivers and the Selector Logic.
The four motor drivers have high output drive capabilities and they can be directly
connected to the four ends of two motor coils. The combination of the PWM Pulse
Generators and Selector Logic is designed to control the rotation of the motor. A
synchronization mechanism assures the synchronous operations of the two PWMs.
The following sections describe the Stepping Motor Controller 0 only. The other
controllers have the same function. The register addresses are found in the I/O map.

New:

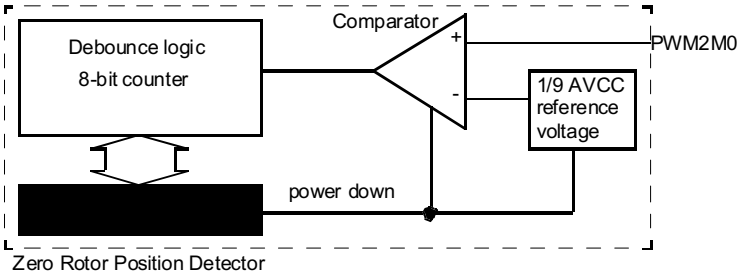
This Chapter provides an overview of the Stepper Motor Control Module, describe the register structure and functions, and described the operation of the Stepper Motor Control Module.

The Stepping Motor Controller consists of two PWM Pulse Generators, four motor drivers, Selector Logic and the Zero Rotor Position Detector. The four motor drivers have high output drive capabilities and they can be directly connected to the four ends of two motor coils. The combination of the PWM Pulse Generators and Selector Logic is designed to control the rotation of the motor. A Synchronization mechanism assures the synchronous operaitons of the two PWMs. The Zero Rotor Position Detector helps CPU obtain feed back information of the rotor movements. The following sections describe the Stepping Motor Controller 0 only. The other controllers have the same functions. The register addresses are found in the I/O map.

<Note> The Rotor Zero Position Detection capability is protected by a patent from Mannesmann VDO and may only be used with VDO’s prior approval.

- Stepping Motor Control Block

Additionally Diagram:



Chapter 20.2 Stepping Motor Control Registers:

Additionally Register ZPDC:

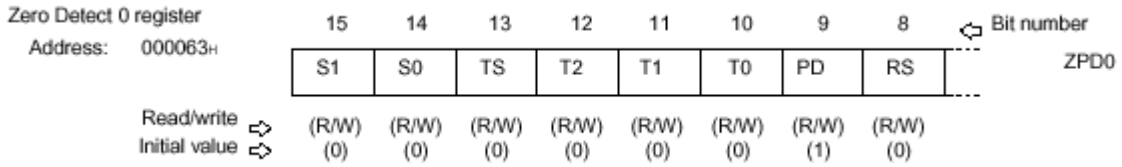
Zero Detect 0 register
Address: 000063H

15	14	13	12	11	10	9	8	⇦ Bit number
S1	S0	TS	T2	T1	T0	PD	RS	ZPD0
(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	⇦ Read/write
(0)	(0)	(0)	(0)	(0)	(0)	(1)	(0)	⇦ Initial value

I/O MAP:

62 H	PWM Control 0	PWC0	R/W	Stepping Motor Controller 0	00000__0
63 H	Zero Detect 0	ZPD0	R/W		00000010
64 H	PWM Control 1	PWC1	R/W	Stepping Motor Controller 1	00000__0
65 H	Zero Detect 1	ZPD1	R/W		00000010
66 H	PWM Control 2	PWC2	R/W	Stepping Motor Controller 2	00000__0
67 H	Zero Detect 2	ZPD2	R/W		00000010
68 H	PWM Control 3	PWC3	R/W	Stepping Motor Controller 3	00000__0
69 H	Zero Detect 3	ZPD3	R/W		00000010

Chapter 20.2.4 Zero Detect Register



[bits 15 to 14] S1 to S0 : Debounce clock select bit

These bits specify the clock frequency used for the Debounce logic. The Debounce logic samples the output of the comparator with the specified clock frequency.

S1	S0	Clock input
0	0	Machine clock
0	1	½ Machine clock
1	0	¼ Machine clock
1	1	1/8 Machine clock

[bits 13] TS : Time slice bit

This bit enables the operation of the Zero Rotor Position Detector. While this bit is "1", the Zero Rotor Position Detector compares the input voltage at the PWM2M0 pin with the reference voltage and sets the RS bit if the input voltage exceed the reference voltage.

[bits 12 to 10] T2 to T0 : Number of samples

These bits specifies the number of samples for the Debounce logic. The Debounce logic samples the output of the comparator the specified number of times. The output of the Debounce logic becomes "1" when all the sampled values are "1"

T2	T1	T0	Number of samples
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	1	1	5

[bits 9] PD : Power down bit

When this bit is set to "1", the power supply to the analog components (comparator and reference voltage source) is switched off.

age source) is switched off.

[bits 8] RS : Result bit

The RS bit indicates whether the input voltage at the PWM2M0 pin exceeded the reference voltage.

The RS bit is set to "1" if the output of the Debounce logic becomes "1". While TS bit is "0", the RS bit always indicates "0".

Power-On Reset

Output "unknown value" , when the power supply Is turned on If F^2MC-16LX is used. (Note)

1.Device covered

MB90V595G, MB90598, MB90F598, MB90F598G

2. Note:

During testing it has been found that some port pins may enter an undefined state during power on. By asserting RSTx during the power on reset (2^{17} cycles of main clock) port pins can be forced to high impedance.

1. The following Ports will output a High Impedance (Hi-z) at the terminal when the power supply is turned on when PONR and RSTX = 1 (RSTx not asserted):

P20 – P45, P50 – P67, P90 – P95

2. The following ports can be forced to high impedance state (Hi-z) during PONR if RSTX is asserted during power on (2^{17} cycles of main clock) or with the End of POMR and the Start of the internal clock

P00 – P03, P16 – P17, P46 – P47, P70 – P87

3. The following Ports will output an High-Z with the End of PONR and the Start of internal clocks. RSTx does not force the pins to High-Z during power on.

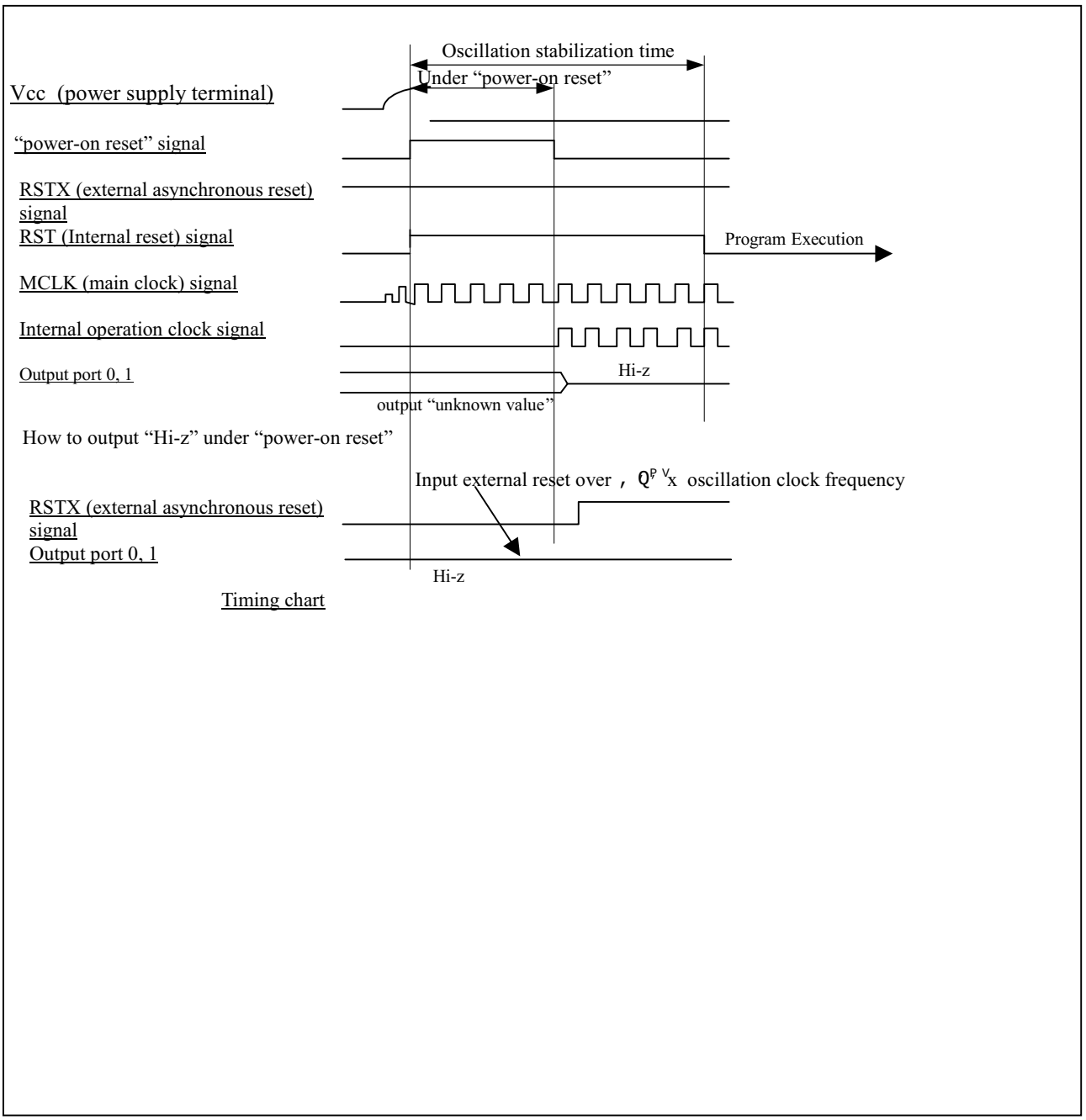
P04 – P15

Note:
This workaround will work for Mode pin setting 011 (Single chip, Internal ROM external bus), 110 (Burn_In ROM), 111 (EPROM mode)

The following diagram shows the timing chart in detail.

See also Datasheet of MB90595/595G series (DS07-13705-2E)

HANDLING DEVICES, (11) Indeterminate outputs from port 0 and 1



Under “power-on reset” •¨ x oscillation clock frequency
(8.192ms in case of oscillation clock frequency = 16MHz)

Waiting time to be stabilized oscillation •¨ x oscillation clock frequency
(16.384ms in case of oscillation clock frequency = 16MHz)