CREMSON-
Subboard
Documentation

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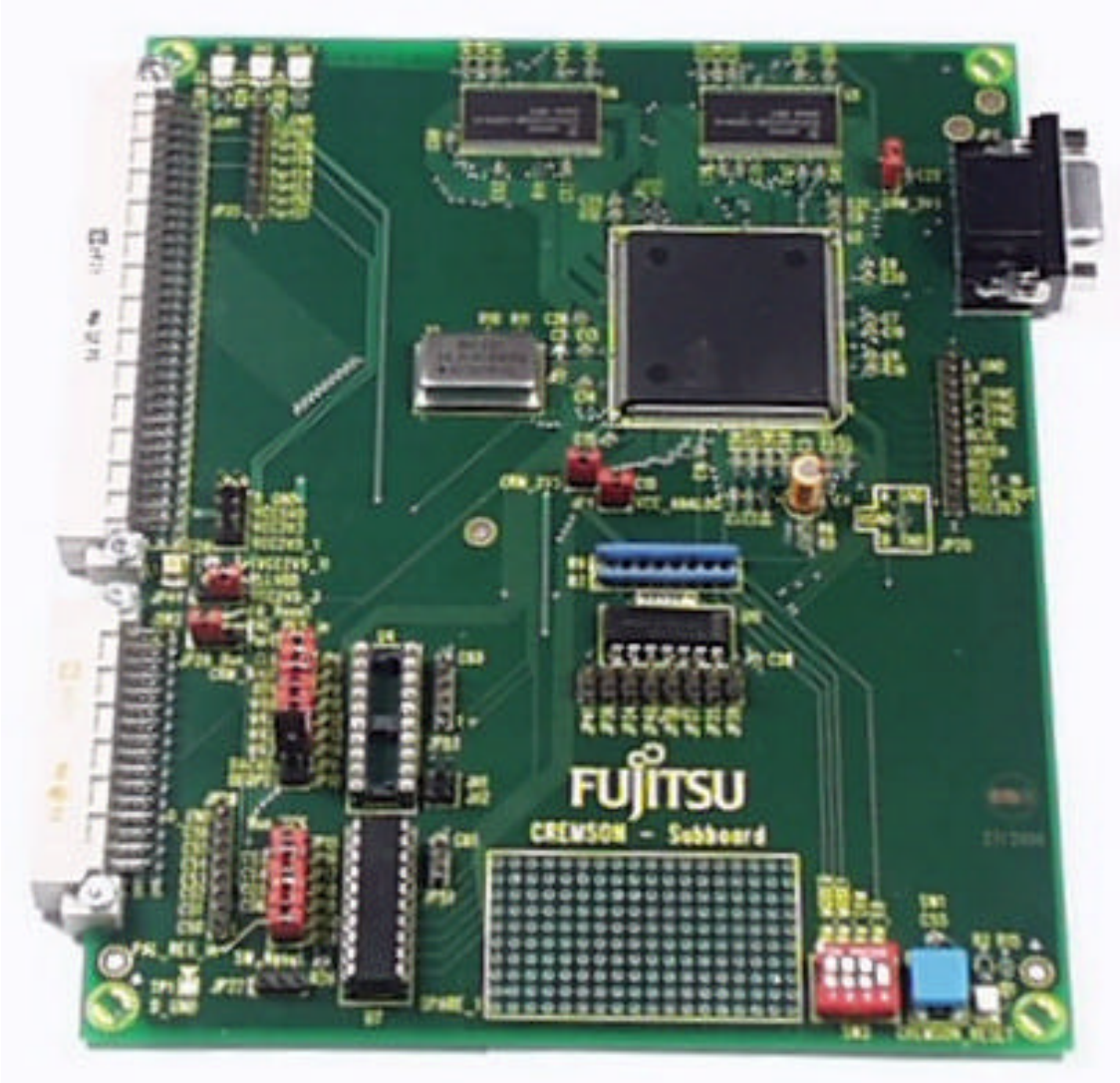

History

Revision	Date	Comment
V1.0	14.03.01	New Document
V1.1	06.06.01	Update (redesign of board)
V1.2	05.07.01	New board plan

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14.03.01 V1.0

1. Introduction

The CREMSON-Subboard is a low cost multifunctional evaluation board for Fujitsu graphic device controller Cremson. It can be used with CREMSON-Starterkit CPU-Modul only for software development and testing as a simple target board.

The board allows the designer immediately to start the software development before his own final target system is available.

2. Features

- Graphic controller Cremson in a package FPT-240P-M03
- 14.318 MHz oscillator
- 2 high-performance 64Mbit SDRAM's designed for demanding multimedia applications (MB81F643242B)
- 2 PALLV16V8
- a 74ALS1034 (six not inverted buffer)
- 3 LEDs for power supply
- Display interface (HD-DSUB-BU-15Pol)
- "CPU-Modul" interface
- Reset button for Cremson

3. Jumpers and Switches

This chapter describes all jumpers and switches which can be modified on the evaluation board. The default setting is shown with a gray shaded area. All jumpers and switches are named directly on the board by its meaning, so it is very easy to set the jumpers according to the features.

3.1 Power Supply Voltage (JP1, JP2, JP4)

	Jumper setting	Description
2V5 power supply (JP1)	ON (closed)	Power supply
	OFF (open)	NO Power supply

	Jumper setting	Description
3V3 power supply (JP2)	ON (closed)	Power supply
	OFF (open)	NO Power supply

	Jumper setting	Description
2V5 power supply (JP4)	ON (closed)	Analog Power supply
	OFF (open)	NO Analog Power supply

NOTE:
The supply voltage for the core and the IO Pins must be set. Otherwise it could happen that the controller does not work correctly!

3.2 Define graphic controller Operating Mode (SW2)

The Cremson can be connected to Fujitsu FR30, Hitachi SH4(SH7750), SH3(SH7709/09A) and NEC V832. The host CPU type is specified by the MODE pins.

	CPU Type	SW2/Mode0	SW2/Mode1
Mode1-0	FR30/SH3	ON	ON
	SH4	OFF	ON
	V832	ONF	OFF
	Reserved	OFF	OFF

	SW2/CKM	Description
Clock mode signal	ON	Output from internal PLL is selected
	OFF	Host CPU bus clock is selected

	SW2/EO	Description
Even/Odd signal mode	ON	Low level output in even frame, High level output in odd frame
	OFF	High level output in even frame, Low level output in odd frame

3.3 Reset Pin (JP29)

The Jumper JP212 determines the Scarlet Reset Pin.
It can be connected directly with the Reset of the VGC, or with a port of the MCU, to execute a software Reset.

	JP29	Description
Reset	1-2	MCU Reset
	2-3	Software Reset (Port S0)

3.4 PLL power supply voltage (JP44)

	JP44	Description
PLL power supply	1-2	PLLVDD connect to core voltage
	2-3	PLLVDD connect to separated voltage

3.5 C-sync for display (JP5)

	JP5	Description
C-sync	ON (closed)	C-sync connected to VGA connector
	OFF (open)	C-sync not connected

3.6 PAL Settings (JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP50, JP24)

	JP6	Description
Bus clock for PALLV16V8	ON (closed)	Needed for internal state machine
	OFF (open)	-

	JP7	Description
Wait request	ON (closed)	Wait request from Scarlet
	OFF (open)	-

	JP8	Description
Read strobe	ON (closed)	Read signal to Scarlet
	OFF (open)	-

	JP11	Description
Write strobe XWE0	ON (closed)	Write signal D0 – D7
	OFF (open)	-

	JP12	Description
Write strobe XWE1	ON (closed)	Write signal D8 – D15
	OFF (open)	-

	JP13	Description
Write strobe XWE2	ON (closed)	Write signal D16 – D23
	OFF (open)	-

	JP14	Description
Write strobe XWE3	ON (closed)	Write strobe D24 – D31
	OFF (open)	-

	JP9	Description
DMA acknowledge	ON (closed)	Not needed for internal logic
	OFF (open)	

	JP10	Description
DMA end operation	ON (closed)	Not needed for internal logic
	OFF (open)	

	JP15	Description
Bus clock for PALLV16V8	ON (closed)	Not needed for internal logic
	OFF (open)	

	JP16	Description
CS3	ON (closed)	CS3 for PAL logic enable
	OFF (open)	CS3 for PAL logic disable

	JP17	Description
CS4	ON (closed)	CS4 for PAL logic enable
	OFF (open)	CS4 for PAL logic disable

	JP18	Description
CS5	ON (closed)	CS5 for PAL logic enable
	OFF (open)	CS5 for PAL logic disable

	JP19	Description
CS6	ON (closed)	CS6 for PAL logic enable
	OFF (open)	CS6 for PAL logic disable

	JP50	Description
PAL Reset	ON (closed)	PAL Reset from MCU
	OFF (open)	-

	JP24	Description
Reset Switch	ON (closed)	Reset from switch SW1
	OFF (open)	-

3.7 Interrupt

	JP21 / JP27	Description
Interrupt enable	ON (closed)	Connected interrupt to MCU
	OFF (open)	Not connected

3.8 DMA

	JP23 / JP26	Description
DREQ0 enable	ON (closed)	Connected DREQ0 to MCU
	OFF (open)	Not connected

3.9 Header for Debug Signals

Analog Output (JP20)

- DCLK_OUT - Dot Clock Signal for Display
- DCLK_IN - Dot Clock Input for External Synchronization
- RED - Analog signal output (RED)
- GREEN - Analog signal output (GREEN)
- BLUE - Analog signal output (BLUE)
- H_SYNC - Horizontal sync signal output
- V_SYNC - Vertical sync signal output
- C_SYNC - Composite sync signal output
- GV - Video/Graphics Switch

Chip Select Signals(JP28)

- CS0-6 - Chip Select from MCU

PWM (JP25)

- PortS7-1 - Free usable Port S (bit 1…7)

Power Supply Voltage (JP49)

- Power supply voltage (2V5, 3V3, 5V0) – GND

Buffer signals (JP34, JP35, JP36, JP37, JP38, JP39, JP40, JP41)

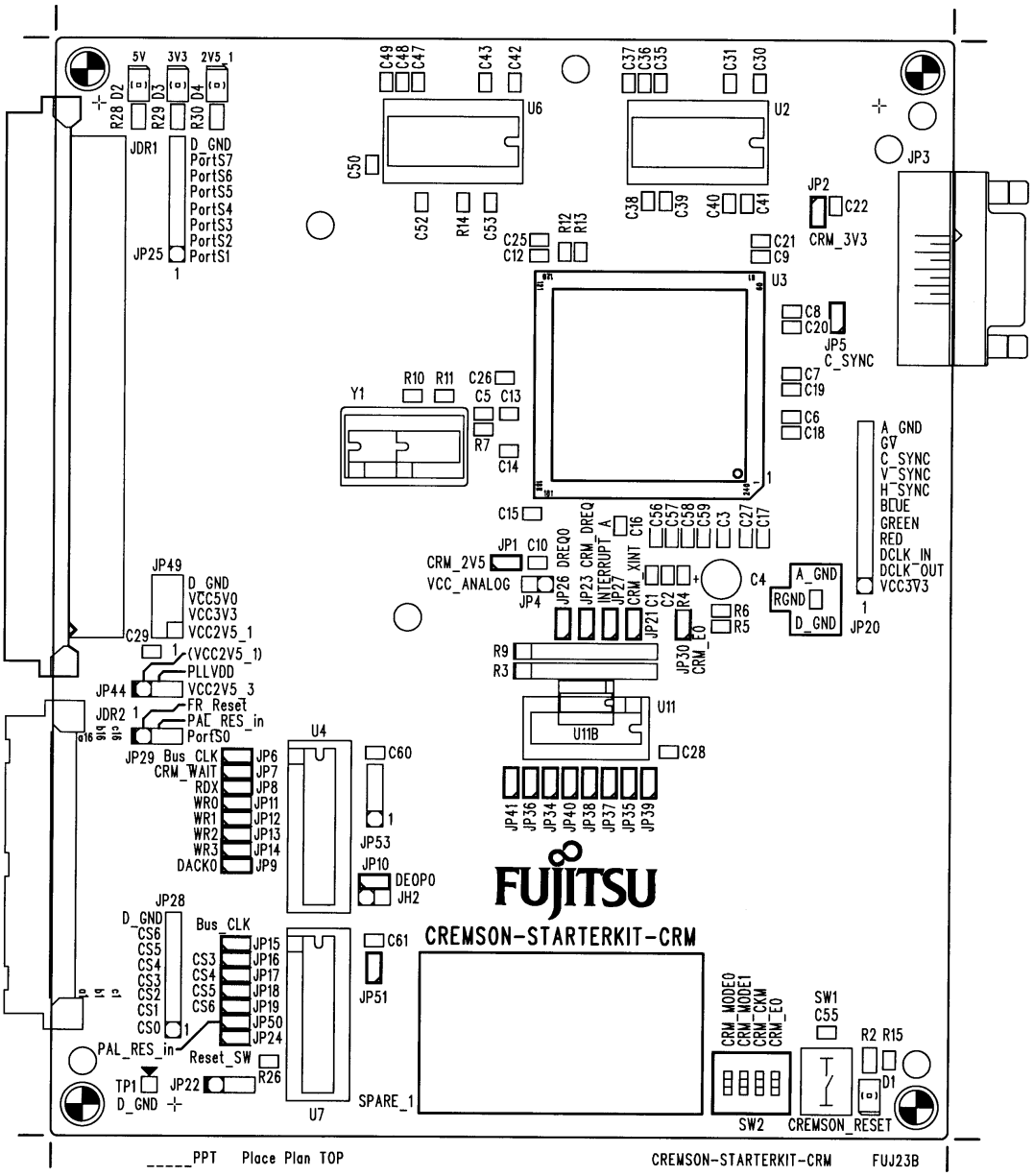
- I/O Pins for 74ALS1034 (six not inverted buffer)

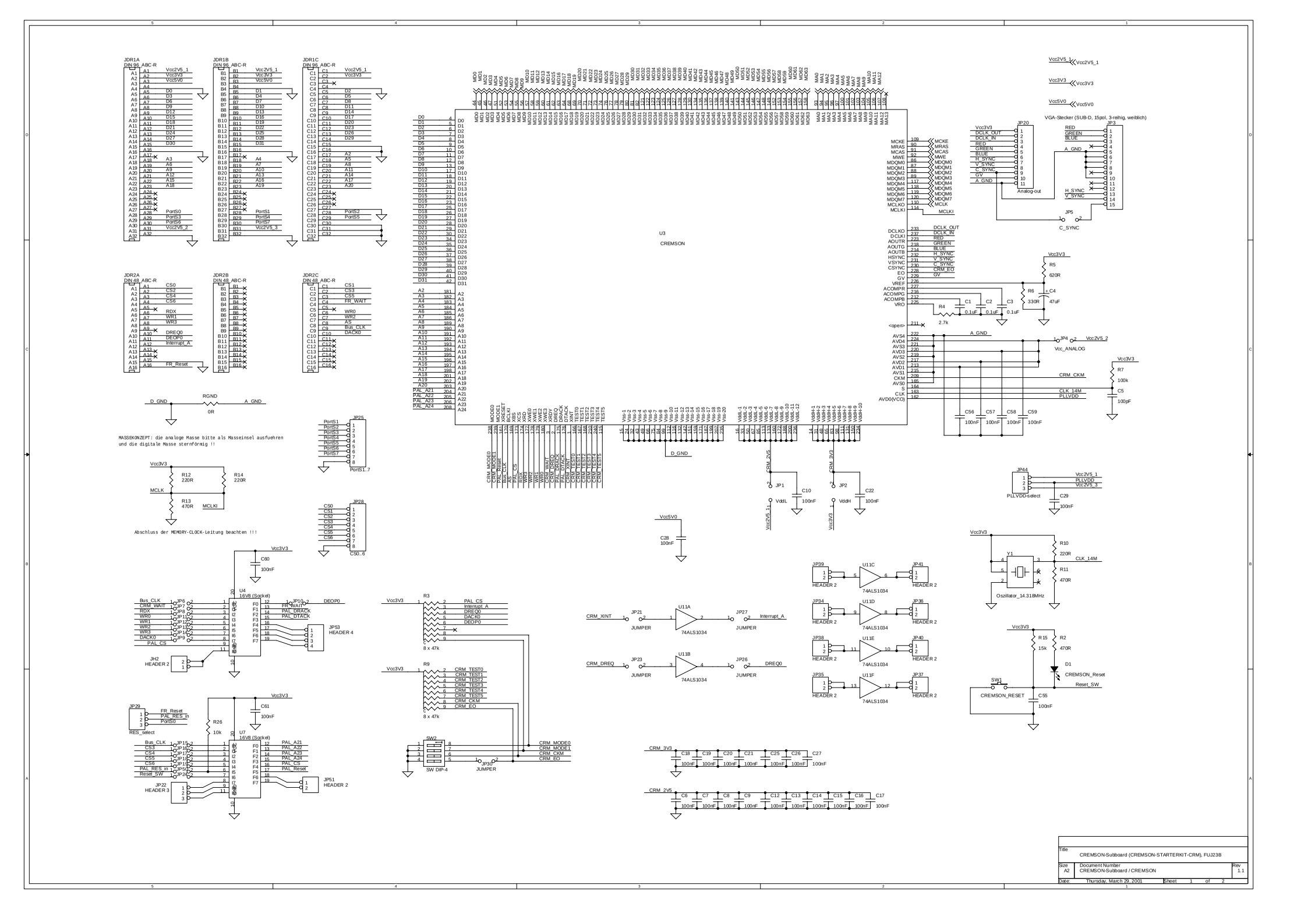
PAL Output Pins (JH1, JH2, JP22, JP51, JP53)

- Not used in internal Logic

For more information please look at the Hardware Manual of the Cremson graphic controller and the Data Sheet of the PALLV16V8.

4. Schematics and Drawings




JDR1A
JDR1B
JDR1C
JDR2A
JDR2B
JDR2C
U3
CREMSON
VGA-Stecker (SUB-D, 15pol, 3-reihig, weiblich)
MASSEKONZEPT: die analoge Masse bitte als Masseinsel ausfuehren und die digitale Masse sternförmig !!
Abschluss der MEMORY-CLOCK-Leitung beachten !!!
U4
16V8 (Socket)
U7
16V8 (Socket)
8 x 47k
SW DIP-4
74ALS1034
HEADER 2
HEADER 3
HEADER 4
JUMPER
Oszillator_14.318MHz
Analog-out
C_SYNC
Vcc_ANALOG
PLLVDD-select
SW1
CREMSON_RESET
Reset_SW
Title
CREMSON-Subboard (CREMSON-STARTERKIT-CRM), FUJ23B
Size
A2
Document Number
CREMSON-Subboard / CREMSON
Rev
1.1
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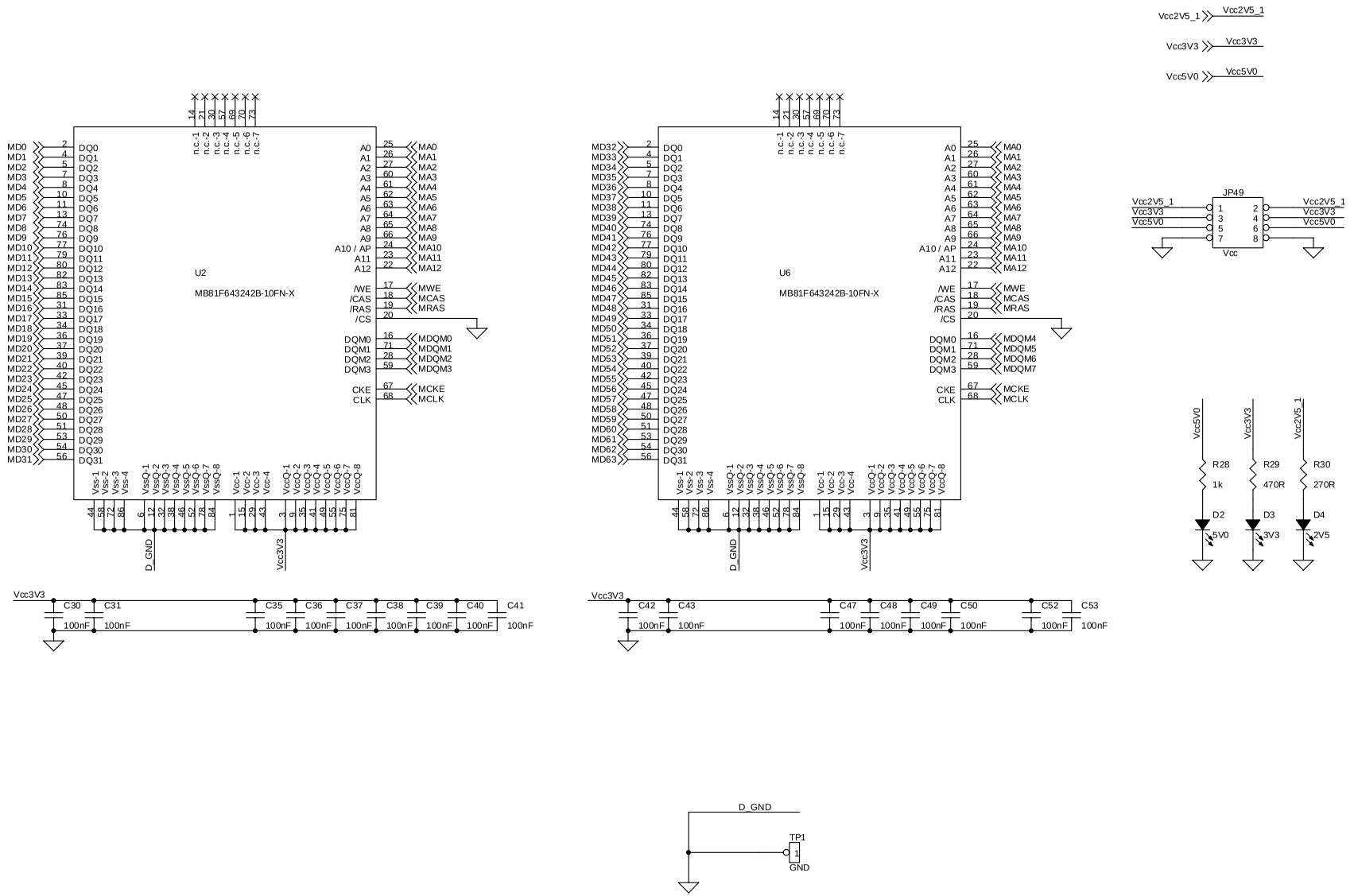

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