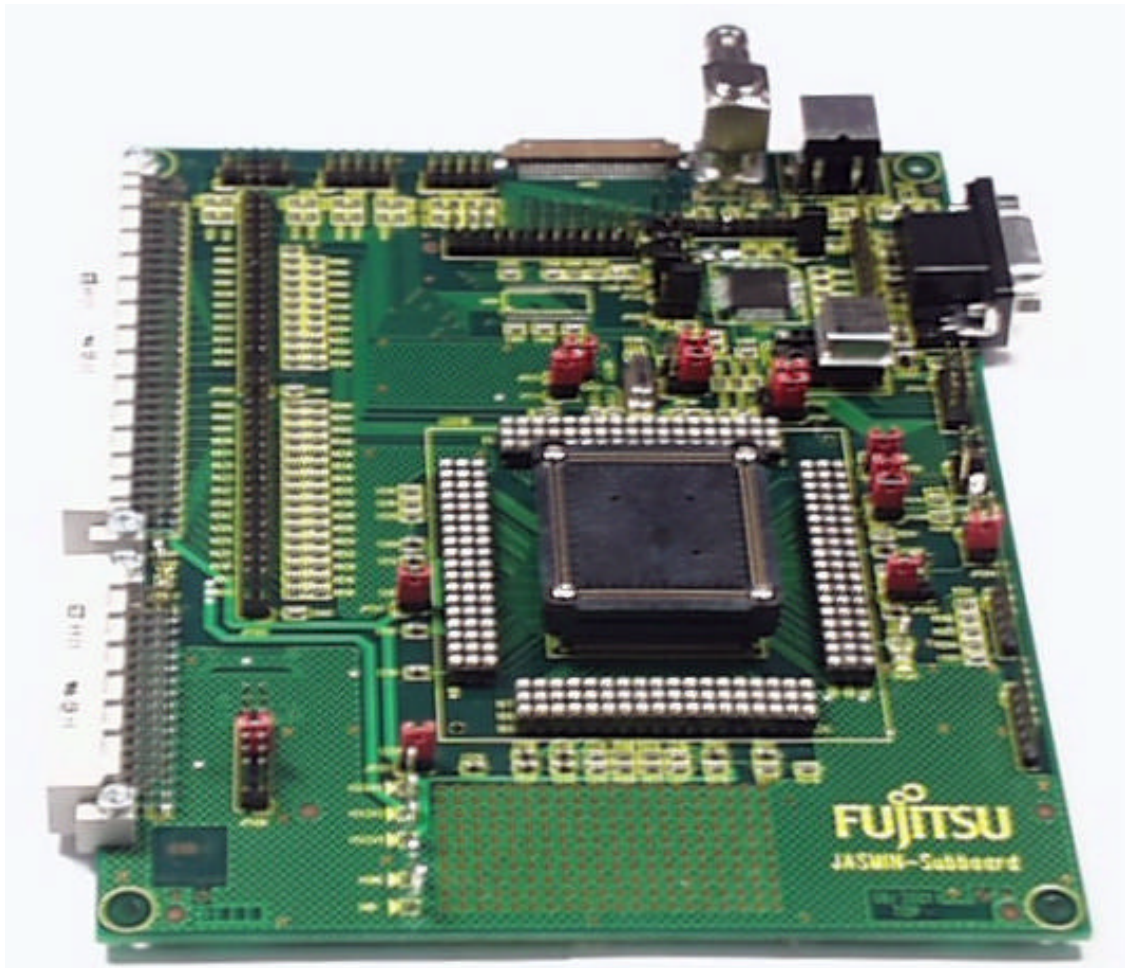


# **JASMINE- Subboard Documentation**

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### History

Revision	Date	Comment
V1.0	07.03.01	New Document

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07.03.01 V1.0

## 1. Introduction

The JASMINE-Subboard is a low cost multifunctional evaluation board for Fujitsu graphic device controller Jasmine. It can be used with CREMSON-Starterkit CPU-Modul only for software development and testing as a simple target board.

The board allows the designer immediately to start the software development before his own final target system is available.

## 2. Features

- Graphic controller Jasmine in a package FPT-208P-M01
- 12 MHz crystal
- Enhanced Video Input Processor (SAA7111A)
- Quarzoszilator for VIC
- Video input connector (BNC-90)
- Display interface (HD-DSUB-BU-15Pol)
- "CPU-Modul" interface

## 3. Jumpers

This chapter describes all jumpers which can be modified on the evaluation board. The default setting is shown with a gray shaded area. All jumpers and switches are named directly on the board by its meaning, so it is very easy to set the jumpers according to the features.

### 3.1 Power Supply Voltage (JP205, JP206, JP207)

	Jumper setting	Description
2V5 power supply (JP205)	ON (closed)	Core supply 2V5
	OFF (open)	NO power supply

	Jumper setting	Description
3V3 power supply (JP206)	ON (closed)	IO supply 3V3
	OFF (open)	NO power supply

	Jumper setting	Description
3V3 power supply (JP207)	ON (closed)	IO supply 3V3
	OFF (open)	NO power supply

#### NOTE:

**The supply voltage for the core and the IO Pins must be set. Otherwise it could happen that the controller does not work correctly!**

### 3.2 Chip Select (JP508)

CS	Jumper setting	Description
CS0	ON (closed 1-2)	ULB-Interface Chip-Select 0
CS1	ON (closed 3-4)	ULB-Interface Chip-Select 1
CS2	ON (closed 5-6)	ULB-Interface Chip-Select 2
CS3	ON (closed 7-8)	ULB-Interface Chip-Select 3
CS4	ON (closed 9-10)	ULB-Interface Chip-Select 4
CS5	ON (closed 11-12)	ULB-Interface Chip-Select 5
CS6	ON (closed 13-14)	ULB-Interface Chip-Select 6

### 3.3 Define graphic controller Operating Mode (JP201, JP202, JP203)

Up to four Jasmine devices can be join one chip select. The size and location of configuration for every Jasmine is fixed. The size is set to 64 kByte for every Jasmine and the location are specified by Mode Jumpers (JP201, JP202).

	Jasmine number	JP202	JP201
Mode1-0	Jasmine 0	2-3	2-3
	Jasmine 1	2-3	1-2
	Jasmine 2	1-2	2-3
	Jasmine 3	1-2	1-2

Jasmine can also act as a 16Bit device from MCU's point of view. The data mode can be set by Jumper JP203.

	JP203	Description
Mode2	1-2	32 Bit data mode
	2-3	16 Bit data mode

It is possible to invert the RDY signal (Mode3 = 1). The RDY signal is not inverted with the application of the CPU-Module (Mode3 = 0).

	JP204	Description
Mode3	5-6	RDY not inverted

### 3.4 Fujitsu Test Pin (JP210)

This pin is usable for internal tests if the chip is in the test mode. In run mode this jumper must be put on GND.

	JP210	Description
Test	1-2	Test mode
	2-3	Run mode

### 3.5 Reset Pin (JP212)

The Jumper JP212 determines the Jasmine Reset Pin.

It can be connected directly with the Reset of the VGC, or with a port of the MCU, to execute a software Reset.

	JP212	Description
Reset	1-2	Software Reset
	2-3	VGC Reset

### 3.6 SPB Interface (JP209, JP215)

	JP209	Description
SPB_BUS	ON (closed)	SPB needs pull-up for operation
	OFF (open)	SPB no operation

	JP215	Description
SPB_TST (clock debug output)	ON (closed)	Probe clock enable
	OFF (open)	Probe clock not enable

### 3.7 RDY (JP213)

Tristate enable for RDY. RDY can be driven with a pull-up if several devices are connected to the bus.

	JP213	Description
RDY Tristate enable	1-2	RDY for several devices
	2-3	RDY for one device

### 3.8 External Clock Input (JP214)

	JP214	Description
Ext. Clock	ON (closed)	NO ext. clock
	OFF (open)	Can used with a pull-up as ext. Clock

### 3.9 Video Input Processor (JP308, JP302, JP301, JP305, JP306, JP307)

	JP308	Description
Power supply voltage	On (closed)	Digital and analog supply voltage for VIC
	OFF (open)	NO power supply

	JP302	Description
VIC enable	1-2	Chip enable connected with VCC
	2-3	Chip enable connected with PortS0-MCU

	JP301	Description
I <sup>2</sup> C-Bus slave address select	GND (closed)	0 = 48h for write, 49h for read
	VCC (open)	1 = 4Ah for write, 4Bh for read

	JP305	Description
Video Scaler Vertical Reference	1-2	HS connected with VREF (GDC)
	2-3	VS connected with VREF (GDC)

	JP306	Description
Video active flag from ext. video decoder	1-2	Video flag from ext. video decoder
	2-3	-

	JP307	Description
Video Scaler Clock	4-6	Video clock output from SAA7111A



### 3.10 Header for Debug Signals

#### CCFL Signals (JP208)

- CCFL\_OFF – CCFL supply control OFF
- CCFL\_IGNIT – CCFL supply control IGNITION
- CCFL\_FET2 – CCFL FET driver2
- CCFL\_FET1 – CCFL FET driver1

#### I<sup>2</sup>C Signals from SAA7111A (JP211)

- I<sup>2</sup>C\_SCL – Serial clock line
- I<sup>2</sup>C\_SDA – Serial data line
- RES-out – Reset output (active low)

#### SAA7111A Signals (JP304)

- RTC0 – Real time control output
- VSC\_IDENT – Video scaler field identification
- ALPHA – Video scaler ALPHA
- V<sub>ref</sub> – Vertical reference output signal
- H<sub>ref</sub> – Horizontal reference output signal
- C<sub>ref</sub> – Clock reference output
- HS – Horizontal sync output signal
- VS – Vertical sync output signal
- GPSW – General purpose switch output
- RES-out – Reset output (active low)

#### VIC Signals (JP401)

- BUS\_VCS\_D7-0 – Video scaler data input
- VSC\_CLKV – Video scaler clock

#### LVDS connector (JP402)

Signals for LVDS connector

#### Display Signals (JP501)

- DIS\_PIXCLK – Display pixel clock
- A\_RED – Analog red
- A\_GREEN – Analog green
- A\_BLUE – Analog blue
- DIS\_HSYNC – Horizontal sync signal
- DIS\_VSYNC – Vertical sync signal
- DIS\_VREF – Display vertical reference signal
- DIS\_CK – Display clock

#### Display Digital Signals (JP502, JP503, JP504)

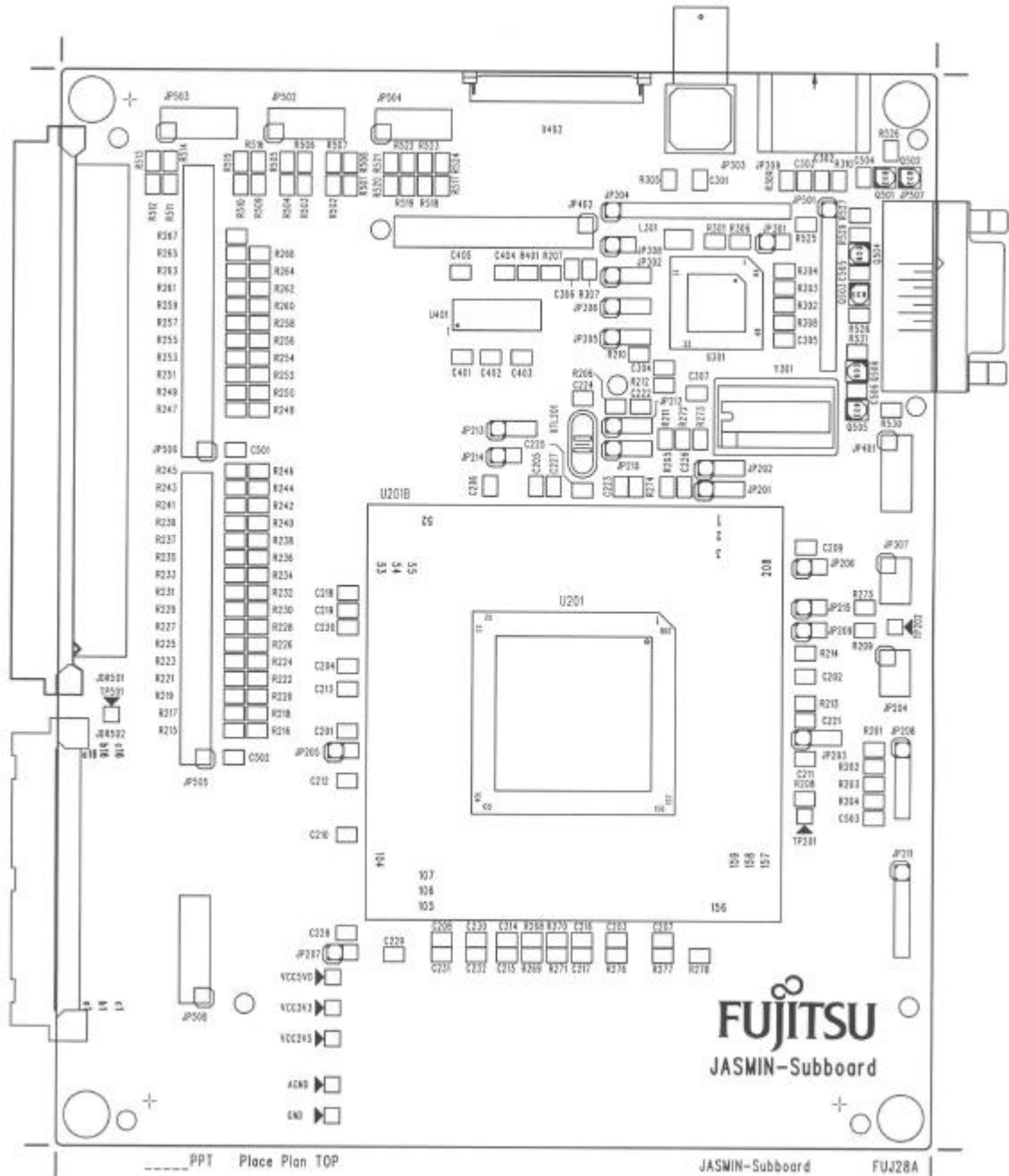
- BUS\_DIS\_D7-0 – Digital display data
- BUS\_DIS\_D15-8 – Digital display data
- BUS\_DIS\_D23-16 – Digital display data

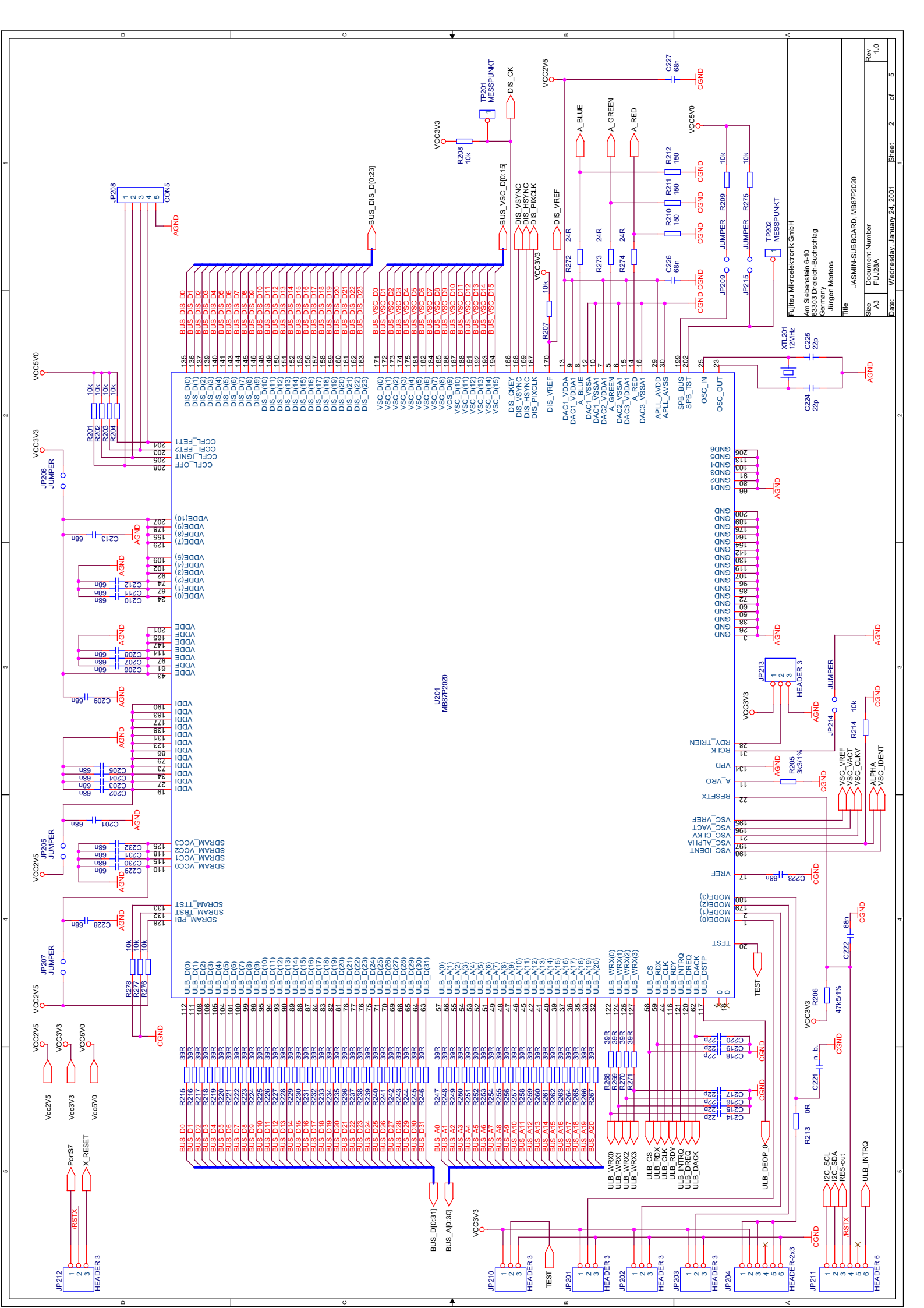
### **ULB Signals (JP505, JP506)**

- BUS\_D31-0 - ULB interface data bus
- BUS\_A20-0 - ULB interface address bus
- ULB\_INTRQ - ULB interrupt request
- ULB\_RDY - Ready signal for bus transfer
- ULB\_RDX - Read enable for ULB data bus
- ULB\_WRX3-0 - Write enable for ULB data bus
- ULB\_CLK - ULB interface clock
- ULB\_CS - Chip select
- ULB\_DREQ - DMA request signal
- ULB\_DACK - DMA acknowledge signal

For more information please look at the Hardware Manual of the Jasmine graphic controller and the Data Sheet of the Video Input Processor SAA7111A.

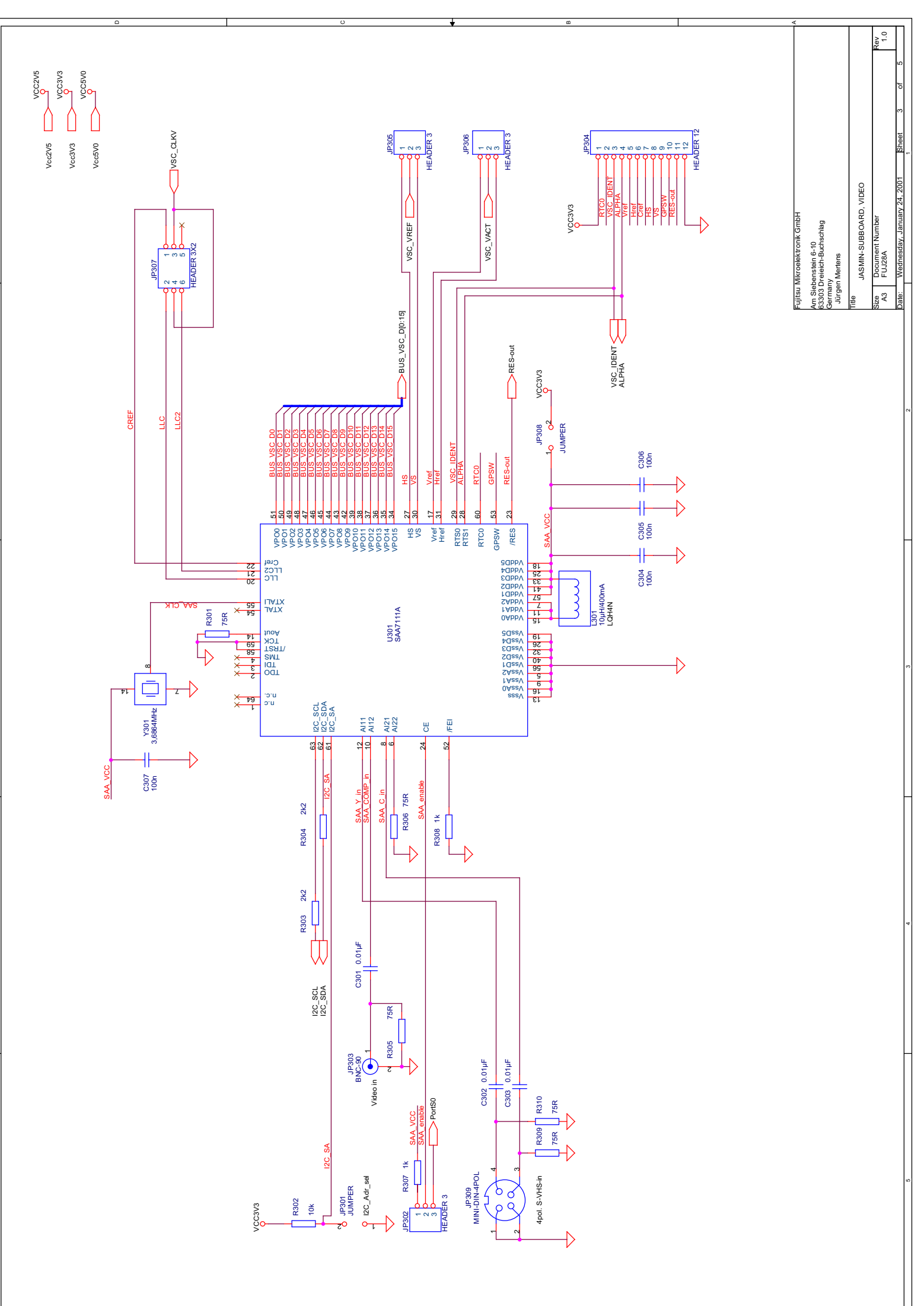
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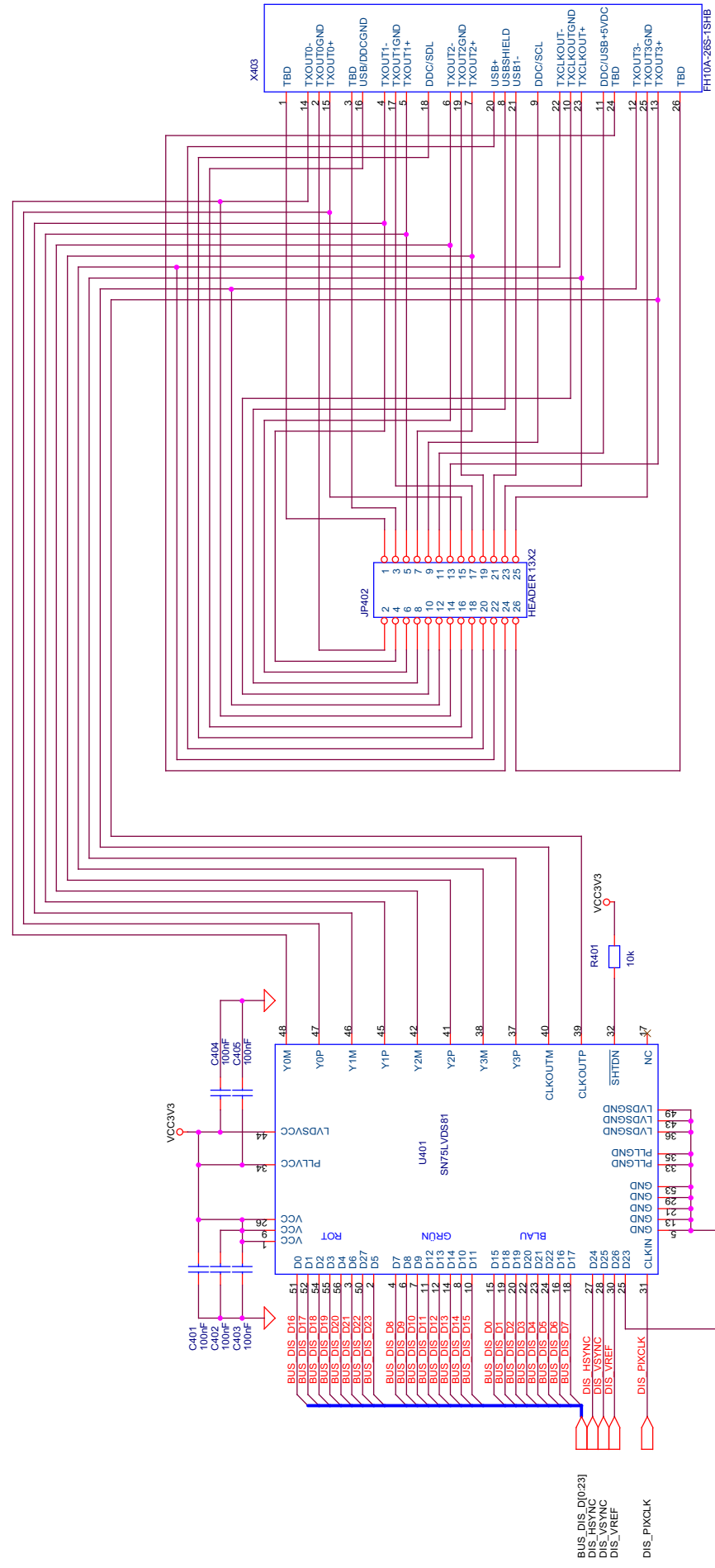
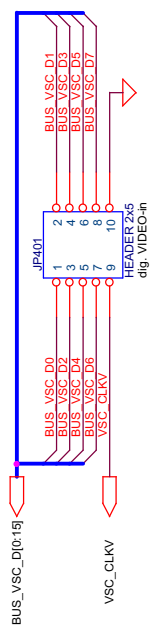
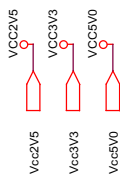




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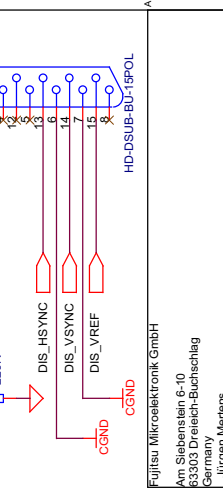
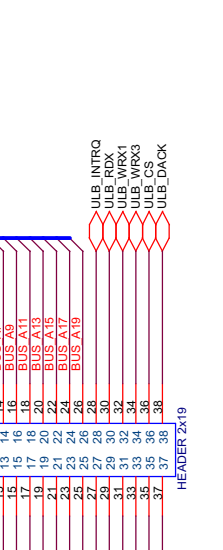
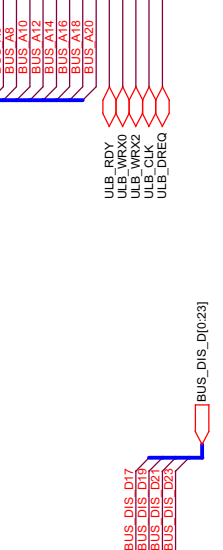
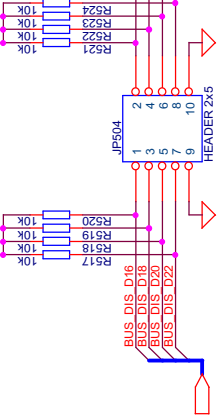
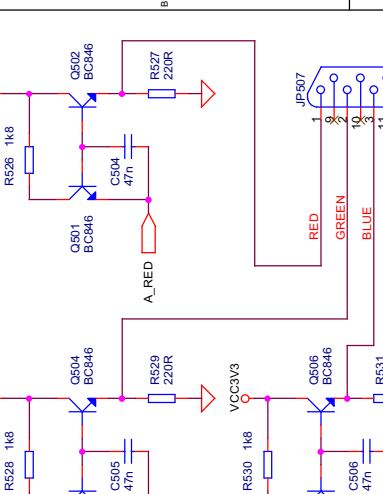
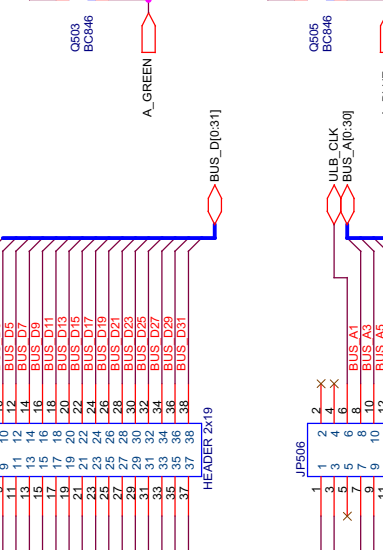
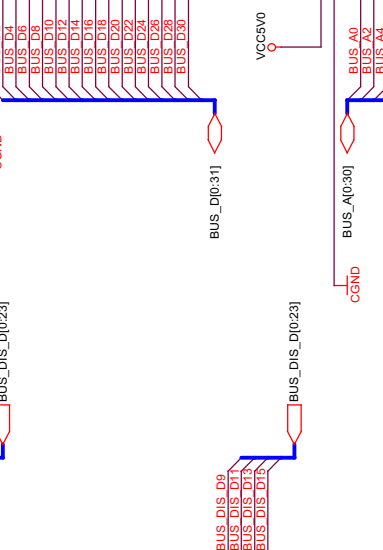
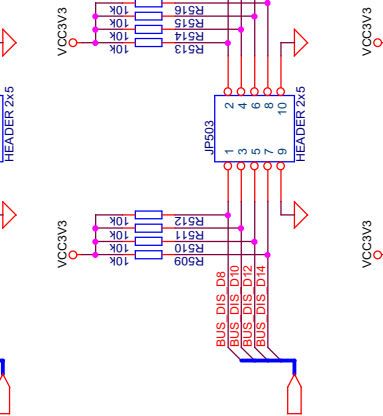
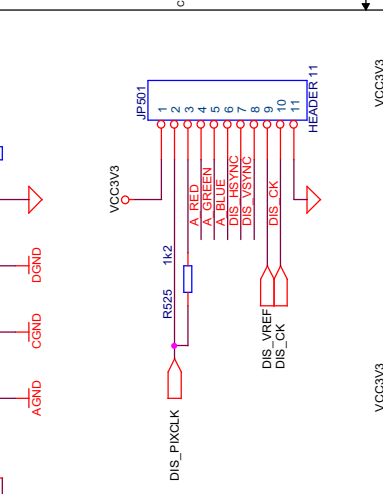
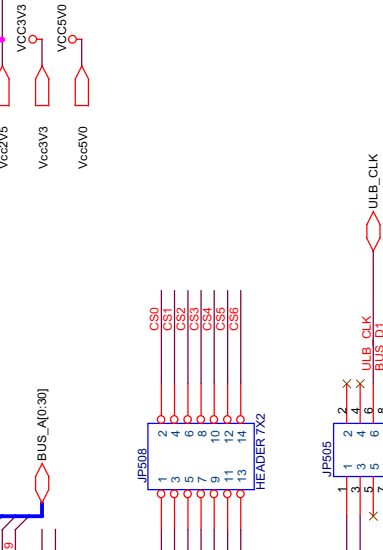
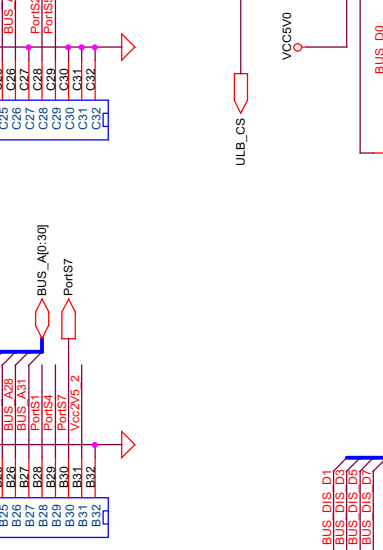
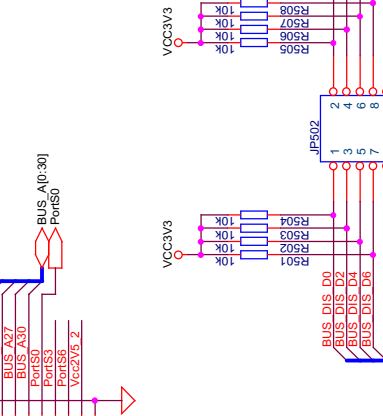
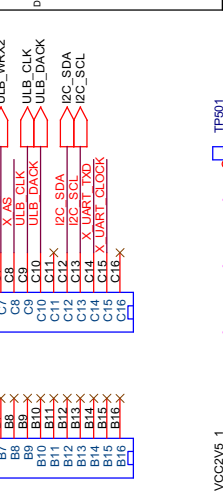
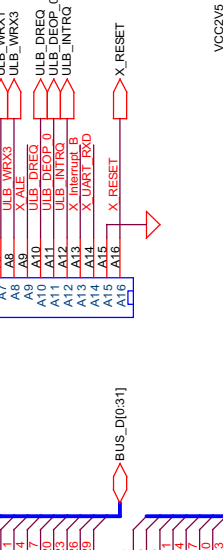
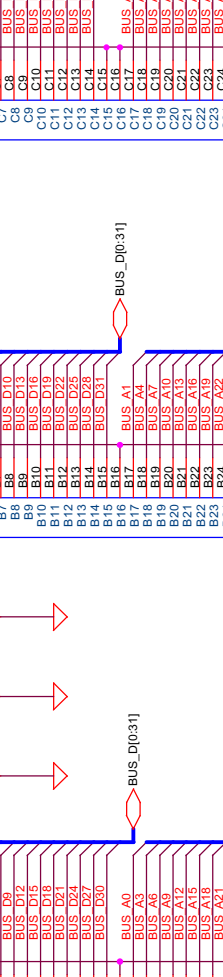
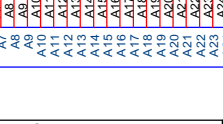
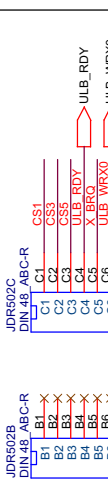
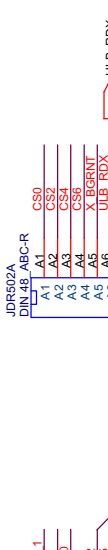
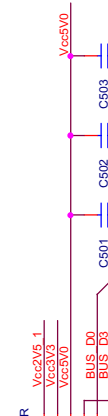
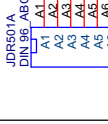
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