LAVENDER-
Subboard
Documentation

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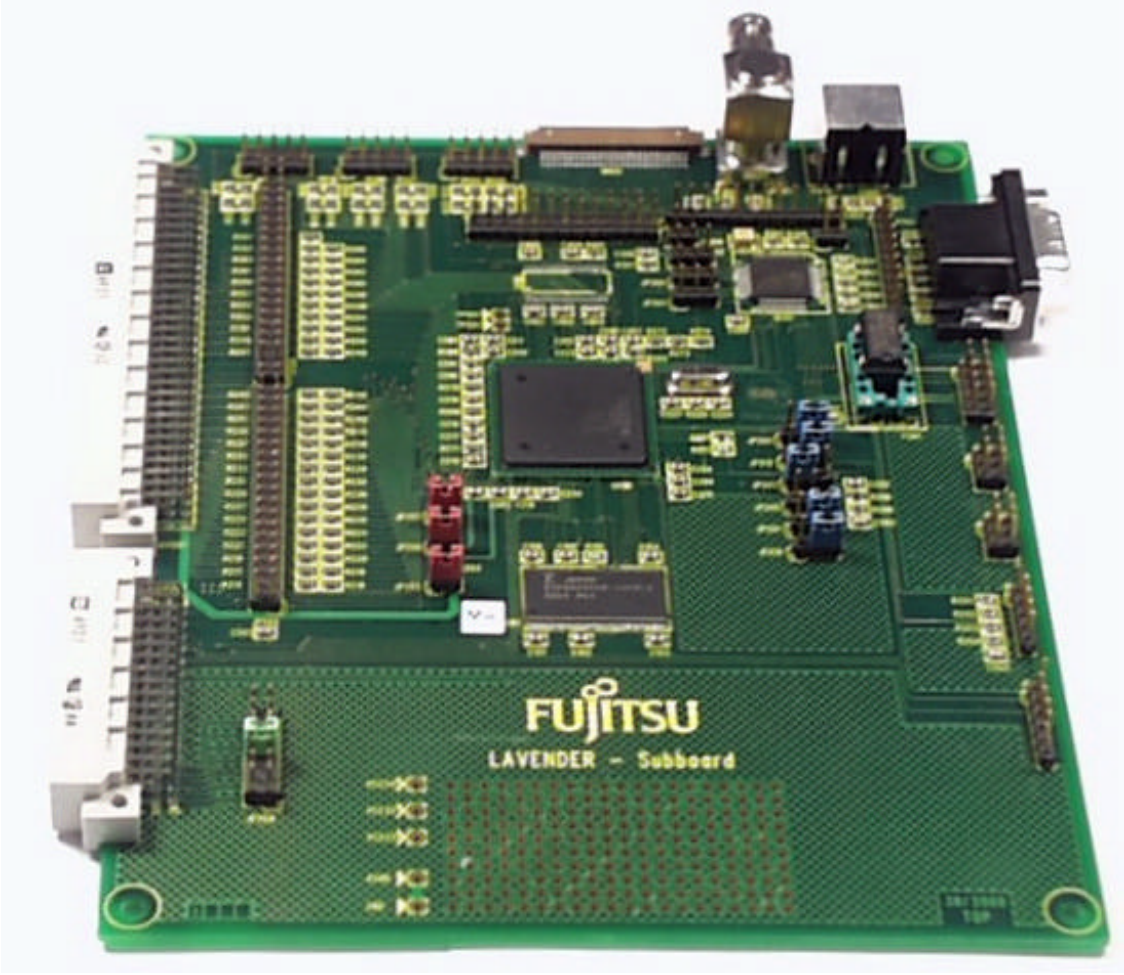

History

Revision	Date	Comment
V1.0	06.03.01	New Document

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06.03.01 V1.0

1. Introduction

The LAVENDER-Subboard is a low cost multifunctional evaluation board for Fujitsu graphic device controller Lavender. It can be used with CREMSON-Starterkit CPU-Modul only for software development and testing as a simple target board.

The board allows the designer immediately to start the software development before his own final target system is available.

2. Features

- Graphic controller Lavender in a package BGA-256P-M01
- 12 MHz crystal
- a high-performance 64Mbit SDRAM designed for demanding multimedia applications (MB81F643242B)
- Enhanced Video Input Processor (SAA7111A)
- Video input connector (BNC-90)
- Crystal oscillator for VIC
- Display interface (HD-DSUB-BU-15Pol)
- “CPU-Modul” interface

3. Jumpers

This chapter describes all jumpers which can be modified on the evaluation board. The default setting is shown with a gray shaded area. All jumpers and switches are named directly on the board by its meaning, so it is very easy to set the jumpers according to the features.

3.1 Power Supply Voltage (JP205, JP206, JP207)

	Jumper setting	Description
2V5 power supply (JP205)	ON (closed)	Core supply 2V5
	OFF (open)	NO power supply

	Jumper setting	Description
3V3 power supply (JP206)	ON (closed)	IO supply 3V3
	OFF (open)	NO power supply

	Jumper setting	Description
3V3 power supply (JP207)	ON (closed)	IO supply 3V3
	OFF (open)	NO power supply

NOTE: The supply voltage for the core and the IO Pins must be set. Otherwise it could happen that the controller does not work correctly!

3.2 Chip Select (JP508)

CS	Jumper setting	Description
CS0	ON (closed 1-2)	ULB-Interface Chip-Select 0
CS1	ON (closed 3-4)	ULB-Interface Chip-Select 1
CS2	ON (closed 5-6)	ULB-Interface Chip-Select 2
CS3	ON (closed 7-8)	ULB-Interface Chip-Select 3
CS4	ON (closed 9-10)	ULB-Interface Chip-Select 4
CS5	ON (closed 11-12)	ULB-Interface Chip-Select 5
CS6	ON (closed 13-14)	ULB-Interface Chip-Select 6

3.3 Define graphic controller Operating Mode (JP201, JP202, JP203, JP204)

Up to four Lavender devices can be join one chip select. The size and location of configuration for every Lavender is fixed. The size is set to 64 kByte for every Lavender and the location are specified by Mode Jumpers (JP201, JP202).

	Lavender number	JP202	JP201
Mode1-0	Lavender 0	2-3	2-3
	Lavender 1	2-3	1-2
	Lavender 2	1-2	2-3
	Lavender 3	1-2	1-2

Lavender can also act as a 16Bit device from MCU’s point of view. The data mode can be set by Jumper JP203.

	JP203	Description
Mode2	1-2	32 Bit data mode
	2-3	16 Bit data mode

It is possible to invert the RDY signal (Mode3 = 1). The RDY signal is not inverted with the application of the CPU-Module (Mode3 = 0).

	JP204	Description
Mode3	5-6	RDY not inverted

3.4 Fujitsu Test Pin (JP210)

This pin is usable for internal tests if the chip is in the test mode. In run mode this jumper must be put on GND.

	JP210	Description
Test	1-2	Test mode
	2-3	Run mode

3.5 Reset Pin (JP212)

The Jumper JP212 determines the Lavender Reset Pin.
It can be connected directly with the Reset of the VGC, or with a port of the MCU, to execute a software Reset.

	JP212	Description
Reset	1-2	Software Reset
	2-3	VGC Reset

3.6 Video Input Processor (JP308, JP302, JP301, JP305, JP306, JP307)

	JP308	Description
Power supply voltage	On (closed)	Digital and analog supply voltage for VIC
	OFF (open)	NO power supply

	JP302	Description
VIC enable	1-2	Chip enable connected with VCC
	2-3	Chip enable connected with PortS0-MCU

	JP301	Description
I^2C-Bus slave address select	GND (closed)	0 = 48h for write, 49h for read
	VCC (open)	1 = 4Ah for write, 4Bh for read

	JP305	Description
Video Scaler Vertical Reference	1-2	HS connected with VREF (GDC)
	2-3	VS connected with VREF (GDC)

	JP306	Description
Video active flag from ext. video decoder	1-2	Video flag from ext. video decoder
	2-3	-

	JP307	Description
Video Scaler Clock	4-6	Video clock output from SAA7111A

3.7 SBP Bus

	JP209	Description
SPB_BUS	ON (closed)	SPB needs pull-up for operation
	OFF (open)	SPB no operation

3.8 Header for Debug Signals

CCFL Signals (JP208)

- CCFL_OFF – CCFL supply control OFF
- CCFL_IGNIT – CCFL supply control IGNITION
- CCFL_FET2 – CCFL FET driver2
- CCFL_FET1 – CCFL FET driver1

I^2C Signals from SAA7111A (JP211)

- I^2C_SCL - Serial clock line
- I^2C_SDA - Serial data line
- RES-out - Reset output (active low)

SAA7111A Signals (JP304)

- RTC0 - Real time control output
- VSC_IDENT - Video scaler field identification
- ALPHA - Video scaler ALPHA
- V_{ref} - Vertical reference output signal
- H_{ref} - Horizontal reference output signal
- C_{ref} - Clock reference output
- HS - Horizontal sync output signal
- VS - Vertical sync output signal
- GPSW - General purpose switch output
- RES-out - Reset output (active low)

VIC Signals (JP401)

- BUS_VCS_D7-0 - Video scaler data input
- VSC_CLKV - Video scaler clock

LVDS connector (JP402)

Signals for LVDS connector

Display Signals (JP501)

- DIS_PIXCLK - Display pixel clock
- A_RED - Analog red
- A_GREEN - Analog green
- A_BLUE - Analog blue
- DIS_HSYNC - Horizontal sync signal
- DIS_VSYNC - Vertical sync signal
- DIS_VREF - Display vertical reference signal
- DIS_CK - Display clock

Display Digital Signals (JP502, JP503, JP504)

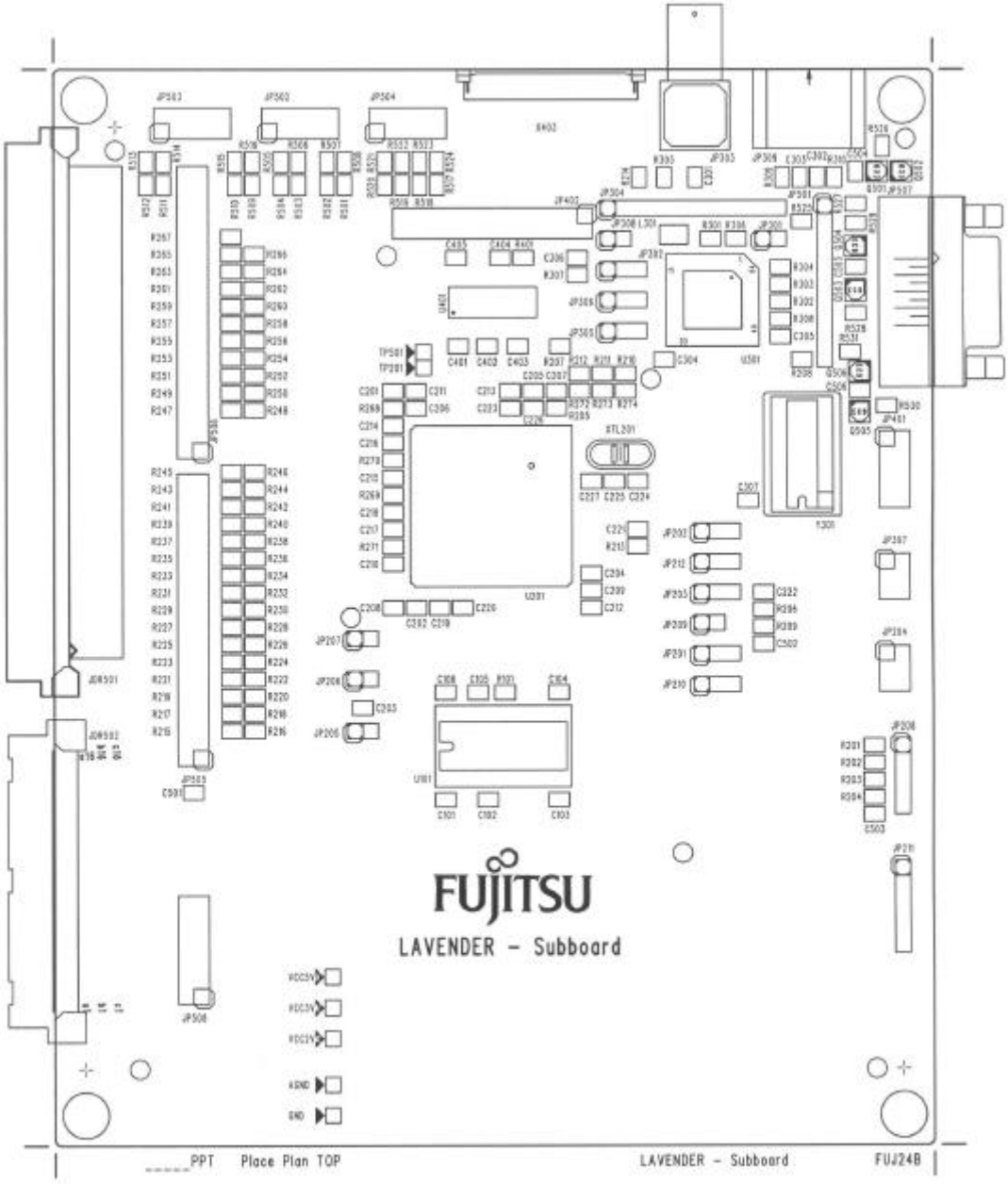
- BUS_DIS_D7-0 - Digital display data
- BUS_DIS_D15-8 - Digital display data
- BUS_DIS_D23-16- Digital display data

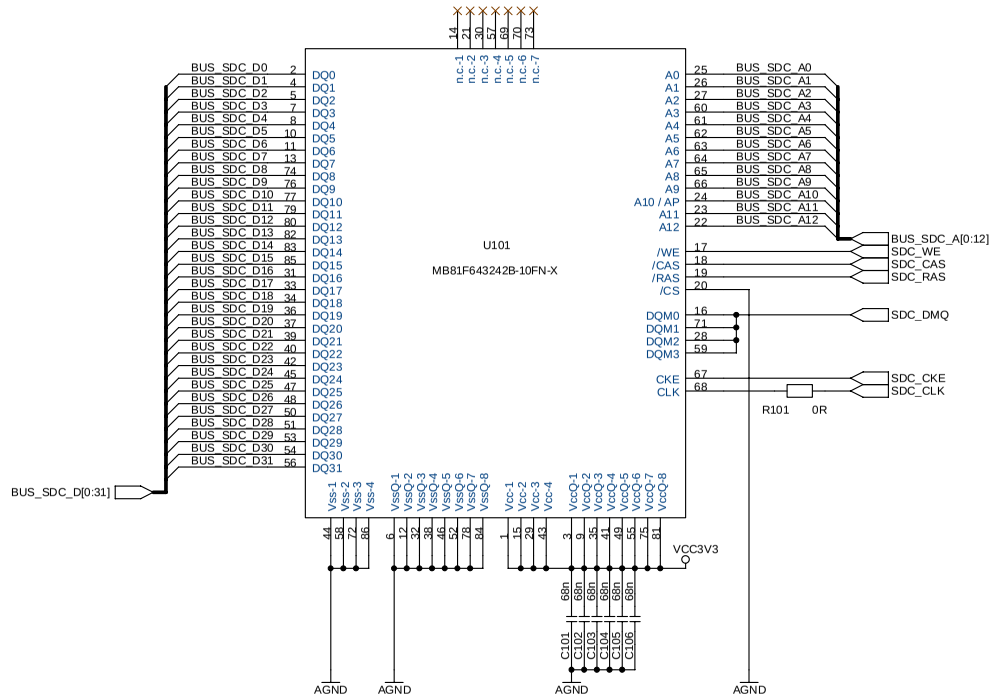
ULB Signals (JP505, JP506)

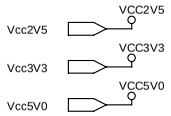
- BUS_D31-0 - ULB interface data bus
- BUS_A20-0 - ULB interface address bus
- ULB_INTRQ - ULB interrupt request
- ULB_ RDY - Ready signal for bus transfer
- ULB_RDX - Read enable for ULB data bus
- ULB_WRX3-0 - Write enable for ULB data bus
- ULB_CLK - ULB interface clock
- ULB_CS - Chip select
- ULB_DREQ - DMA request signal
- ULB_DACK - DMA acknowledge signal

For more information please look at the Hardware Manual of the Lavender graphic controller and the Data Sheet of the Video Input Processor SAA7111A.

4. Schematics and Drawings







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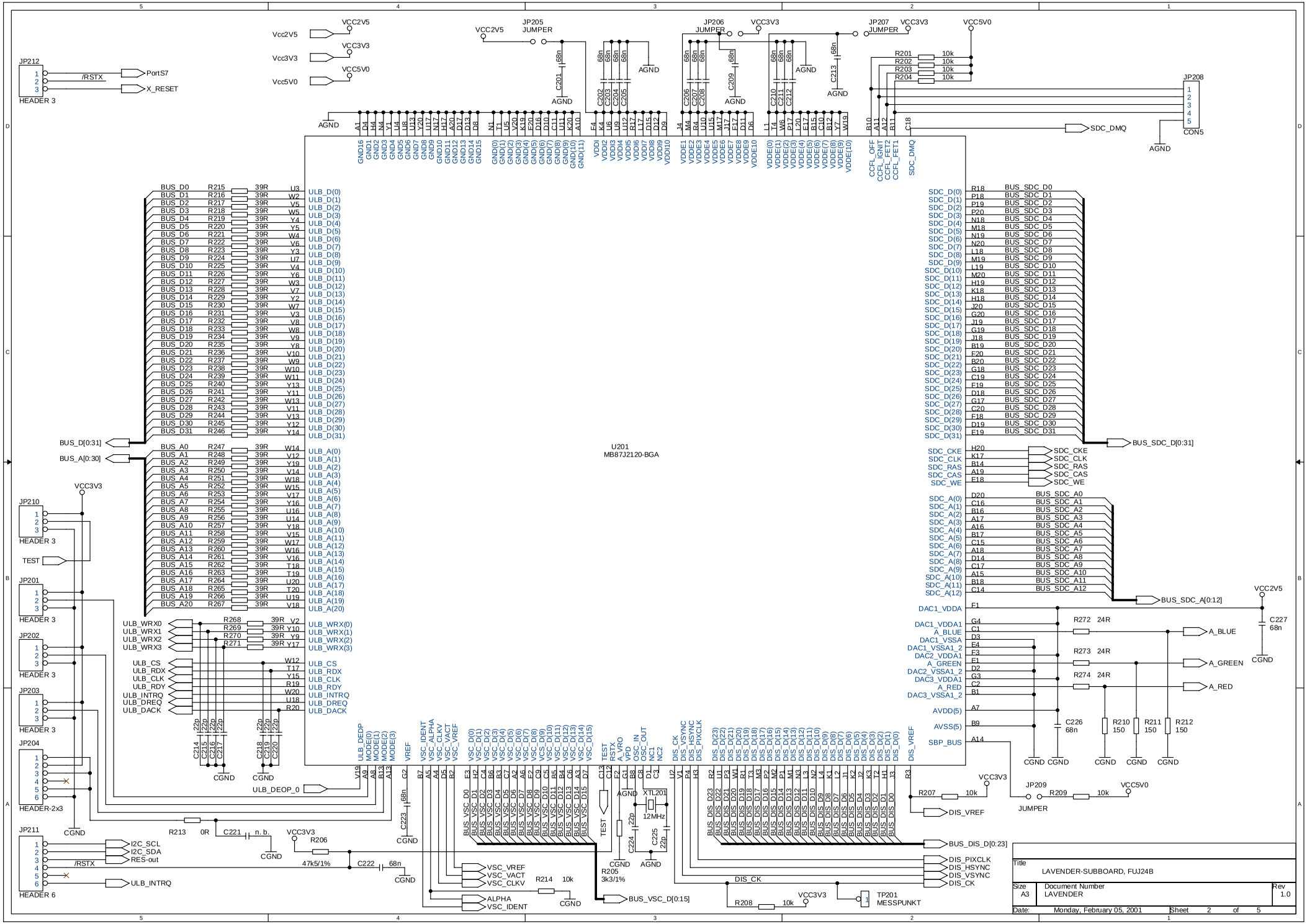
JP212
HEADER 3
/RSTX
PortS7
X_RESET
Vcc2V5
Vcc3V3
Vcc5V0
VCC2V5
VCC3V3
VCC5V0
JP205
JUMPER
JP206
JUMPER
JP207
JUMPER
C201
C209
C213
68n
AGND
R201
R202
R203
R204
10k
JP208
CON5
SDC_DMQ
U201
MB87J2120-BGA
BUS_D[0:31]
BUS_A[0:30]
ULB_D(0)
ULB_D(1)
ULB_D(2)
ULB_D(3)
ULB_D(4)
ULB_D(5)
ULB_D(6)
ULB_D(7)
ULB_D(8)
ULB_D(9)
ULB_D(10)
ULB_D(11)
ULB_D(12)
ULB_D(13)
ULB_D(14)
ULB_D(15)
ULB_D(16)
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ULB_D(26)
ULB_D(27)
ULB_D(28)
ULB_D(29)
ULB_D(30)
ULB_D(31)
ULB_A(0)
ULB_A(1)
ULB_A(2)
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ULB_A(13)
ULB_A(14)
ULB_A(15)
ULB_A(16)
ULB_A(17)
ULB_A(18)
ULB_A(19)
ULB_A(20)
ULB_WRX(0)
ULB_WRX(1)
ULB_WRX(2)
ULB_WRX(3)
ULB_CS
ULB_RDX
ULB_CLK
ULB_RDY
ULB_INTRQ
ULB_DREQ
ULB_DACK
ULB_DEOP_0
BUS_SDC_D[0:31]
BUS_SDC_A[0:12]
SDC_CKE
SDC_CLK
SDC_RAS
SDC_CAS
SDC_WE
DAC1_VDDA
A_BLUE
A_GREEN
A_RED
AVDD(5)
AVSS(5)
SBP_BUS
C227
68n
R272 24R
R273 24R
R274 24R
R210 150
R211 150
R212 150
C226
68n
CGND
JP209
JUMPER
R207 10k
DIS_VREF
R209 10k
JP210
HEADER 3
TEST
JP201
HEADER 3
JP202
HEADER 3
JP203
HEADER 3
JP204
HEADER-2x3
JP211
HEADER 6
I2C_SCL
I2C_SDA
RES-out
/RSTX
ULB_INTRQ
R213 0R
C221 n. b.
R206 47k5/1%
C222 68n
R214 10k
R205 3k3/1%
XTL201
12MHz
C223 68n
C224 22p
C225 22p
VSC_VREF
VSC_VACT
VSC_CLKV
ALPHA
VSC_IDENT
BUS_VSC_D[0:15]
BUS_DIS_D[0:23]
DIS_PIXCLK
DIS_HSYNC
DIS_VSYNC
DIS_CK
R208 10k
TP201
MESSPUNKT
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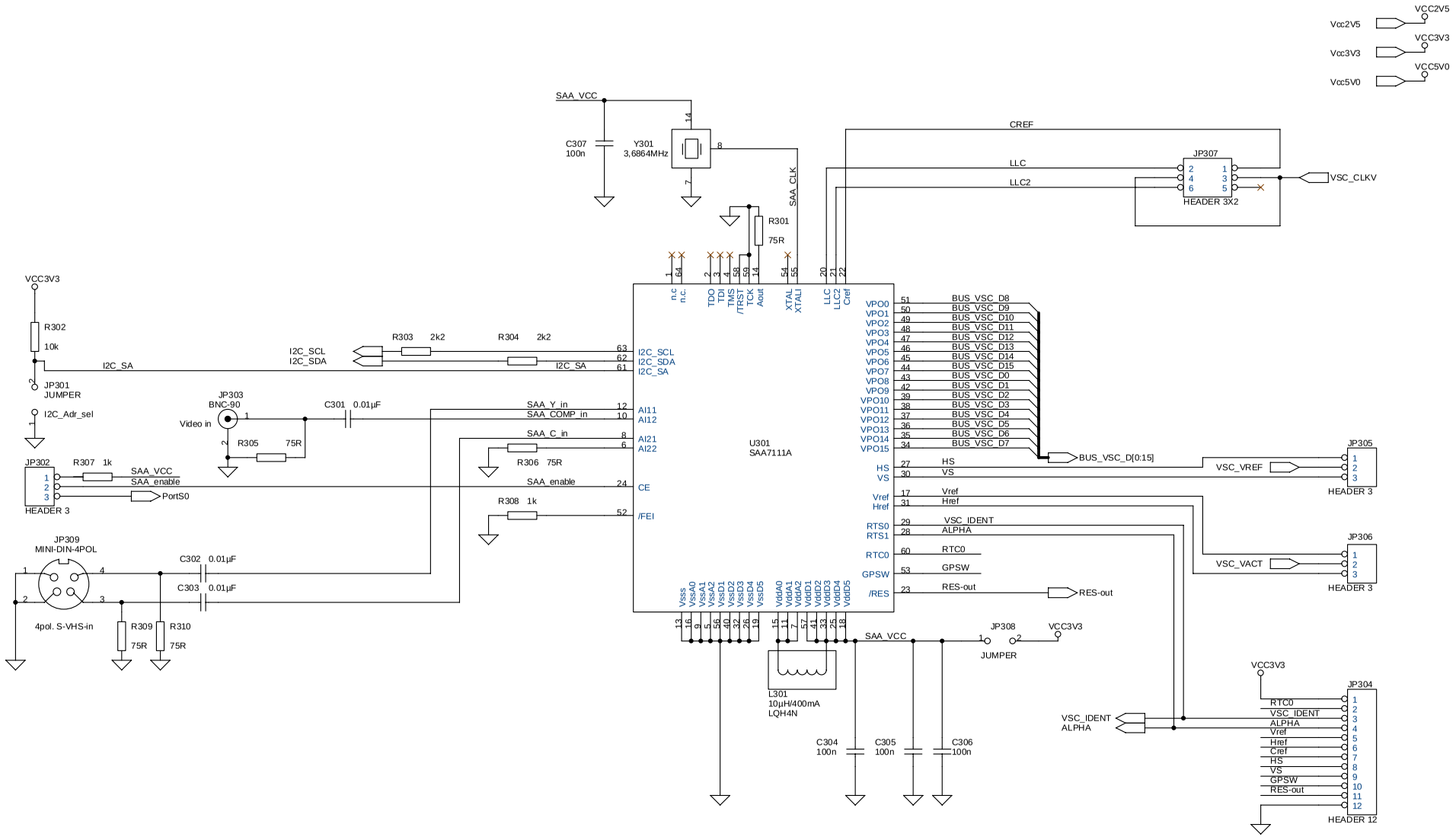

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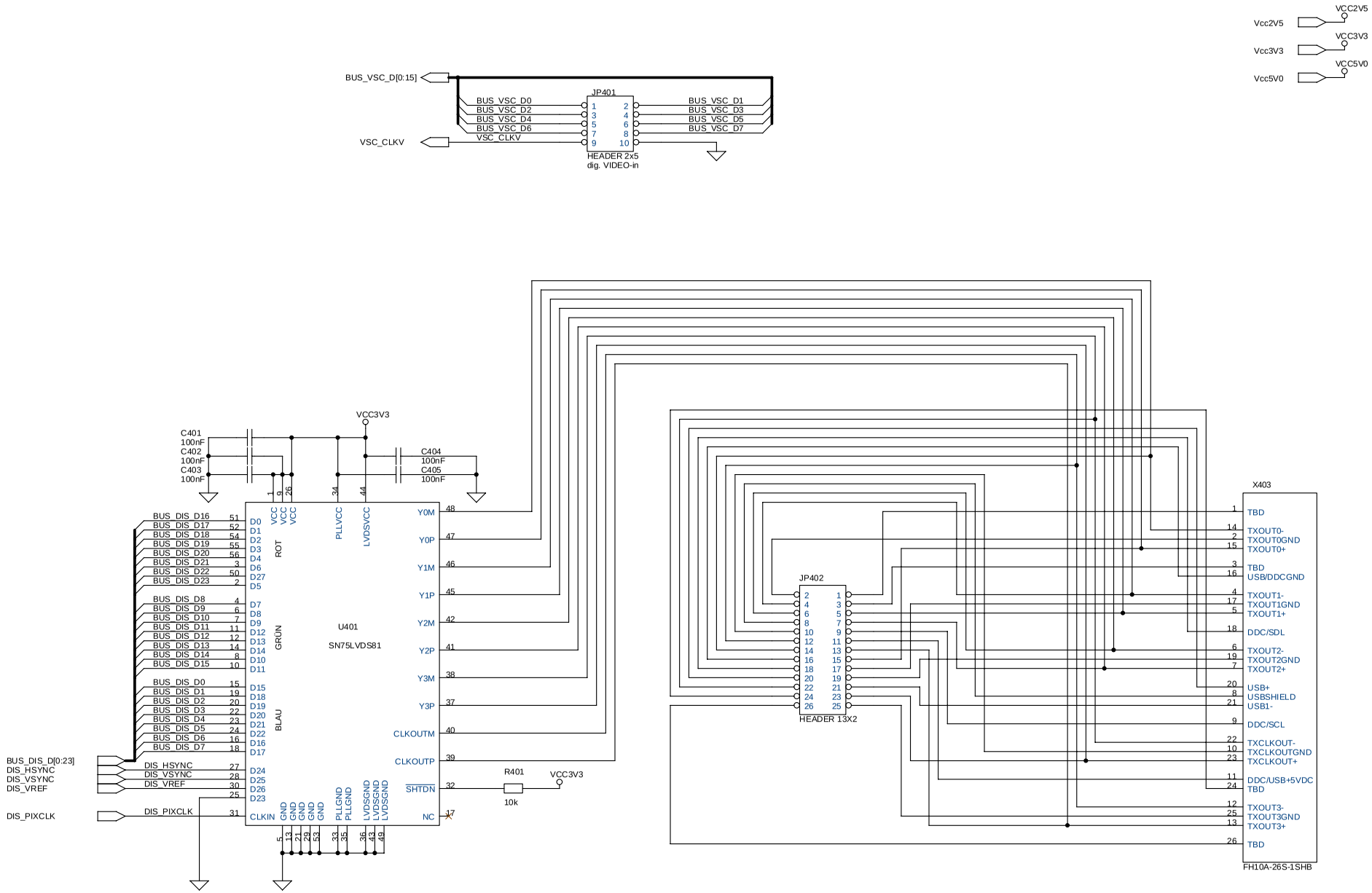

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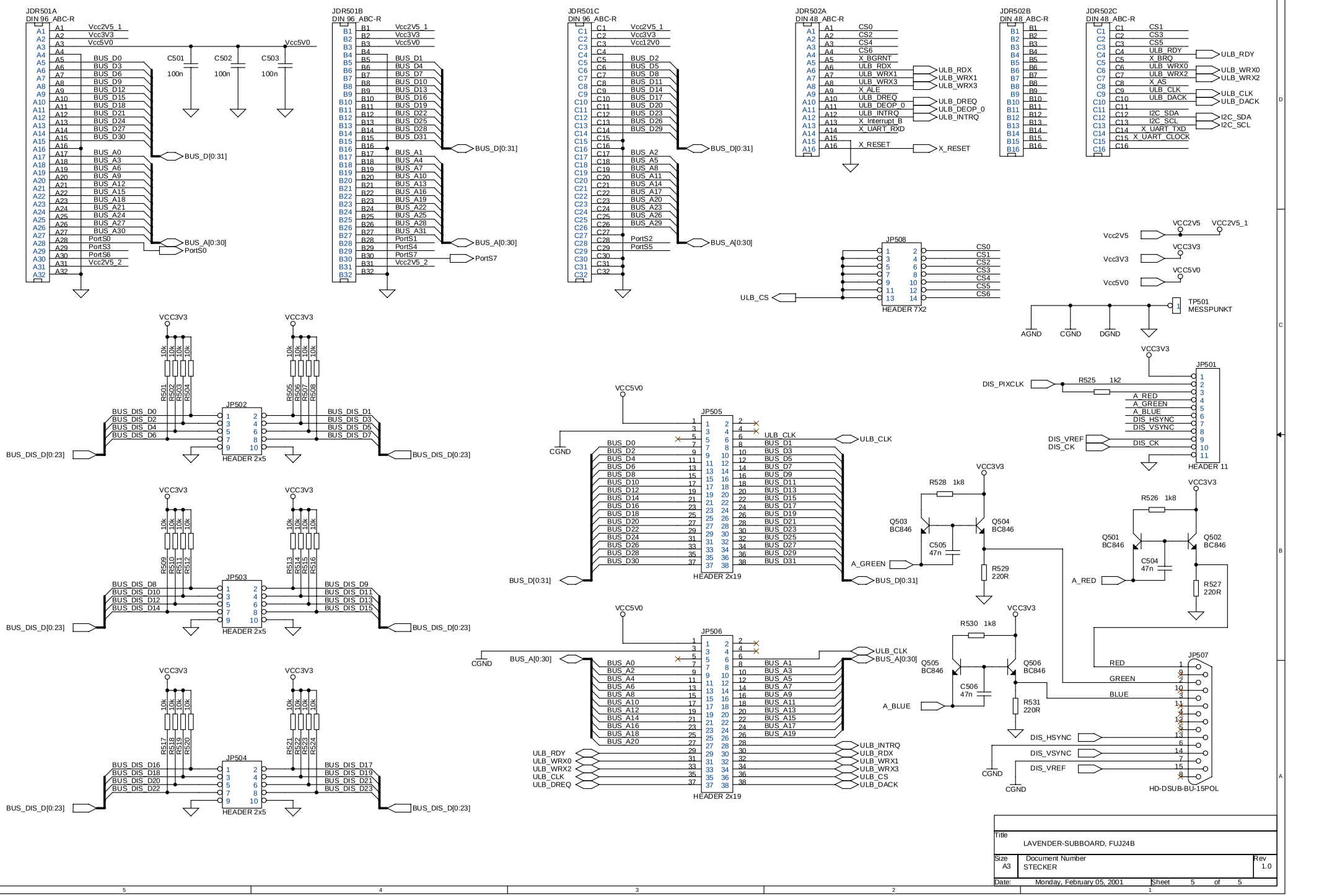

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