SCARLET

Subboard
Documentation

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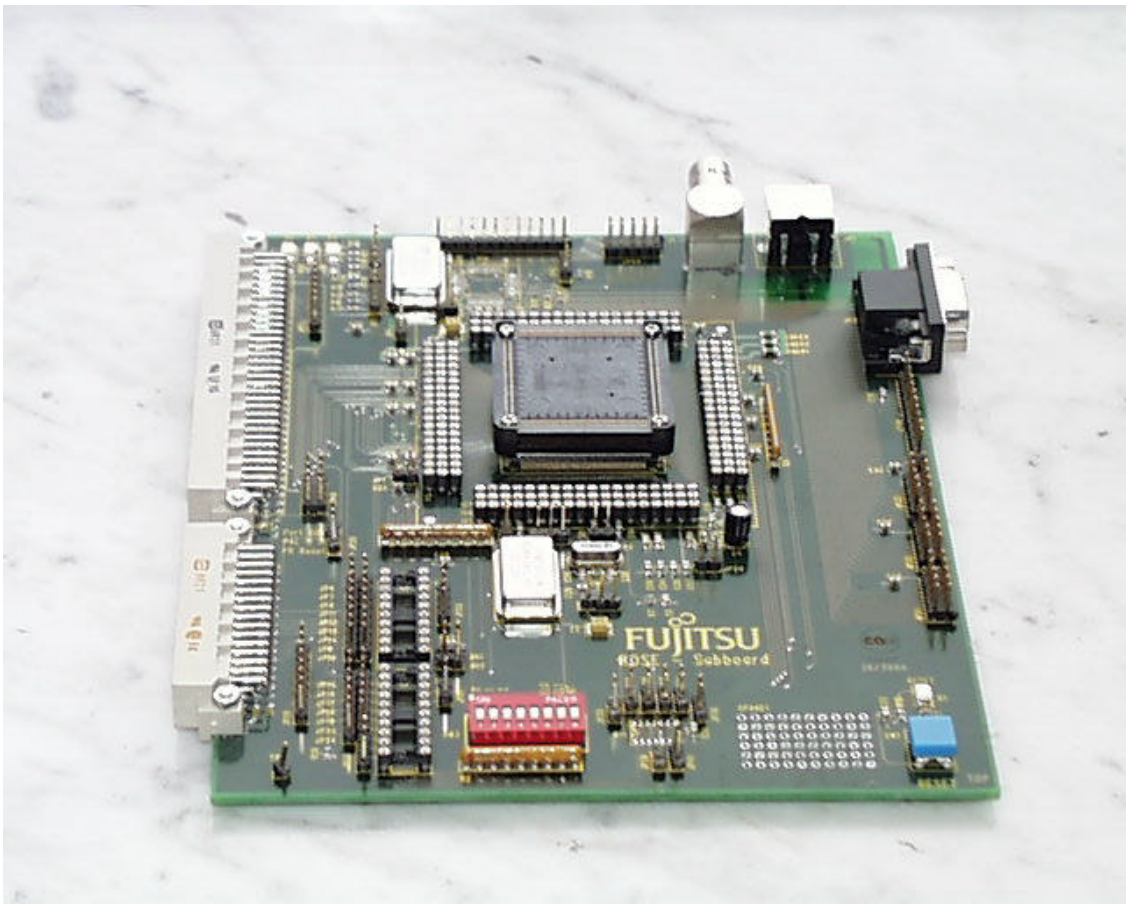

History

Revision	Date	Comment
V1.0	12.03.01	New Document
V1.1	06.06.01	Update (redesign of board)
V1.2	05.07.01	New board plan

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12.03.01 V1.0

1. Introduction

The SCARLET-Subboard is a low cost multifunctional evaluation board for Fujitsu graphic device controller Scarlet. It can be used with CREMSON-Starterkit CPU-Modul for software development and testing as a simple target board.

The board allows the designer immediately to start the software development before his own final target system is available.

2. Features

- Graphic controller Scarlet in a package HQFP208
- 14.318 MHz crystal and 14.318 MHz oscillator
- Enhanced Video Input Processor (SAA7111A)
- Quarzoszilator for VIC
- Video input connector (BNC-90)
- 2 PALLV16V8
- a 74ALS1034 (six not inverted buffer)
- 3 LEDs for power supply
- Display interface (HD-DSUB-BU-15Pol)
- “CPU-Modul” interface
- Reset button for Scarlet

3. Jumpers and Switches

This chapter describes all jumpers and switches which can be modified on the evaluation board. The default setting is shown with a gray shaded area. All jumpers and switches are named directly on the board by its meaning, so it is very easy to set the jumpers according to the features.

3.1 Power Supply Voltage (JP1, JP2, JP4, JP20)

	Jumper setting	Description
3V3 power supply (JP1)	ON (closed)	Power supply
	OFF (open)	NO Power supply

	Jumper setting	Description
2V5 power supply (JP2)	ON (closed)	Power supply
	OFF (open)	NO Power supply

	Jumper setting	Description
2V5 power supply (JP4)	ON (closed)	Power supply
	OFF (open)	NO Power supply

	Jumper setting	Description
2V5 power supply (JP20)	ON (closed)	Analog Power supply
	OFF (open)	NO Analog Power supply

NOTE:
The supply voltage for the core and the IO Pins must be set. Otherwise it could happen that the controller does not work correctly!

3.2 Define graphic controller Operating Mode (SW3)

The Scarlet can be connected to Fujitsu FR30, Hitachi SH4(SH7750), SH3(SH7709/09A) and NEC V832. The host CPU type is specified by the MODE pins.

	CPU Type	SW3/Mode0	SW3/Mode1
Mode1-0	FR30/SH3	ON	ON
	SH4	OFF	ON
	V832	ON	OFF
	Reserved	OFF	OFF

	SW3/Mode2	Description
Mode2	ON	XRDY signal finished at low level
	OFF	XRDY signal finished at high level

	SW3/CKM	Description
Clock mode signal	ON	Output from internal PLL is selected
	OFF	Host CPU bus clock is selected

	SW3/EO	Description
Even/Odd signal mode	ON	Low level output in even frame, High level output in odd frame
	OFF	High level output in even frame, Low level output in odd frame

	Clock Input	SW3/CLKSEL0	SW3/CLKSEL1
Input Clock Selection	13.5 MHz	ON	ON
	14.32 MHz	OFF	ON
	17.73 MHz	ON	OFF
	Reserved	OFF	OFF

	SW3/OSCCNT	Description
Oscillator control	ON	Control of internal clock-module (should be H-level)
	OFF	

3.3 Reset Pin (JP29)

The Jumper JP212 determines the Scarlet Reset Pin.
It can be connected directly with the Reset of the VGC, or with a port of the MCU, to execute a software Reset.

	JP29	Description
Reset	1-2	Reset from CPU-board
	2-3	Using port S0 from MCU

3.4 Video Input Processor (JP5, JP47, JP30)

	JP5	Description
Power supply voltage	On (closed)	Digital and analog supply voltage for VIC
	OFF (open)	NO power supply

	JP47	Description
VIC enable	1-2	VCC – VIC enable
	2-3	GND – VIC disable

	JP30	Description
I^2C-Bus slave address select	GND (closed)	0 = 48h for write, 49h for read
	VCC (open)	1 = 4Ah for write, 4Bh for read

	JP57	Description
I^2C-Serial data line (SDA)	1-2	Serial data line from MCU I^2C-Interface
	2-3	Serial data line from Scarlet I^2C-Interface

	JP27	Description
I^2C-Serial clock line (SCL)	1-2	Serial clock line from MCU I^2C-Interface
	2-3	Serial clock line from Scarlet I^2C-Interface

	JP58	Description
VIC signal	ON (closed)	Conclusion resistance 75 Ohm
	OFF (open)	More than 75 Ohm

3.5 Clock Settings (JP42, JP43, JP44)

	JP42	Description
Clock input enable	1-2	Scarlet clock from Oscillator Y1
	2-3	Scarlet clock from Crystal Y2

	JP43	Description
Crystal Y2	ON (closed)	Crystal enable
	OFF (open)	Crystal disable

	JP44	Description
PLL power supply	1-2	PLLVDD connect to core voltage
	2-3	PLLVDD connect to separated voltage

3.6 C-sync for display (JP5)

	JP5	Description
C-sync	ON (closed)	C-sync connected to VGA connector
	OFF (open)	C-sync not connected

3.7 PAL Settings (JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18, JP19, JP50, JP24)

	JP6	Description
Bus clock for PALLV16V8	ON (closed)	Needed for internal state machine
	OFF (open)	-

	JP7	Description
Wait request	ON (closed)	Wait request from Scarlet
	OFF (open)	-

	JP8	Description
Read strobe	ON (closed)	Read signal to Scarlet
	OFF (open)	-

	JP11	Description
Write strobe XWE0	ON (closed)	Write signal D0 – D7
	OFF (open)	-

	JP12	Description
Write strobe XWE1	ON (closed)	Write signal D8 – D15
	OFF (open)	-

	JP13	Description
Write strobe XWE2	ON (closed)	Write signal D16 – D23
	OFF (open)	-

	JP14	Description
Write strobe XWE3	ON (closed)	Write strobe D24 – D31
	OFF (open)	-

	JP9	Description
DMA acknowledge	ON (closed)	Not needed for internal logic
	OFF (open)	

	JP10	Description
DMA end operation	ON (closed)	Not needed for internal logic
	OFF (open)	

	JP15	Description
Bus clock for PALLV16V8	ON (closed)	Not needed for internal logic
	OFF (open)	

	JP16	Description
CS3	ON (closed)	CS3 for PAL logic enable
	OFF (open)	CS3 for PAL logic disable

	JP17	Description
CS4	ON (closed)	CS4 for PAL logic enable
	OFF (open)	CS4 for PAL logic disable

	JP18	Description
CS5	ON (closed)	CS5 for PAL logic enable
	OFF (open)	CS5 for PAL logic disable

	JP19	Description
CS6	ON (closed)	CS6 for PAL logic enable
	OFF (open)	CS6 for PAL logic disable

	JP50	Description
PAL Reset	ON (closed)	PAL Reset from VGC
	OFF (open)	-

	JP24	Description
Reset Switch	ON (closed)	Reset from switch SW1
	OFF (open)	-

3.7 Interrupt

	JP21 / JP52	Description
Interrupt enable	ON (closed)	Connected interrupt to MCU
	OFF (open)	-No connected

3.8 DMA

	JP23 / JP54	Description
DREQ0 enable	ON (closed)	Connected DREQ0 to MCU
	OFF (open)	-No connected

3.9 Header for Debug Signals

PWM (JP25)

- PortS7-1 - Free usable Port S (bit 1..7)

Display Signals (JP45)

- RTC0 - Real time control output
- RTS0 - PAL line identifier (SAA7111A)
- RTS1 - PAL line identifier (SAA7111A)
- V_{ref} - Vertical reference output signal
- H_{ref} - Horizontal reference output signal
- C_{ref} - Clock reference output
- HS - Horizontal sync output signal
- VS - Vertical sync output signal
- GPSW - General purpose switch output
- RES-out - Reset output (active low)

Power Supply Voltage (JP49)

- Power supply voltage (2V5, 3V3, 5V0) – GND

Video Input Processor Signals (JP84)

- SAA_VI7-0 - Digital Video Port Out-Bus from SAA7111A
- VI_CLK - Line-locked System Clock Output (27MHz) from SAA7111A

Chip Select Signals(JP28)

- CS0-6 - Chip Select from MCU

Buffer signals (JP34, JP35, JP36, JP37, JP38, JP39, JP40, JP41)

- I/O Pins for 74ALS1034 (six not inverted buffer)

Digital RED (JP31)

- R0-7 - Digital signal output (RED)

Digital GREEN (JP32)

- G0-7 - Digital signal output (GREEN)

Digital BLUE (JP33)

- B0-7 - Digital signal output (BLUE)

Analog Output (JP46)

- DCLK_OUT - Dot Clock Signal for Display
- DCLK_IN - Dot Clock Input for External Synchronization
- RED - Analog signal output (RED)
- GREEN - Analog signal output (GREEN)

- BLUE - Analog signal output (BLUE)
- H_SYNC - Horizontal sync signal output
- V_SYNC - Vertical sync signal output
- C_SYNC - Composite sync signal output
- GV - Video/Graphics Switch

PAL Output Pins (JH1, JH2, JP22, JP51, JP53)

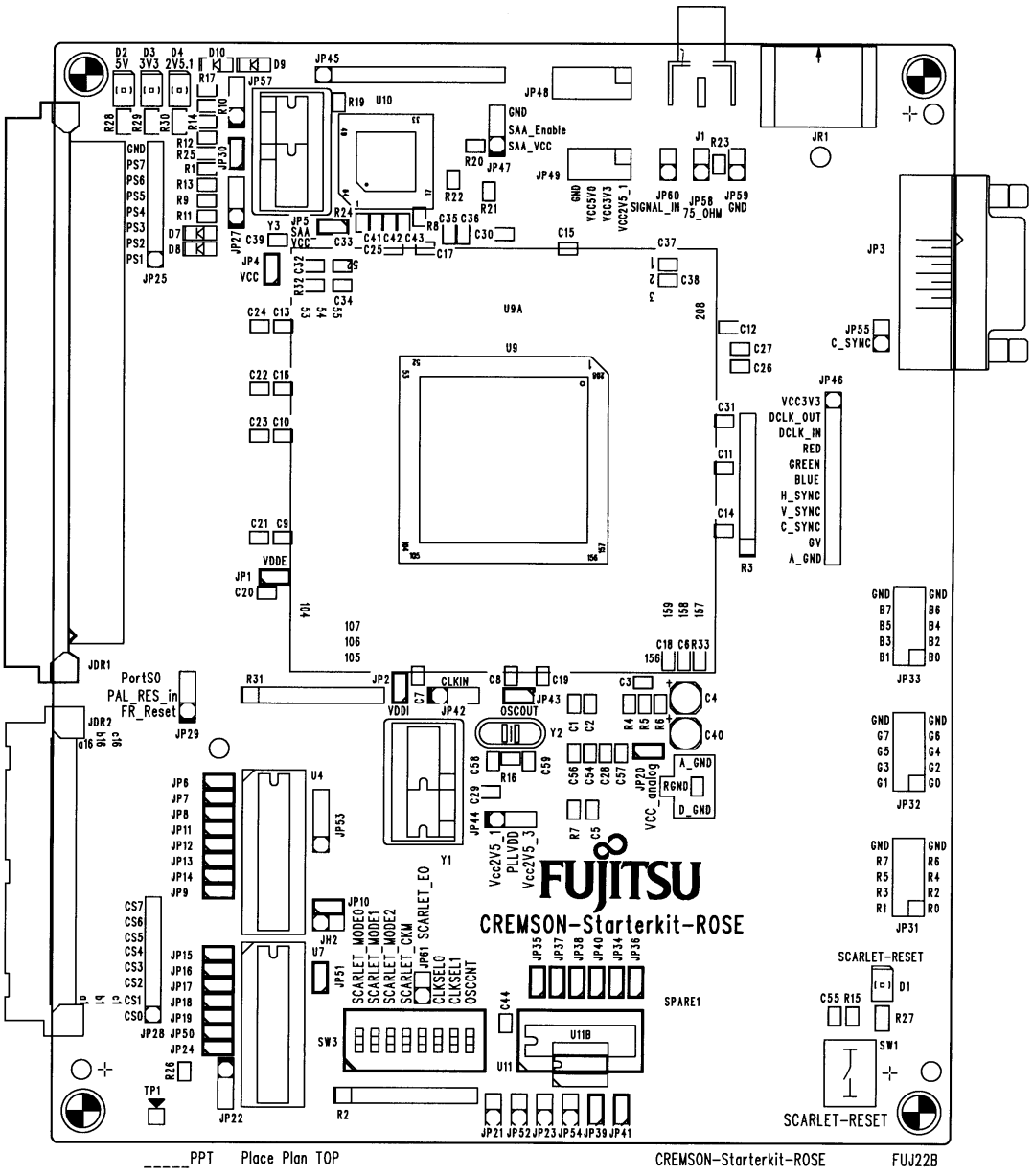
- Not used in internal Logic

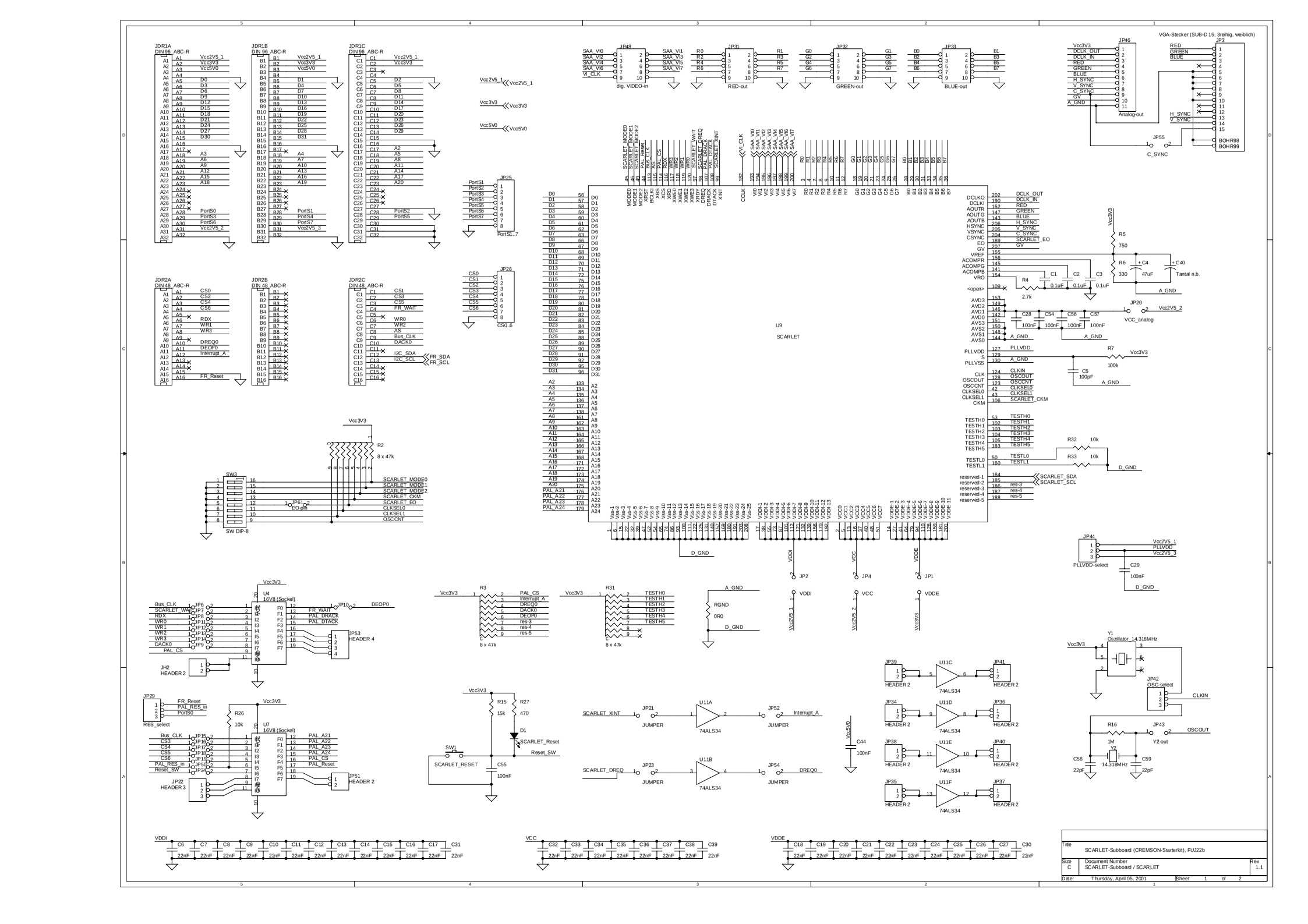
VIC Signal (JP59, JP60)

- Second connection for the video camera (video-in and camera GND)

For more information please look at the Hardware Manual of the Scarlet graphic controller, the Data Sheet of the Video Input Processor SAA7111A and the Data Sheet of the PALLV16V8.

4. Schematics and Drawings




VGA-Stecker (SUB-D 15, 3reihig, weiblich)
JDR1A
JDR1B
JDR1C
JDR2A
JDR2B
JDR2C
JP48
dig. VIDEO-in
JP31
RED-out
JP32
GREEN-out
JP33
BLUE-out
JP46
Analog-out
JP3
JP55
C_SYNC
JP25
PortS1..7
JP28
CS0..6
U9
SCARLET
JP20
VCC_analog
JP44
PLLVDD-select
SW3
SW DIP-8
U4
16V8 (Sockel)
U7
16V8 (Sockel)
JP53
HEADER 4
JP51
HEADER 2
JH2
HEADER 2
JP22
HEADER 3
JP29
RES_select
JP39
JP41
JP34
JP36
JP38
JP40
JP35
JP37
U11C
U11D
U11E
U11F
74ALS34
JP21
JUMPER
JP52
JP23
JP54
U11A
U11B
SW1
D1
Y1
Oszillator_14.318MHz
JP42
OSC-select
JP43
Y2-out
Y2
14.318MHz
Tantal n.b.
D_GND
A_GND
Vcc3V3
Vcc2V5_1
Vcc5V0
Vcc2V5_2
PLLVDD
Vcc2V5_3
VDDI
VCC
VDDE
SCARLET_MODE0
SCARLET_MODE1
SCARLET_MODE2
SCARLET_CKM
SCARLET_EO
CLKSEL0
CLKSEL1
OSCCNT
FR_SDA
FR_SCL
FR_WAIT
PAL_DRACK
PAL_DTACK
DEOP0
Interrupt_A
SCARLET_RESET
SCARLET_XINT
SCARLET_DREQ
Reset_SW
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Sheet
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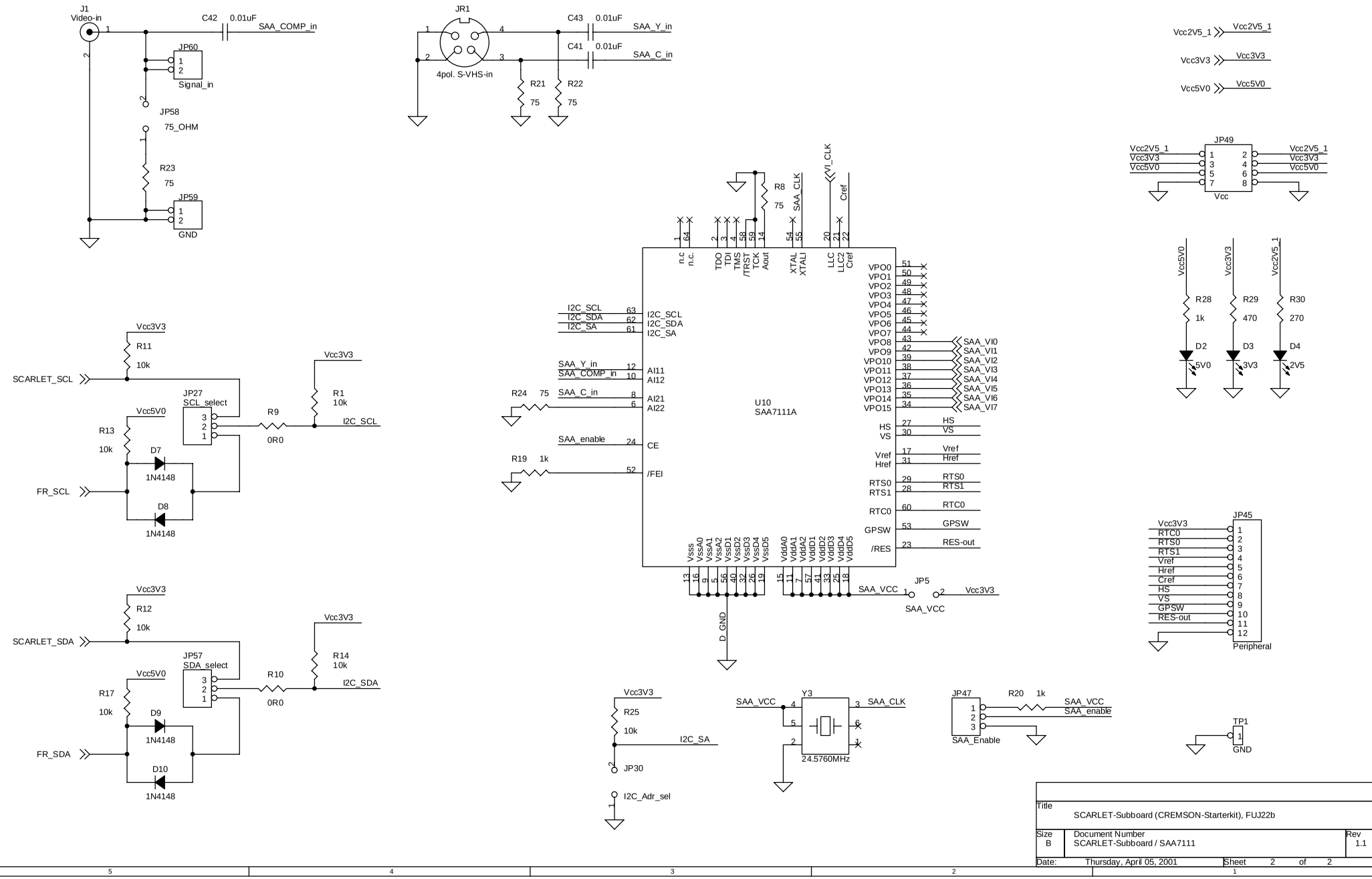

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Date: Thursday, April 05, 2001	Sheet 2 of 2	