

Addendum to
MC68705S3
8-Bit Microcomputer Unit (MCU)
ADI997R1

This addendum applies to the MC68705S3 8-bit Microcomputer Unit (MCU) device described in the MC6805S2/D data sheet (ADI997R1). MC68705S3 MCU device information contained in document ADI997R1 applies to the TJ6 mask set.


Information contained in this addendum applies to the MC68705S3 MCU device mask set A20T. The A20T mask set contains several design improvements as well as functional changes to improve performance and reliability. All material described in the MC6805S2/D data sheet also applies to the A20T mask set with the following exceptions:

1. Miscellaneous register (\$0A), watchdog control bit 4 (MR4) - Once MR4 is cleared enabling the watchdog timer, the MR4 bit cannot be set via software. The only way to disable the watchdog timer is with a reset condition. This functional change was implemented to prevent runaway software from accidentally setting the MR4 bit and preventing a watchdog reset from occurring.
2. Mask Option Register (MOR), bit 5 — Bit 5 of the MOR (\$F1E) is used to determine the port B toggle source. This bit is not used on the TJ6 mask set.
If the MOR bit 5 is cleared to a logic zero (0), then the port B toggle source operation is identical to the TJ6 mask set operation as follows:
After the first write operation to timer C, the toggle source coming from the timer B overflow is replaced by the timer C overflow. If no write operation is performed on timer C, then timer B is the port B toggle source.
If the MOR bit 5 is set to a logic one (1), then the port B toggle source will come from the timer B overflow even if a write operation is performed on timer C.
3. The minimum value for V_{IRES+} is decreased from 1.5 Vdc to 1.3 Vdc.
4. Use of a 1K ohm pullup resistor on the \overline{RESET}/V_{PP} pin (pin 23) will allow proper operation of the reset and watchdog timer operations.

CAUTION

Voltage on the \overline{RESET}/V_{PP} pin must not exceed +22.0 Vdc. MCU damage may result.



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