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Motorola Semiconductor Application Note

AN1736

Variations in the Motorola MC68HC05Px Family

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Introduction

The Motorola MC68HC05 P Family of 8-bit microcontrollers is one of the largest and most widely used. This application note clarifies the important differences among the various HC05P Family devices for anyone who may be developing an application using one of these devices. It is particularly useful for those familiar with one of the members of the family but wishes to move to another.

Since Motorola is improving specifications and optimizing its MCU portfolio constantly, the reader is always encouraged to consult the latest data books for specification details and availability.

This application note discusses:

- Similarities and comparisons
- Pinouts
- The A strategy
- Changing from OTP/FLASH to ROM
- Changing from non-A to A versions
- Voltage, frequency, and temperatures tables
- Development tools

Recommendations for Future Designs

Although this application note covers all current variants of the HC05P Family, it is recommended that these two devices not be used, as they do not have OTPs (one-time programmer), which emulate them specifically:

- HC05P8
- HC05P15

Regarding the HC05P1, HC05P4, and HC05P9, Motorola offers the A equivalent for new designs exclusively, for example HC05P1A, HC05P4A, and HC05P9A.

The HC705P6 and the HC705P9 will be discontinued in the future and the HC705P6A will be the replacement OTP.

Similarities and Comparisons

Similarities

Similarities exist in the 16-bit input capture/output compare timer and the COP watchdog.

16-Bit Input Capture/Output Compare Timer

The timer core is a 16-bit, free-running counter, which provides the timing reference for the input capture and output compare functions. The input capture and output compare functions provide a means of latching the times at which external events occur and generating output waveforms and timing delays.

The HC05P8 is the only member of the P Family which does not have a 16-bit programmable timer. It has a 15-stage ripple counter.

COP Watchdog

A COP watchdog (computer operating properly) is used in a system to make sure that the software operates correctly. At regular intervals, the COP must be refreshed. If this does not happen because the application software has “run away” or it has entered a loop that it cannot exit, the COP watchdog will time out and force an MCU reset.

The only P Family device which does not have a COP is the HC05P1. On all other P Family devices, the COP is enabled by mask option. However, there are variations in the way the COP is refreshed.

Comparisons

The P Family variations are summarized in **Table 1** and **Table 2**.

Table 1. P Family Variations

Device	05P1	05P1A	05P3	705P3	05P4	05P4A	05P6	705P6	705P6A
COP enable	No	Mask Option	Mask Option	Clear bit 1 $0F	Mask Option	Mask Option	Mask Option	Set bit 0 $1F00	Set bit 0 $1F00
COP timeout $f_{op} = f_{osc}/2$	No	$2^{17}/f_{op}$	Software selectable	Software selectable	$2^{17}/f_{op}$	$2^{17}/f_{op}$	$2^{17}/f_{op}$	$2^{17}/f_{op}$	$2^{17}/f_{op}$
COP clear	No	Clear bit 0 $1FF0	Clear bit 0 $0FF0	Clear bit 0 $0FF0	Clear bit 0 $1FF0	Clear bit 0 $1FF0	Clear bit 0 $1FF0	Clear bit 0 $1FF0	Clear bit 0 $1FF0
Stop disable	No	Mask option	No	No	No	No	Mask option	Bit 5 MOR	Bit 5 MOR2
Port A pullups	No	Mask option	No	No	No	Mask option	No	No	Yes MOR1
High current	No	PC0, PC1	No	No	No	PC0, PC1	No	No	PC0, PC1
A/D	No	No	No	No	No	No	4 channel, 8 bit	4 channel, 8 bit	4 channel, 8 bit
RC, OSC	Mask option	Mask option	No	No	Mask option	Mask option	Mask option	No	No
LVR	No	No	No	No	No	No	No	No	No
SIOP clock rate $f_{op} = f_{osc}/2$	—	—	—	—	1/4 f_{op}	1/4 f_{op}	Software selectable	Software selectable	Software selectable
SIOP MSB/LSB	—	—	—	—	Mask option	Mask option	Mask option	Bit 2 MOR	Bit 2 MOR2
Mask option register	No	No	No	$0F	No	No	No	$1F00	$1EFF, $1F00
Security	No	No	No	No	No	Yes	No	No	Yes
EEPROM	No	No	128	128	No	No	No	No	No
RAM	128	128	128	128	176	176	176	176	176
EP(ROM) exc. vectors	2096	2304	3072	3072	4144	4144	4656	4656	4656
Recom-mended OTP	705P6A	705P6A	705P3	—	705P6A	705P6A	705P6A	—	—

Table 2. Comparisons among the P Family Devices

Device	05P7	05P8	05P9	05P9A	705P9	05P15	05P18	805P18
COP enable	Mask option	Mask option	Mask option	Mask option	Set bit 0 $0900	Mask option	Mask option	Set bit 0 $3F00
COP timeout $f_{op} = f_{osc}/2$	$2^{17}/f_{op}$	Program-mable	$2^{17}/f_{op}$	$2^{17}/f_{op}$	$2^{17}/f_{op}$	$2^{17}/f_{op}$	$2^{17}/f_{op}$	$2^{17}/f_{op}$
COP clear	Clear bit 0 $1FF0	Clear bit 0 $1FF0	Clear bit 0 $1FF0	Clear bit 0 $1FF0	Clear bit 0 $1FF0	Clear bit 0 $1FF0	Clear bit 0 $3FF0	Clear bit 0 $3FF0
Stop disable	No	Mask option	No	Mask option	No	Mask option	Mask option	Yes
Port A pullups	No	No	No	Yes	No	Yes	Yes	Yes
High current	No	No	No	PC0, PC1	No	No	PC0, PC1	PC0, PC1
A/D	No	4 channel, 8 bit	4 channel, 8 bit	4 channel, 8 bit	4 channel, 8 bit	Compar-ator	4 channel, 8 bit	4 channel, 8 bit
RC OSC	Mask option	No	No	Mask option	No	Mask option	No	No
LVR	No	No	No	No	No	No	Yes	Yes
SIOP clock rate $f_{op} = f_{osc}/2$	1/4 f_{op}	—	1/4 f_{op}	1/4 f_{op}	1/4 f_{op}	—	Software selectable	Software selectable
SIOP MSB/LSB	Mask option	—	Mask option	Mask option	Bit 2 MOR	—	Mask option	Bit 2 MOR1
Mask option register	No	No	No	No	$0900	No	No	$3F00, $3F01
Security	No	No	No	Yes	No	No	No	No
EEPROM	No	32	No	No	No	No	128	128+8048
RAM	128	112	128	128	128	128	192	192
EP(ROM) exc vectors	2096	2048	2096	2096	2096	3136	8048	—
Recom-mended OTP	705P9/ 705P6A	705P9/ 705P6A	705P9/ 705P6A	705P6A	—	—	805P18	—

Stop Disable

These P Family devices do not have an option to disable stop mode:

- HC05P1
- HC05P3
- HC705P3
- HC05P4
- HC05P4A
- HC05P7
- HC05P8
- HC05P9
- HC705P9

On all other devices, stop can be disabled by a mask option.

Analog- to-Digital Converter

These P Family members do not have an analog-to-digital (A/D) converter:

- HC05P1
- HC05P1A
- HC05P3
- HC705P3
- HC05P4
- HC05P4A

All other devices, with the exception of the HC05P15, have a 4-channel, 8-bit successive approximation A/D converter. The A/D subsystem shares its inputs with port C pins PC3–PC7.

The HC05P15 has one analog voltage comparator with a digital output. It shares its pins with PB5–PB7.

RC Oscillator

The P Family devices which have an RC oscillator option are:

- HC05P1
- HC05P1A
- HC05P4
- HC05P4A
- HC05P6
- HC05P7
- HC05P9A
- HC05P15

The RC oscillator option provides a low-cost oscillator and is enabled by a mask option. An external resistor is required. **Figure 1** shows the resistor connected to the oscillator pins.

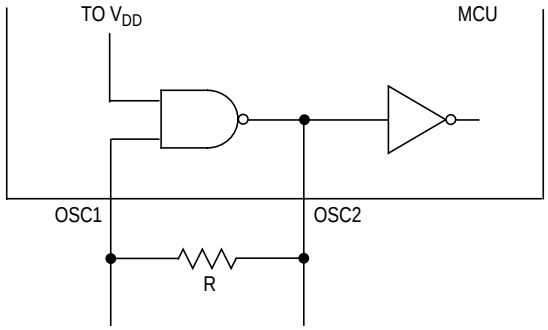

Figure 1. RC Oscillator Circuit Diagram

Since the accuracy of the RC oscillator is ±50%, the nominal design frequency must be limited to 66% of the maximum frequency to ensure that the operating frequency remains below the upper limit of operating frequency. The 50% tolerance only allows for the MCU variation, and additional allowance must be for the tolerance(s) of any external components. Refer to the device specification for the graph showing the relationship between the external resistor, R, and the operating frequency, f_{op}.

Low-Voltage Reset (LVR)

The only devices which have a low-voltage reset (LVR) are:

- HC05P18
- HC805P18

Serial Input/Output Port (SIOP)

These devices do not have an SIOP subsystem:

- HC05P1
- HC05P1A
- HC05P3
- HC705P3
- HC05P8
- HC05P15

All other P Family devices have an SIOP. It is possible to choose whether the most significant bit (MSB) or least significant bit (LSB) comes first. On some devices, the SIOP clock rate can be chosen through software or it is fixed at 1/4 of the operating frequency (f_{op}).

Pinouts

There is variation in the pin positions of the P Family devices, although they each have 28 pins.

The pinout for these devices are shown in **Figure 2**:

- HC05P1
- HC05P1A
- HC05P4
- HC05P4A
- HC05P6
- HC705P6
- HC705P6A
- HC05P7
- HC05P9
- HC05P9A
- HC705P9
- HC05P18
- HC805P18

NOTE: *The HC05P1A has two pinouts. While it has the pinout described in **Figure 2**, it also has a low-noise pinout, which is shown in **Figure 4**. This pinout is chosen on the ROM header as part number MC68LNC05P1A.*

The HC05P3 and HC705P3 have the pinout shown in **Figure 5** and the HC05P8 pinout is shown in **Figure 7**. The HC05P15 has the pinout shown in **Figure 6**.

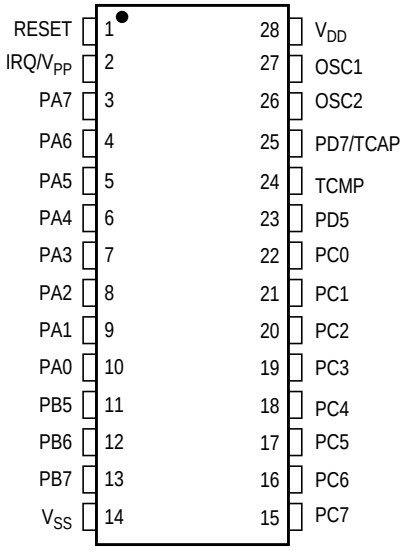

Figure 2. Pinout

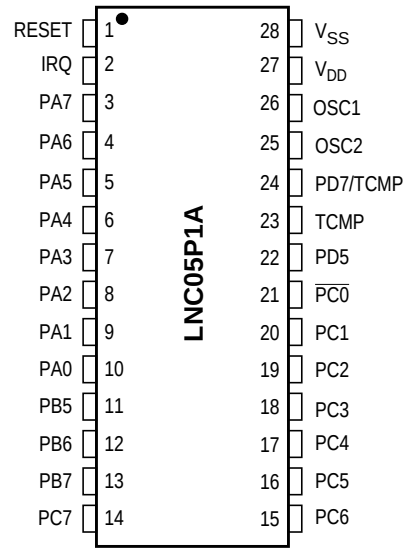

Figure 3. LNC05P1A Pinout

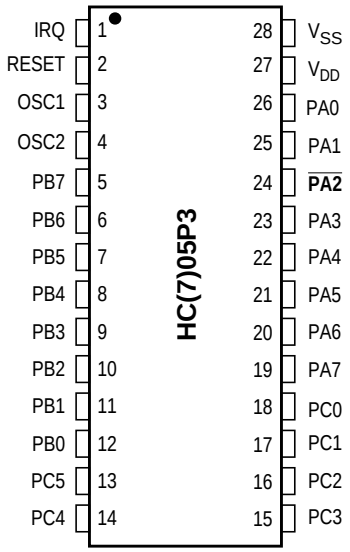

Figure 4. HC705P3 Pinout

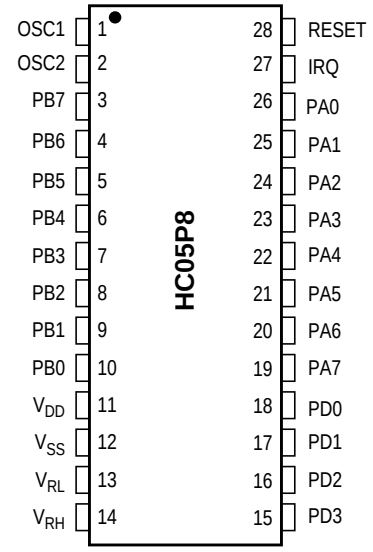

Figure 5. HC05P8 Pinout

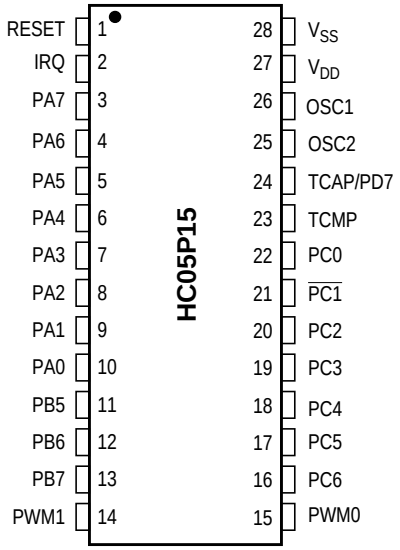

Figure 6. HC05P15 Pinout

The A Strategy

The A strategy was introduced in the P Family and other families within the Motorola 8-bit microcontrollers portfolio to enhance the features that the device offers.

The A features include:

- Port A pullups
- High current drive capability on PC0 and PC1
- (EP)ROM security

Port A Interrupts/Pullups

Port A has mask options to enable pullup devices and interrupt capability on each pin. **Figure 7** shows the port A setup.

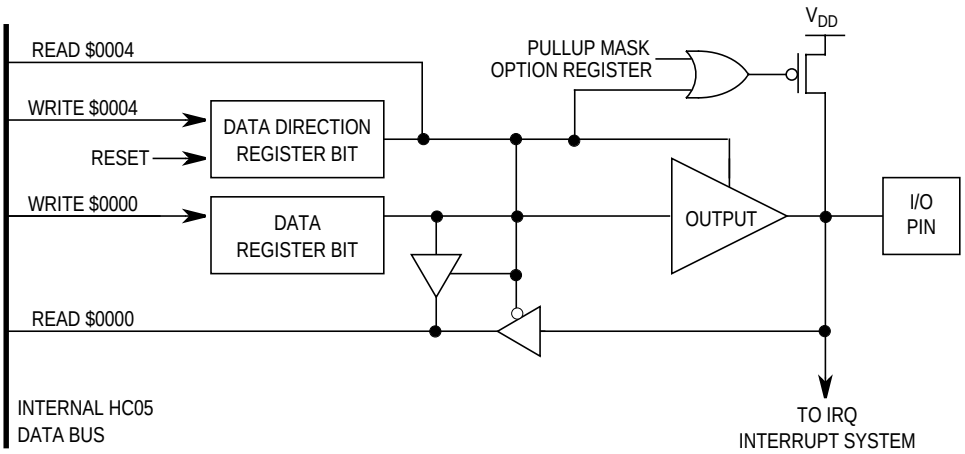

Figure 7. Port A I/O and Interrupt Circuitry

High Current Drive on PC0, PC1

The output current drive capability on port C bit 0 and bit 1 has been increased. **Table 3** shows the differences between the non-A and A devices.

Table 3. Port C Pin 7 Characteristics

Characteristic	Non-A	P1A/P4A	P9A/705P6A
V_{DD} = 5.0 V PC0, PC1 current drive (I_{OH}) @ V_{OH} = V_{DD} –0.8 V PC0, PC1 current sink (I_{OL}) @ V_{OL} = 0.4 V	0.8 mA 1.6 mA	5.0 mA 15.0 mA	5.0 mA 10.0 mA
V_{DD} = 3.0 V PC0, PC1 current drive (I_{OH}) @ V_{OH} = V_{DD} –0.3 V PC0, PC1 current sink (I_{OL}) @ V_{OL} = 0.3 V	0.2 mA 0.4 mA	1.5 mA 6.0 mA	1.2 mA 2.5 mA

(EP)ROM Security

Security has been incorporated into the P Family A devices to help prevent unauthorized reading of code in the (EP)ROM. On the ROM devices, this is fixed during manufacturing, not as a mask option on the ROM header.

On the HC705P6A, the security is enabled by setting bit 7 in the mask option register at address $1F00.

NOTE: *The only exception to this is the HC05P1A, which does not have ROM security.*

Changing from OTP/FLASH to ROM

These conversions are discussed in this application note:

- HC705P6A to HC05P6
- HC705P6A to HC05P7
- HC705P6A to HC05P8
- HC705P6A to HC05P1A
- HC705P6A to HC05P4A
- HC705P6A to HC05P9A
- HC705P9 to HC05P6
- HC705P9 to HC05P7
- HC705P9 to HC05P8
- HC705P9 to HC05P1A
- HC705P9 to HC05P4A
- HC705P9 to HC05P9A
- HC805P18 to HC05P18

HC705P6A to HC05P6

Memory

The memory maps of the HC705P6A and the HC05P6 are identical.

Mask Options

These options are chosen by manipulating bits in the mask option register(s) on the HC705P6A, but on the HC05P6 they are chosen when submitting ROM code to the factory via the mask option header.

- COP watchdog, enable/disable
- Stop, enable/disable
- SIOP, MSB/LSB
- IRQ sensitivity, edge or edge and level

Functional Blocks

The HC705P6A and HC05P7 have these differences:

- The SIOP clock rate is software selectable on the HC705P6A, but on the HC05P7 the clock rate is fixed at 1/4 operating frequency.
- The HC705P6A has stop disable, port A pullups/Interrupts, EPROM security (mask programmable options) and PC0 and PC1 as high current ports. The HC05P7 does not have these functions.
- The HC705P6A has an A/D subsystem, and the HC05P7 does not.
- The HC05P7 has an optional RC oscillator, and the 7HC05P6A does not.

HC705P6A to HC05P8

Memory

The HC705P6A has 176 bytes RAM starting at address $0050. The HC05P8 has 112 bytes starting at address $0090.

The HC705P6A has 4656 bytes of ROM starting at address $0100. The HC05P8 has 2048 bytes starting at address $1680.

The HC05P8 has 32 bytes of EEPROM starting at address $0030. This is not on the HC705P6A.

Mask Options

These two options are chosen by manipulating bits in the mask option register(s) on the HC705P6A, but on the HC05P8 they are chosen when submitting ROM code to the factory via the mask option header.

- COP watchdog, enable/disable
- IRQ sensitivity, edge or edge and level

Functional Blocks

The HC705P6A and the HC05P8 have these differences:

- The HC705P6A has stop disable, port A pullups/interrupts, EPROM security (mask programmable options), and PC0 and PC1 as high current ports. The HC05P8 does not have these functions.
- An SIOP subsystem is on the HC705P6A. This is not present on the HC05P8.

HC705P6A to HC05P1A

Memory

The HC705P6A has 176 bytes of RAM starting at address $0050. The HC05P1A has 128 bytes starting at address $0080.

The HC705P6A has 4656 bytes of EPROM. The HC05P1A has 2304 bytes. Both devices have their main user (EP)ROM starting at address $0100.

The HC705P6A and HC05P1A both have their user vector areas starting at $1FF8.

Mask Options

These options are chosen by manipulating bits in the mask option register(s) on the HC705P6A, but on the HC05P1A they are chosen when submitting ROM code to the factory via the mask option header.

- COP watchdog, enable/disable
- Port A pullups/interrupts, enable/disable
- Stop, enable/disable
- IRQ sensitivity, edge or edge and level

Functional Blocks

The HC705P6A has these functions and the HC05P1A does not:

- A/D subsystem
- SIOP subsystem
- EPROM security, mask programmable option

The HC05P1A has an optional RC oscillator, and the HC705P6A does not.

HC705P6A to HC05P4A

Memory

The HC705P6A and the HC05P4A have 176 bytes of RAM starting at address $0050.

The HC705P6A has 4656 bytes EPROM. The HC05P4A has 4144 bytes. Both devices have their main user EPROM starting at address $0100.

The HC705P6A and HC05P4A both have the user vector area starting at address $1FF8.

Mask Options

These options are chosen by manipulating bits in the mask option register(s) on the HC705P6A, but on the HC05P4A they are chosen when submitting ROM code to the factory via the mask option header.

- COP watchdog, enable/disable
- Port A pullups/interrupts, enable/disable
- SIOP, MSB/LSB
- IRQ sensitivity, edge or edge and level

Functional Differences

The HC705P6A has an A/D subsystem, and the HC05P4A does not.

The HC05P4A has an optional RC oscillator, and the HC705P6A does not.

The HC705P6A has optional stop disable, and the HC05P4A does not.

The SIOP clock rate is software selectable on the HC705P6A, but on the HC05P4A the clock rate is fixed at 1/4 operating frequency.

HC705P6A to HC05P9A

Memory

The HC705P6A has 176 bytes RAM starting at address $0050. The HC05P9A has 128 bytes starting at address $0080.

There are 4656 bytes of EPROM on the HC705P6A and 2096 bytes of ROM on the HC05P9A. Both devices have their main user (EP)ROM starting at address $0100.

The HC705P6A and HC05P9A both have their user vector areas starting at address $1FF8.

Mask Options

These options are chosen by manipulating bits in the mask option register(s) on the HC705P6A, but on the HC05P9A they are chosen when submitting ROM code to the factory via the mask option header.

- COP watchdog, enable/disable
- Port A pullups/interrupts, enable/disable
- Stop, enable/disable
- SIOP, MSB/LSB
- IRQ sensitivity, edge or edge and level

Functional Blocks

The HC05P9A has an optional RC oscillator, and the HC705P6A does not.

The SIOP clock rate is software selectable on the HC705P6A, but on the HC05P9A the clock rate is fixed at 1/4 operating frequency.

HC705P9 to HC05P6

Memory

The HC05P6 has 176 bytes of RAM starting at address $0050. The HC705P9 has 128 bytes starting at address $0080.

The HC05P6 has 4656 bytes of ROM and the HC705P9 has 2096 bytes. Both devices have their main user (EP)ROM starting at address $0100.

Mask Options

These options are chosen by manipulating bits in the mask option register(s) on the HC705P9, but on the HC05P6 they are chosen when submitting ROM code to the factory via the mask option header.

- COP watchdog, enable/disable
- SIOP, MSB/LSB
- IRQ sensitivity, edge or edge level

Functional Blocks

The HC05P6 has optional stop disable, and the HC705P9 does not.

The HC05P6 has an optional RC oscillator, and the HC705P9 does not.

The SIOP clock rate is software selectable on the HC05P6, but on the HC705P9 the clock rate is fixed at 1/4 operating frequency.

HC705P9 to HC05P7

Memory

The memory maps of the HC705P9 and the HC05P7 are identical.

Mask Options

These options are chosen by manipulating bits in the mask option register(s) on the HC705P9, but on the HC05P7 they are chosen when submitting ROM code to the factory via the mask option header.

- COP watchdog, enable/disable
- IRQ sensitivity, edge or edge and level

Functional Blocks

The HC705P9 has an A/D subsystem, but the HC05P7 does not.

The HC05P7 has an optional RC oscillator, but the HC705P9 does not.

HC705P9 to HC05P8

Memory

The HC705P9 has 128 bytes of RAM starting at address $0080. The HC05P8 has 112 bytes starting at address $0090.

The HC705P9 has 2096 bytes of ROM starting at address $0100. The HC05P8 has 2048 bytes starting at address $1680.

The HC05P8 has 32 bytes of EEPROM starting at address $0030. The HC705P9 does not have EEPROM.

Mask Options

These options are chosen by manipulating bits in the mask option register(s) on the HC705P9, but on the HC05P8 they are chosen when submitting ROM code to the factory via the mask option header.

- COP watchdog, enable/disable
- IRQ sensitivity, edge or edge and level

Functional Blocks

The HC05P9 has an SIOP subsystem, and the HC05P8 does not.

HC705P9 to HC05P1A

Memory

The HC705P9 and the HC05P1A both have 128 byes of RAM starting at address $0080.

The HC705P9 has 2096 bytes of EPROM. The HC05P1A has 2304 bytes of ROM. Both devices have their main user EPROM beginning at address $0100.

The HC705P9 and HC05P1A both have their user vector areas starting at address $1FF8.

Mask Option

These two options are chosen by manipulating bits in the mask option register(s) on the HC705P9, but on the HC05P1A the option is chosen when submitting ROM code to the factory via the mask option header.

- COP watchdog, enable/disable
- IRQ sensitivity, edge or edge and level

Functional Differences

The HC05P1A has stop disable, port A pullups/interrupts, mask programmable options, and PC0 and PC1 as high current ports. The HC705P9 does not have these functions.

There is an A/D subsystem on the HC705P9, but it is not on the HC05P1A.

There is no RC oscillator option on the HC705P9, but it is an option on the HC05P1A.

There is an SIOP subsystem on the HC705P9, but it is not present on the HC05P1A.

HC705P9 to HC05P4A

Memory

The HC05P9 has 128 bytes of RAM starting at address $0080. The HC05P4A has 176 bytes of RAM starting at address $0050.

There are 2096 bytes of EPROM on the HC705P9. On the HC05P4A, there are 4144 bytes. Both devices have their main user EPROM beginning at address $0100.

The HC705P9 and the HC05P4A both have their user vector areas starting at address $1FF8.

Mask Options

These options are chosen by manipulating bits in the mask option register(s) on the HC705P9, but on the HC05P4A they are chosen when submitting ROM code to the factory via the mask option header.

- COP watchdog, enable/disable
- SIOP, MSB/LSB
- IRQ sensitivity, edge or edge and level

Functional Blocks

The HC05P4A has stop disable, port A pullups/interrupts (mask programmable options), ROM security, and PC0 and PC1 as high current ports. The HC705P9 does not have these functions.

There is an A/D subsystem on the HC705P9 that is not on the HC05P4A.

The HC705P9 has no RC oscillator option, but it is an option on the HC05P4A.

HC705P9 to HC05P9A

Memory

The HC705P9 and the HC05P9A both have:

- 128 bytes of RAM starting at address $0050
- 2096 bytes of ROM starting at address $0100
- User vector areas starting at address $1FF8

Mask Options

These options are chosen by manipulating bits in the mask option register(s) on the HC705P9, but on the HC05P9A they are chosen when submitting ROM code to the factory via the mask option header.

- COP watchdog, enable/disable
- SIOP, MSB/LSB
- IRQ sensitivity, edge or edge and level

Functional Blocks

The HC05P9A has stop disable, port A pullups/interrupts (mask programmable options), EPROM security, and PC0 and PC1 are high current ports. The HC05P9 does not have these functions.

There is no RC OSC option on the HC705P9, but it is an option on the HC05P9A.

HC805P18 to HC05P18

Memory

The memory maps of the HC805P18 and the HC05P18 are identical.

Mask Options

These options are chosen by manipulating the bits in the mask option registers on the HC05P18, but on the HC05P18 they are chosen when submitting ROM codes to the factory via the mask option header.

- IRQ sensitivity, edge or edge and level
- SIOP, MSB/LSB
- SIOP clock rate
- COP watchdog, enable/disable
- Port A pullups/interrupts, enable/disable

Functional Blocks

All functional blocks on the HC805P18 and the HC05P18 are identical.

Changing from Non-A to A Versions

These conversions are discussed in this application note:

- HC05P1 to HC05P1A
- HC05P4 to HC05P4A
- HC05P9 to HC05P9A
- HC705P6 to HC705P6A
- HC705P9 to HC705P6A

HC05P1 to HC05P1A

The HC05P1 and the HC05P1A have differences. For instance, the HC05P1A has:

- Port A pullups/interrupts, mask option
- COP watchdog enable/disable, mask option
- Stop conversion to halt mode, mask option
- High current drive capability on PC0 and PC1
- 2304 bytes of ROM; HC05P1 has 2096 bytes

To provide compatibility with the HC05P1, choose these mask options:

- Port A pullups disabled
- COP watchdog disabled
- Stop enabled

HC05P4 to HC05P4A

HC05P4 and the HC05P4A have differences. The HC05P4A has:

- ROM security, transparent to user
- Mask programmable pullups/interrupts on port A, mask option
- High current drive capability on PC0 and PC1

To provide compatibility with the HC05P4, choose this mask option:

- Port A pullups disabled

HC05P9 to HC05P9A

The HC05P9 and the HC05P9A have differences. For instance, the HC05P9A has:

- RC oscillator, mask option
- Port A pullups/interrupts, mask option
- Stop enable/disable, mask option
- High current drive capability on PC0 and PC1
- ROM security, transparent to user

To provide compatibility with the HC05P9, choose these mask options:

- Port A pullups disabled
- Stop enabled
- Internal OSC input should be crystal/ceramic resonator

HC705P6 to HC705P6A

The HC705P6A is a pin-compatible upgrade of the HC705P6 with these enhancements:

- EPROM/OTP secure mode added
- Keyboard interrupts and pullup options for port A lines
- Two high current drive pins added, PC0 and PC1

The HC705P6 mask option register (MOR) is located at $1F00 and is used to control these options:

- COP watchdog, enable/disable
- IRQ sensitivity, edge or edge and level
- SIOP, MSB/LSB
- SIOP clock rate
- Stop, enable/disable

On the HC705P6A, two mask option registers (MOR) are at addresses $1EFF and $1F00.

$1EFF controls whether port pullups/interrupts capability is enabled for each of the port A I/O lines. $1F00 controls these options:

- COP watchdog, enable/disable
- IRQ sensitivity, edge or edge and level
- SIOP, LSB/MSB
- SIOP clock rate
- Stop, enable/disable
- EPROM security, enable/disable

The M68HC705P9PGMR programs 68HC705P6As without modification, using the same V_{PP} and following the same procedure as programming HC705P6s. If you are using a third party programmer, make sure you contact the manufacturer for a possible software upgrade to support programming HC705P6As.

MOR Programming

On both the HC705P6 and the HC705P6A, the mask option register (MOR) is programmed in bootloader mode, using the hardware shown in the respective specifications.

On the HC705P6 the programming procedure is:

1. Write the desired data to the MOR.
2. Apply the programming voltage to the IRQ/V_{PP} pin.
3. Set the MPGM (mask option register programming) bit in the EPROM programming register at address $001C.
4. Wait for programming time, t_{EPGM}.
5. Clear the MPGM bit.
6. Remove the programming voltage from the IRQ/V_{PP} pin.

The HC705P6A has no MPGM (mask option register programming) bit.

On the HC705P6A, the procedure is:

1. Set the ELAT (EPROM latch) bit in the EPROM programming register at address $001C.
2. Write the desired data to the desired MOR address, $1EFF or $1F00.
3. Set the EPGM (EPROM programming) bit in the EPROM programming register at address $001C.
4. Wait for programming time, t_{EPGM}.
5. Clear the ELAT and EPGM bits.
6. Remove the programming voltage from the IRQ/V_{PP} pin.

HC705P9 to HC705P6A

The HC705P6A is a pin-compatible upgrade of the HC705P9 with these enhancements:

- RAM memory increased from 128 bytes to 176 bytes
- EPROM/OTP memory increased from 2096 bytes to 4656 bytes
- EPROM/OTP secure mode added
- Keyboard interrupts and pullup options for port A lines
- Two high current drive pins added, PC0 and PC1
- Stop enable/disable
- SIOP clock rate

The HC705P9 mask option register (MOR) is located at $0900 and is used to control these options:

- COP watchdog, enable/disable
- IRQ sensitivity, edge or edge and level
- SIOP, MSB/LSB

The HC705P6A uses address $0900 for EPROM/OTP program area. Two new mask option registers are used on the HC705P6A.

$1EFF controls whether port pullups/interrupts capability is enabled for each of the port A I/O lines. $1F00 controls these options:

- COP watchdog, enable/disable
- IRQ sensitivity, edge or edge and level
- SIOP, MSB/LSB
- SIOP clock rate
- Stop, enable/disable
- EPROM security, enable/disable

The M68HC705P9PGMR programs 68HC705P6As without modification, using the same V_{PP} and following the same procedure as programming HC705P9s. If you are using a third party programmer, make sure to contact the manufacturer for a possible software upgrade to support programming HC705P6As.

MOR Programming

On both the HC705P9 and the HC705P6A, the mask option register (MOR) is programmed in bootloader mode using the hardware shown in the respective specifications. The procedures for both devices are identical.

7. Set the ELAT (EPROM latch) bit in the EPROM programming register at address $001C.
8. Write the desired data to the desired MOR address, $1EFF or $1F00.
9. Set the EPGM (EPROM programming) bit in the EPROM programming register at address $001C.
10. Wait for programming time, t_{EPGM}.
11. Clear the ELAT and EPGM bits.
12. Remove the programming voltage from the IRQ/V_{PP} pin.

Shrink Level

The A parts are manufactured as 1.2 μm technology or smaller, whereas the non-A parts are 1.5 μm or 1.75 μm technology.

While the electrical and functional specifications of the device remain unchanged, the EMC (electromagnetic compatibility) performance of a device may change with package type, shrink level, ROM size, and type of programmable memory (EPROM or ROM). Every new MCU should be treated and tested independently. Sensible application design guidelines should be used to minimize the noise presented to the MCU.

Three application notes and one article, designed to help customers develop good EMC behavior into their applications, are available. The application notes can be ordered through Motorola channels as documents or can be found on the Worldwide Web at http://motorola.com.sps.

- *Designing for Electromagnetic Compatibility with Single Chip MCUs*, Motorola document order number AN1263/D
- *Designing for Electromagnetic Compatibility with HCMOS MCUs*, Motorola document order number AN1050
- *System Design and Layout Techniques for Noise Reduction in MCU-Based Systems*, Motorola document order number AN1259/D

The article *Fast Transients and Noise Susceptibility of 8-Bit Microcontroller Applications* can be found in the October/November 1996 issue of the publication “Embedded System Engineering” (Vol. 4, No. 6).

The HC05P18 and the HC805P18 are the only two non-A parts which are manufactured at 1.2 µm technology.

Voltage, Frequency, and Temperature

Table 4 provides the voltage, speed, and temperature specifications for the P Family of MCUs.

Temperature ranges are:

- 0 °C to +70 °C
- C = –40 °C to +85 °C
- V = –40 °C to +105 °C
- M = –40 °C to +125 °C

The high speed and low power options on the ROM devices are chosen at the time of submission of ROM code to the factory.

Table 4. Voltage, Speed, and Temperature Specifications for the P Family

Device	Maximum bus speed/voltage options	Temperature	Comments
MC68HC05P1	V ±10% / 2.1 MHz 3.3 V ± 10% / 1 MHz 5 V ± 10% / 4 MHz 3.3 V ± 10% / 2.1 MHz 5 V ± 10% / 2.1 MHz 2.4 V to 3.6 V / 1 MHz 1.8 V to 3.6 V / 0.5 MH	0–70, C, V, M 0–70, C, V, M 0–70 only 0–70 only 0–70 only 0–70 only 0–70 only	 High speed High speed Low power Low power Low power
MC68HC05P1A	5 V ± 10% / 2.1 MHz 3.3 V ± 10% / 1 MHz 5 V ± 10% / 4 MHz 3.3 V ± 10% / 2.1 MHz 5 V ± 10% / 2.1 MHz 2.4 V to 3.6 V / 1 MHz 1.8 V to 3.6 V / 0.5 MHz	0–70, C, V 0–70, C, V 0–70, C 0–70, C 0–70 only 0–70 only 0–70 only	 High speed High speed Low power Low power Low power
MC68HC05P3	5 V ± 10% / 2.1 MHz 3.3 V ± 10% / 1 MHz	0–70, C, V 0–70, only	
MC68HC705P3	5 V ± 10% / 2.1 MHz 3.3 V ± 10% / 1 MHz	0–70, C 0–70, C	
MC68HC05P4	5 V ± 10% / 2.1 MHz 3.3 V ± 10% / 1 MHz 5 V ± 10% / 4 MHz 3.3 V ± 10% / 2.1 MHz 5 V ± 10% / 2.1 MHz 2.4 V to 3.6 V / 1 MHz 1.8 V to 3.6 V / 0.5 MHz	0–70, C, V 0–70, C, V 0–70, C 0–70, C 0–70 only 0–70 only 0–70 only	 High speed High speed Low power Low power Low power
MC68HC05P4A	5 V ± 10% / 2.1 MHz 3.3 V ± 10% / 1 MHz 5 V ± 10% / 4 MHz 3.3 V ± 10% / 2.1 MHz 5 V ± 10% / 2.1 MHz 2.4 V to 3.6 V / 1 MHz 1.8 V to 3.6 V / 0.5 MHz	0–70, C, V 0–70, C, V 0–70, C 0–70, C 0–70 only 0–70 only 0–70 only	 High speed High speed Low power Low power Low power
MC68HC05P6	5 V ± 10% / 2.1 MHz 3.3 V ± 10% / 1 MHz	0–70, C, V, M 0–70, C, V, M	
MC68HC705P6	5 V ± 10% / 2.1 MHz 3.3 V ± 10% / 1 MHz	0–70, C 0–70, C	
MC68HC705P6A	5 V ± 10% / 2.1 MHz 3.3 V ± 10% / 1 MHz	0–70, C 0–70, C	

Table 4. Voltage, Speed, and Temperature Specifications for the P Family (Continued)

Device	Maximum bus speed/voltage options	Temperature	Comments
MC68HC05P7	5 V ± 10% / 2.1 MHz 3.3 V ± 10% / 1 MHz	0–70, C, V, M 0–70, C, V, M	
MC68HC05P8	5 V ± 10% / 2.1 MHz 3.3 V ± 10%/ 1 MHz	0–70, C 0–70, C	
MC68HC05P9	5 V 10% / 2.1 MHz 3.3 V ± 10% / 1 MHz	0–70, C, V, M 0–70, C, V, M	
MC68HC05P9A	5 V ± 10% / 2.1 MHz 3.3 V ± 10% / 1 MHz	0–70, C, V, M 0–70, C, V, M	
MC68HC705P9	5 V ± 10% / 2.1 MHz 3.3 V ± 10% / 1 MHz	0–70, C 0–70, C	
MC68HC05P15	5 V ± 10% / 2.1 MHz	0–70, C, V	
MC68HC05P18	5 V ± 10% / 2.1 MHz	0–70, C, V, M	
MC68HC805P18	5 V ± 10% / 2.1 MHz	0–70, C, V, M	

Development Tools and Programmers

Table 5 shows the development tools available for the P Family and **Table 6** shows the programmer boards.

Table 5. Development Tools for the P Family

Device	Emulator order number	Package	Target cable	Target head adapter	Surface mount
MC68HC(7)05P3	M68EM05P3	28 PDIP-P 28 SOIC-DW	M68CBL05A M68CBL05A	M68TAX4P28 M68TAX4P28	M68DIP28SOIC
MC68HC05P1/ P1A/P4/P4A/P6/ 7P6(A)/P7/P9A/7P9	X68EML05PA	28 PDIP-P 28 SOIC-DW	M68CBL05A M68CBL05A	M68CBL05A M68CBL05A	M68DIP28SOIC
MC68HC05P18	X68EM05P18	28 PDIP-P 28 SOIC-DW	M68CBL05A M68CBL05A	M68TA05P9P28 M68TA05P9P28	M68DIP28SOIC

Table 6. P Family Programmer Boards

Device	Packages supported	Programmer board
MC68HC705P3	28 PDIP-P 28 SOIC-DW	M68HC705E6PGMR
MC68HC705P6/705P6A/705P9	28 SIP-P/S	M68705P9PGMR
MC68HC805P18	28 SIP-P/S	X68HC805P18PGMR

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