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MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN1029

TV Transposers Band IV and V P_O = 0.5 W/1.0 W

This note describes the performance of a broadband (470-860 MHz) ultra linear amplifier designed for service in band IV and V T V transposers.
Device used :

TPV 596.

Basic specs :

I.M.D. — 60 dB max. at Po = 0.5 watts
Vce = 20 volts ; Ic = 200 mA
Pgain = 11.5 dB min.

The approach used is intended to be straight forward and inexpensive as follows.

1) The load line be defined to provide the correct match for peak power (P. sync).
2) The VSWR at the collector be less than 2 : 1.
3) The input match be designed to provide flat gain with decreasing frequency.
4) Use computer aided design.
5) Use a three tone norm
   Pvision = — 8 dB
   Psound = — 7 dB
   Psideband = — 16 dB
6) Circuit realization to be a distributed design built upon teflon glass copper clad circuit boards. However the design will be analized using Er = 1.0.

The input and output impedances were taken from the TPV596 data sheet and plotted on a smith chart. First consider the input. To have flat gain with an optimum collector load, the basic physics of a class «A» biased device defines a gain slope of −6 dB/octave which must be compensated for. The band of interest is 470–860 MHz which is .915 octaves which implies that 5.25 dB of gain must be compensated for if the device is perfectly matched at 860 MHz. This means that a transmission less of 5.25 dB or a VSWR for 11.0:1 must be employed at 470 MHz. The input Z is converted to Y on Smith Chart (I). The point at 860 MHz will intersect the constant conductance line equal to 1.0 (20 m℧) if it is rotated 0.14 λ using a 20 m ℧ (50 Ω) transmission line. After this rotation a capacitive stub or chip capacitor is used to resonate the susceptance at 860 MHz; A capacitive stub or a chip capacitor equal to 16.7 pF can be used, and the result is shown on Smith chart (I). It is interesting to note that the VSWR vs frequency can be adjusted for gain flatness by selecting an optimum Z_O for the capacitive stub. It is also obvious that the locus of impedances at the circuit input can vary between the locus of points defined by using a chip capacitor, and the imaginary axis by using a stub with $Z_O = \infty$. Graph (II) is a plot of these results. Because infinite isolation doesn't exist between the output and input of any transistor, and because the required network is very simple, the input circuit will be optimized empirically. A computed aided circuit will be defined for the output only. It is also indicated that a combination chip capacitor and stub may provide the best results.

The output circuit considerations were first determined using a Smith Chart approach. It must be clearly understood that computer optimization is only as good as the circuit configuration and associated computer instructions.

The approach follows :

Smith Chart (II)

1) The device output impedances are first converted to admittances and plotted as the conjugate (Y load).
2) In order to allow easy collector lead soldering a Zo = 50 Ω, 3 mm long transmission line is used. Since the Smith chart is normalized to 20 m℧ (50 Ω) we can rotate toward the load directly as the chart is configured.
3) Since the balance of the circuit used Yo = 10 m℧ (100 Ω) we next normalize the chart to 10 m℧. 100 Ω transmission line was chosen as a good compromise between physical length requirements and ease of realization on Teflon Glass.

4) The next element, a shorted shunt transmission line less than λ/4 in length reduces the imaginary part by moving each point of admittance along a line of constant conductance. The length was chosen to locate the lowest frequency point (400 MHz) near the real axis so that the locus of points would be more equally distributed about a 2.0 : 1 VSWR circle.

5) The resultant locus of points are then rotated with a 10 m℧ (100 Ω) transmission line to a degree which locates the admittance point of 860 MHz near the line of constant conductance equal to 2.0 on Smith Chart (II). This conductance is exactly equal to 20 m℧ since the chart is normalized to 10 m℧.

6) The final step is to use a parallel resonant circuit which will reduce the imaginary pacts at both the upper and lower frequencies.

The following approach was used to calculate the element values for the antiresonant circuit.

By observation of the smith chart it was decided to place the 460 and 860 MHz points on or just inside the 2.0 : 1 VSWR circle.

It then follows that

$$\text{at } f_1 = 460 \text{ MHz} \qquad W_1C - \frac{1}{W_1L} = -0.4$$

$$\text{at } f_2 = 860 \text{ MHz} \qquad W_2C - \frac{1}{W_2L} = 1{,}7$$

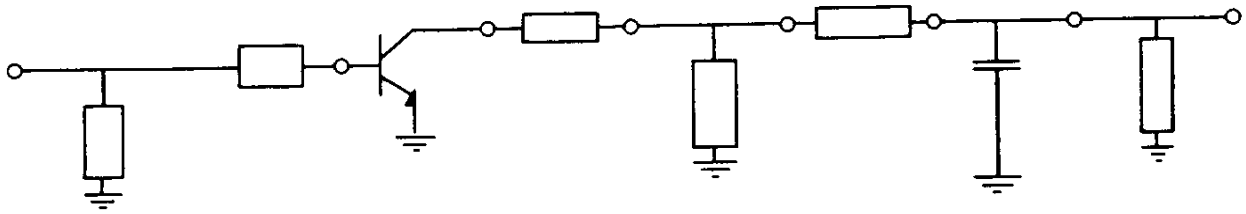
The 2 equations with 2 unknows are solved with the following result.

L = 0,189 nHy
C = 496.11 pFd

since we are normalized to 10 m℧

Lactual = 0.189/.01 nH = 18.9 nHy
Cactual = 496.11 × 0.1 pF = 4.96 pFd

7) The result is normalized to 20 m℧ with the final result shown.



Zo	10 Ω	50 Ω	TPV 596	50 Ω	100 Ω	100 Ω		100 Ω
Calc. Value	45.7 mm	3.78 mm		3 mm	76.1 mm	29,3 mm	4.9 pF	50.4 mm
Empirical Value	8.5 48.8 mm	1.5 mm	Opti-mized Value	3 mm	98.8 mm	39.62	5.5 pF	61.6 mm

Graph (III) shows the various VSWR calculated compared to the theoretical best curve and the actual VSWR measured.

Graph (IV) shows the collector load VSWR for the calculated, optimized, and actual result.

Graph (V) is a plot of the single ended amplifier results taken with a network analyzer. No component losses were considered for the theoretical and optimized analysis. The final circuit was also optimized empirically from 470–860 MHz using a network analyzer.

The following results are a summary of performance, bias conditions circuit configuration and recommended hybrid adaptation.

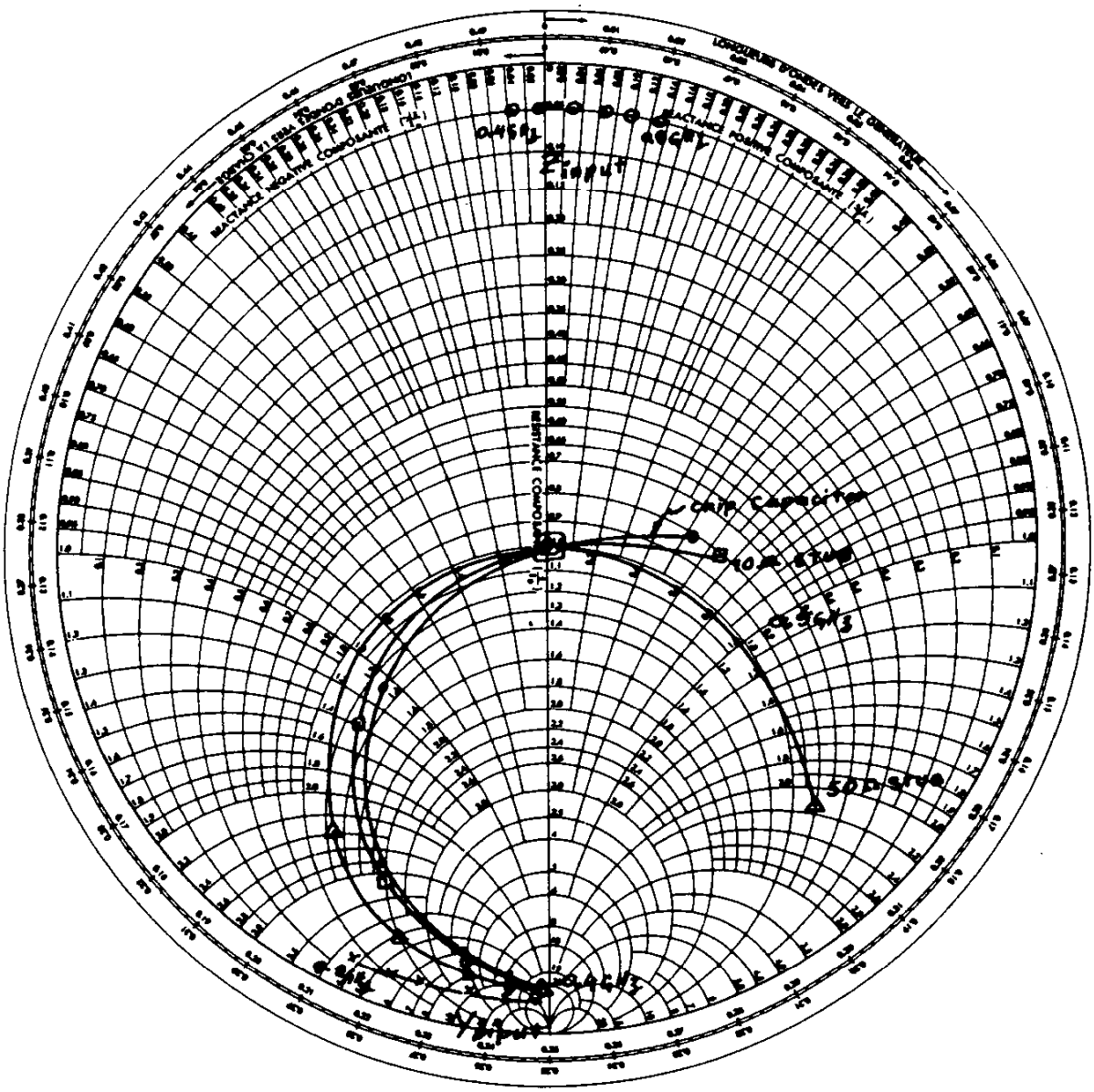
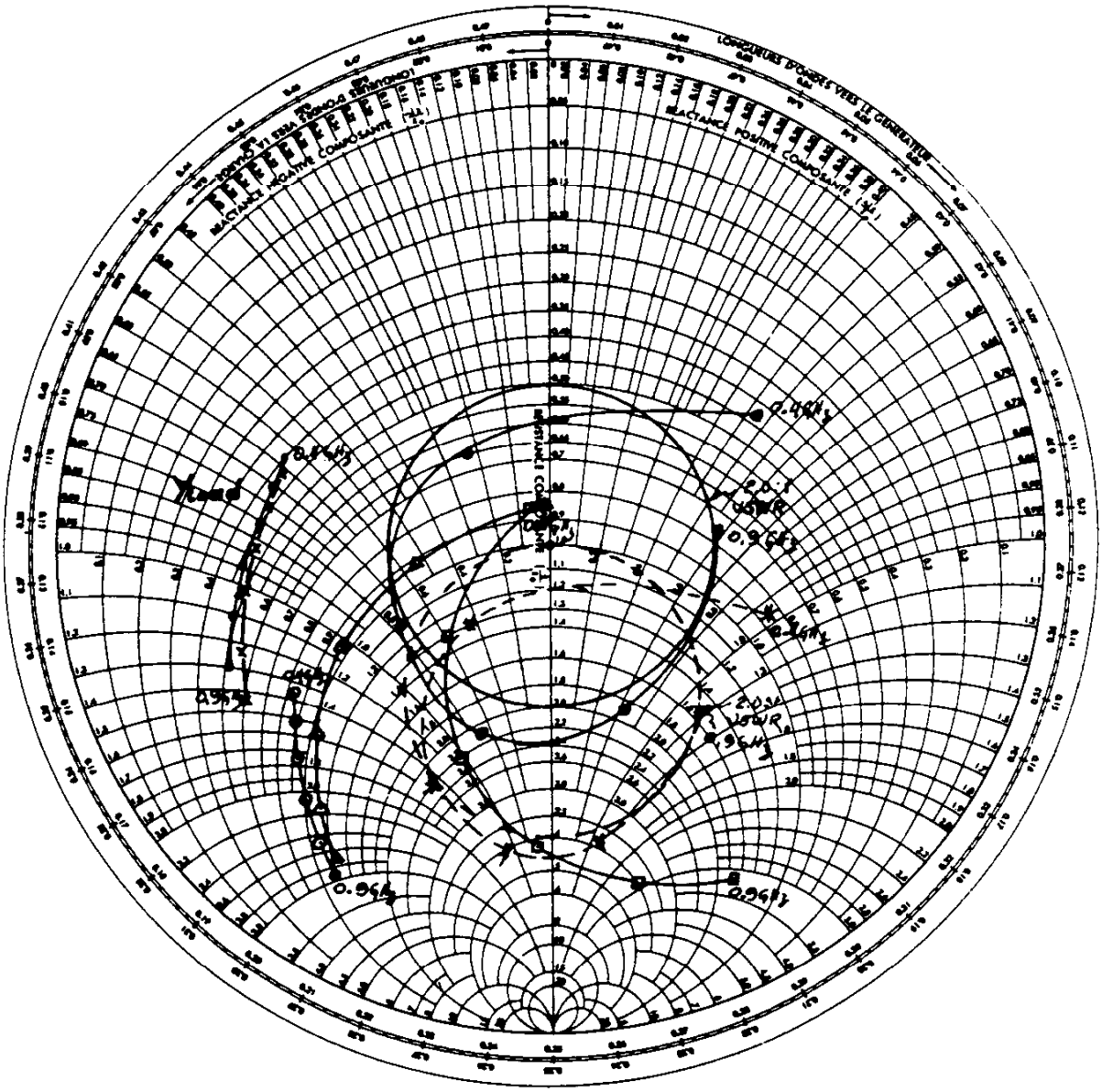


Figure 1. Smith Chart (I)



starting Adm.	
50 Ω rotation	
100 Ω translation	
equiv. shunt Ind.	
100 Ω rotation	
parallel L-C	
final Adm. 50 Ω translation	

Figure 2. Smith Chart (II)

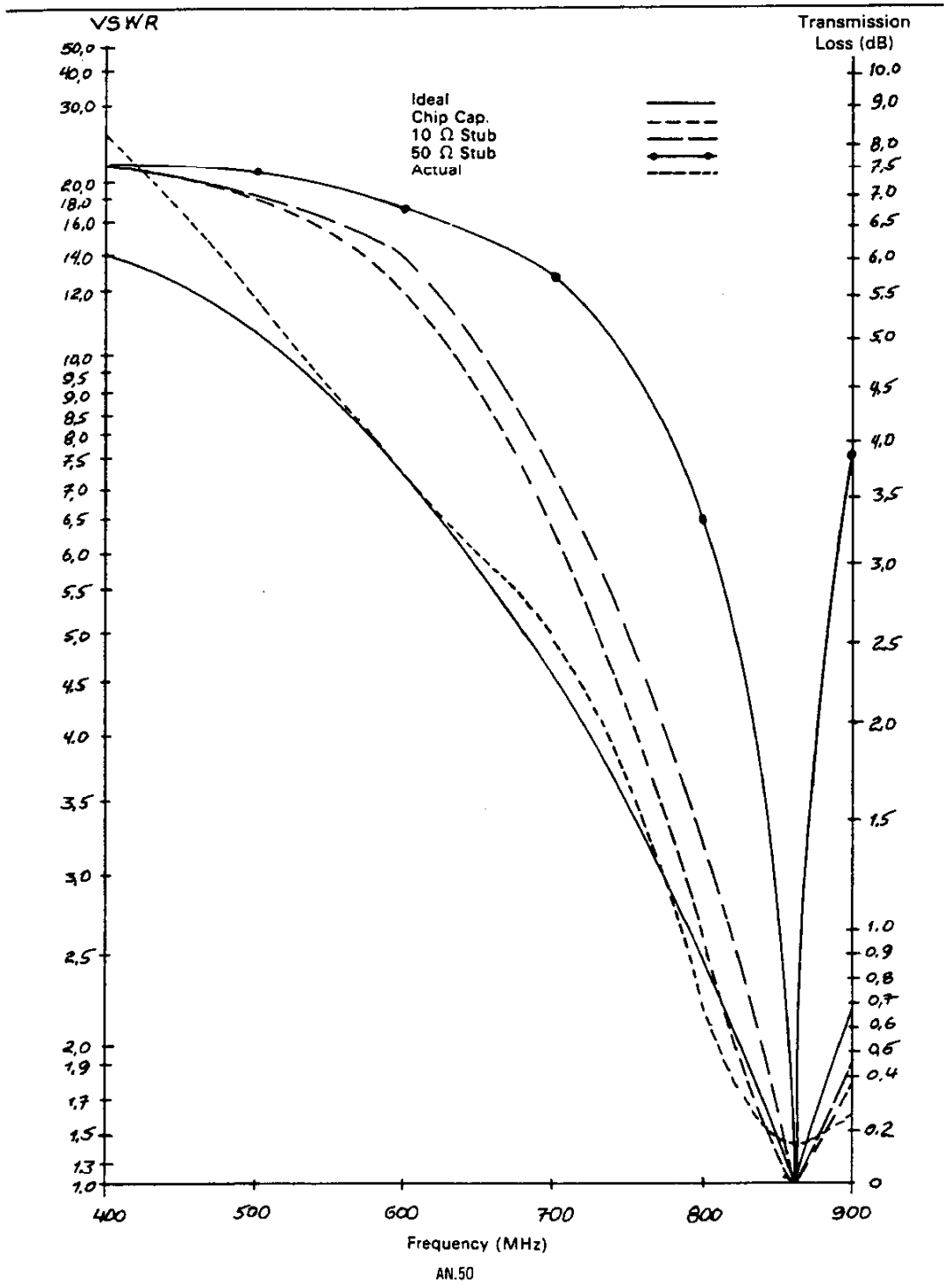


Figure 3. Graph III — VSWR versus Frequency

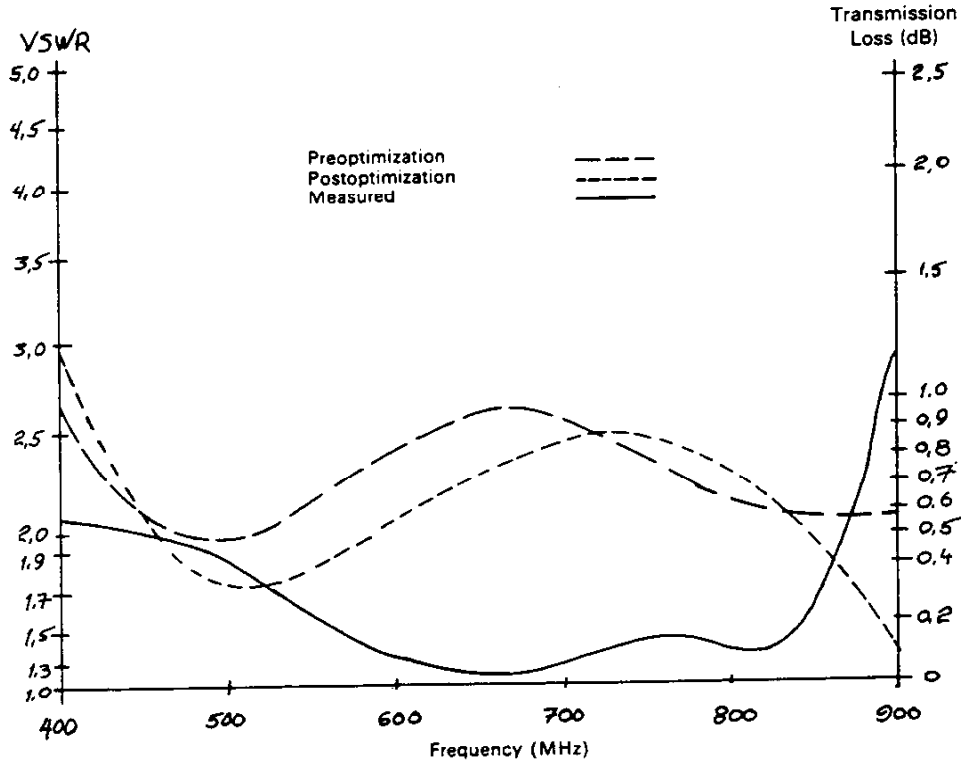


Figure 4. Graph IV — VSWR versus Frequency

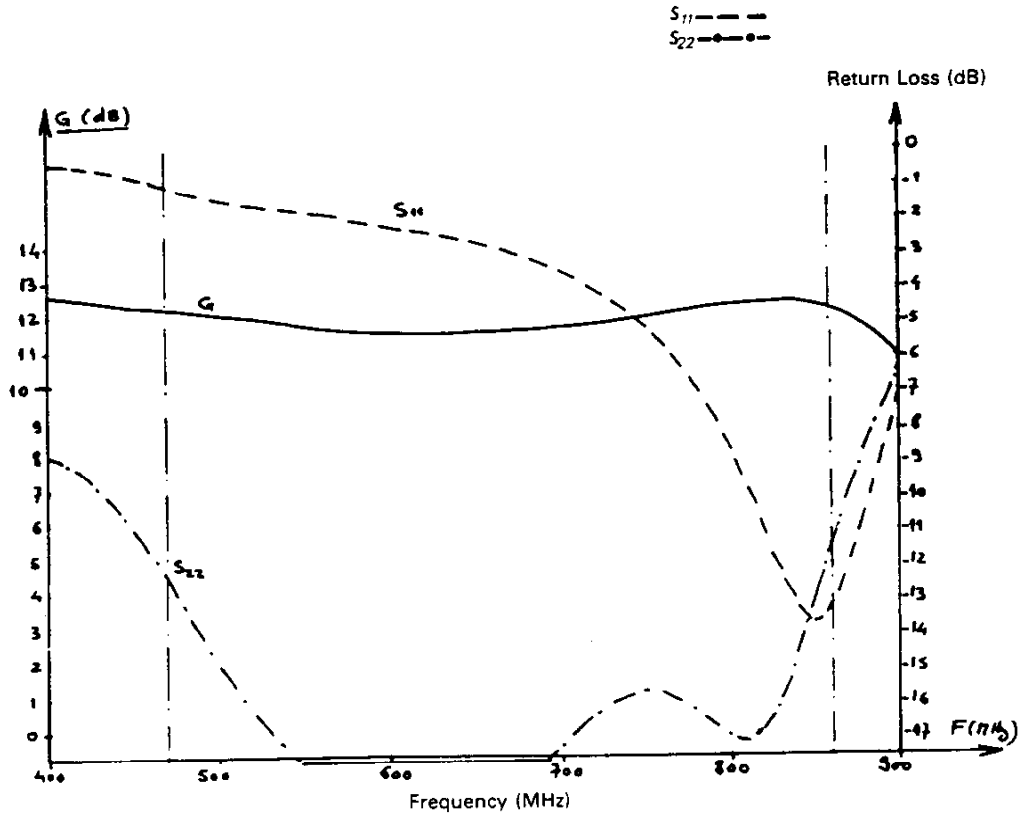
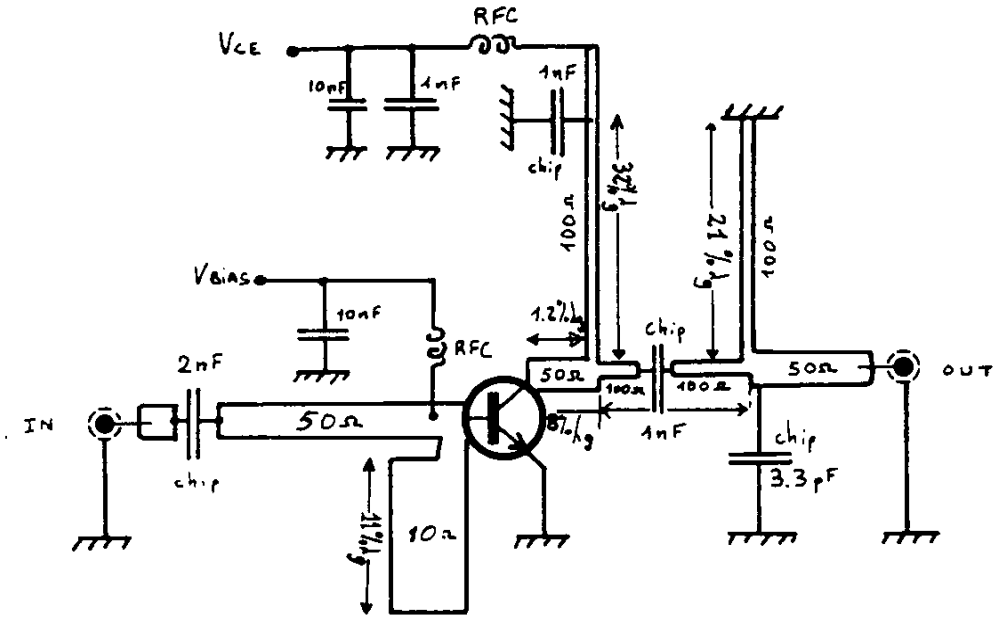


Figure 5. Graph V — TPV596 Amplifier Performance versus Frequency



Class A
V_{CE} = 20 V — I_C = 220 mA
f_o = 860 MHz — WAVELENGTH (λg) at 860 MHz
(material: Glass teflon ϵ_r = 2.55 — 1/16")
Transistor — TPV596

Figure 6. Circuit Diagram for 470–860 MHz Amplifier

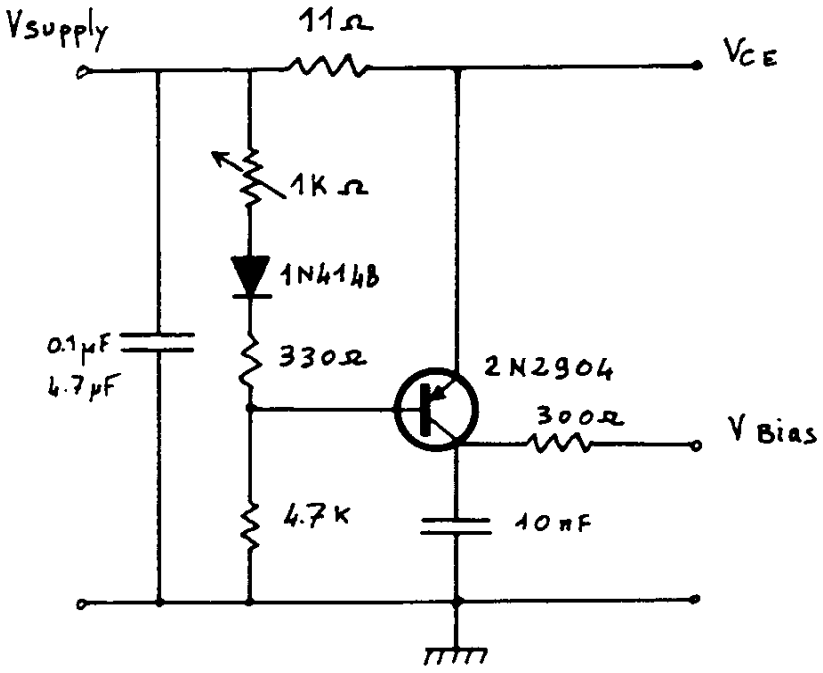


Figure 7. Class A Bias Circuit

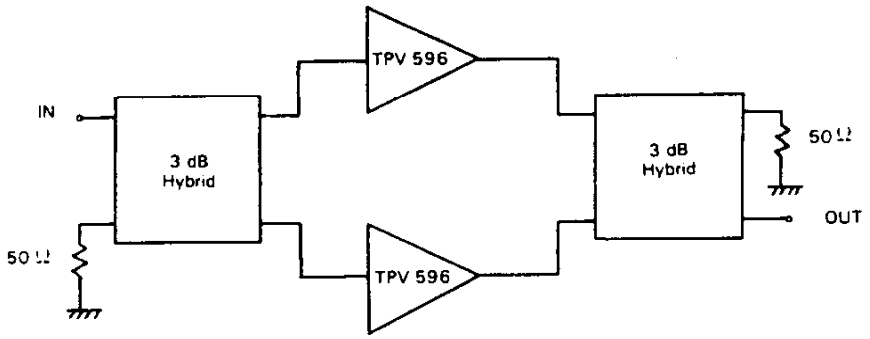
TPV 596 BROADBAND AMPLIFIER

FREQUENCY RANGE	: 470 MHz-860 MHz
POWER OUTPUT AT	: — 60 dB IMD* ≥ 0.5 W
POWER GAIN	: 11.5 ≤ G ≤ 12.7 dB
INPUT RETURN LOSS*	: < — 1 dB
OUTPUT RETURN LOSS	: < — 11 dB
VOLTAGE SUPPLY	: ~ 23 V (V_{CE} = 20 V)
TOTAL CURRENT	: 220 mA

*IMD : Vision : — 8 dB ; Sound carried : — 7 dB ; Side band : — 16 dB

RECOMMENDED CONFIGURATION

*INPUT RETURN LOSS : This amplifier must be used by two connected together with two 3 dB quadrature hybrids to have a balance amplifier with a good input VSWR.



*3 dB - 90° Hybrid coupler from

— ANAREN 10 264-3
— SAGE wireline 3 dB Hybrid 4450 900

IMD VS OUTPUT FOR A SINGLE STAGE
VCE = 20 V-220 mA

F = 860 MHz ; Vision = — 8 dB ; Sound Carrier = — 7 dB ; Sideband = — 16 dB

Pout (W)	0.25 W	0.5 W	1 W
IMD (dB)	— 67 dB	— 61 dB	— 55 dB

F = 860 MHz ; IMD DIN 45004/B
RL = 75 ohms

1.5 V/75 ohms	IMD = — 66 dB
2 V/75 ohms	IMD = — 60 dB

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