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Battery Backup of Self-Refreshing Dynamic Random Access Memory

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INTRODUCTION

In today's information-dependent society, the need for maintaining the integrity of data and program status during a power outage is becoming increasingly important. Even though data files may be stored frequently during a session, in the event of a power failure, any changes since the last save would be lost, and the program would have to initialize and reload the required data. In applications where data loss would be costly in terms of dollars and time spent re-entering data, the use of battery backup circuits in conjunction with robust software can ensure that a power failure would be at most an annoying delay, requiring no user intervention upon the restoration of power.

SELF-REFRESHING DYNAMIC RANDOM ACCESS MEMORY

In the past, the best protection of volatile random access memory (RAM) data against a power loss was provided through the use of static RAMs (SRAMs) in the memory array because of the ease of interfacing with the rest of the system. SRAMs require none of the complex cycle and power consuming refresh circuitry associated with dynamic RAMs (DRAMs), because of their direct addressing and static cell. This has now changed with the introduction of Motorola's newest very low power 512K x 8 DRAM, the MCM5V4800A. Use of self-refreshing DRAMs allows battery backup of an increased memory size at a competitive price.

In addition to the usual methods of DRAM refresh (any read or write cycle, a RAS-only refresh, a CAS before RAS refresh, or a hidden refresh), the MCM5V4800A also incorporates a **self-refresh** operation, previously found only on pseudo-static RAMs (PSRAMs). This self-refresh feature removes the need to have the DRAM control circuitry on the battery backup node, and is expected to be a standard feature on future generations of DRAMs.

The self-refresh operation is entered just as a normal $\overline{CAS}$ before RAS refresh, but $\overline{CAS}$ and $\overline{RAS}$ are held low for a period greater than t_{RASS} min (>100 μs), as shown in Figure 1. After this time, the DRAMs internal timer starts, and a new row is refreshed approximately every 130 μs. When the refresh pulse is generated by the internal timer, the I_{CC} current may peak to 120 mA, but the current I_{CCS} during the self-refresh is guaranteed to be a maximum of 200 μA, as shown in Figure 2.

The MCM5V4800A CMOS processing makes it particularly well suited for use in battery backup systems because of the inherent advantages of CMOS technology: superior noise immunity, faster switching speeds, low standby power dissipation, and a wide operating range.

For battery backup applications, chief among these advantages is the low standby power dissipation. Due to the series connection of P and N channel devices in CMOS designs, current is only drawn during switching. Thus, when the DRAM is in the self-refresh mode, the only current drawn is due to surface, junction, and channel leakage and the operation of the internal refresh timer.

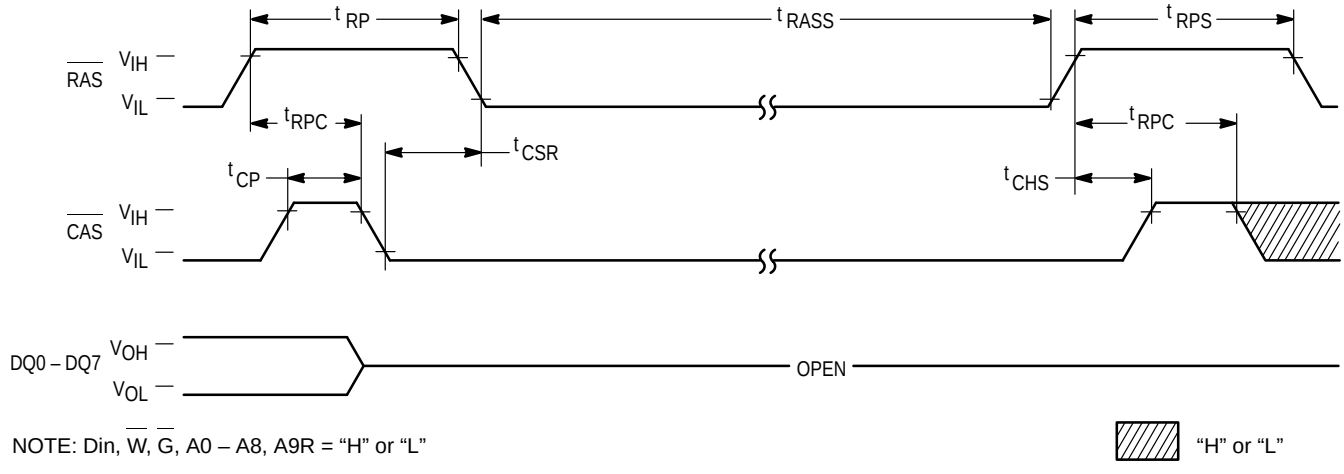

Figure 1. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle for the MCM5V4800A

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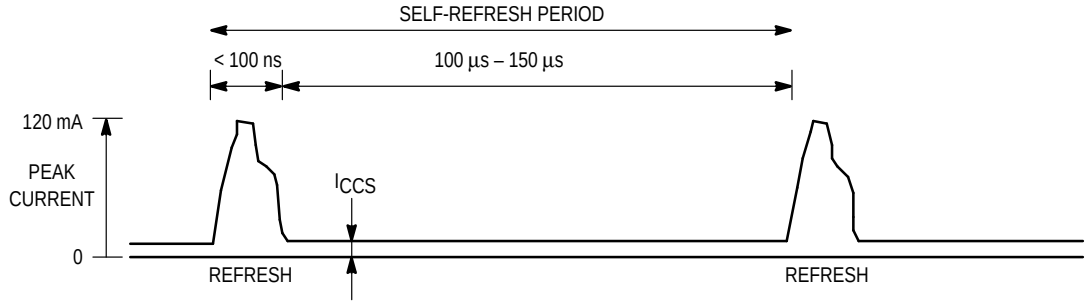

Figure 2. Power Supply Current of the MCM5V4800A During Self-Refresh

Pull-down resistors should be placed on the $\overline{CAS}$ and $\overline{RAS}$ pins to ensure that the DRAM stays in the self-refresh mode during the battery backup period. All other pins (addresses, data inputs/outputs, output enable, and write enable) should use pull-ups or pull-downs so that they do not float, creating undesirable current paths that would shorten battery life and possibly destroy data. (The use of pull-up and pull-down resistors to terminate each transmission line in the memory's bus is a wise practice with many inherent advantages. This topic is discussed in more detail in Motorola Application Notes AN971 and AN973. Although these notes specifically address Fast Static RAM applications, the principals generally can be applied to all volatile memories.)

BATTERY BACK-UP SYSTEM REQUIREMENTS

It is desirable after the occurrence of a power failure to be able to recover after power is restored and resume operation as if only a delay had occurred. This process is called fault recovery. Figure 3 shows the dc power bus for a system utilizing a low power processor, such as Motorola's MC68300 family of processors.

Note that besides the memory array, the processor and power failure detection circuit are also on the battery backup node. The MC68300 family is capable of low power standby necessary for battery backup operation. Having a low power processor greatly simplifies the circuitry and software required for fault recovery, because the processor itself can now store internal registers and keep track of the power state, without the need of external control logic comprising a finite state machine.

BATTERY BACKUP CIRCUIT

The battery backup circuit is one of the key components of the system. Its function is to supply power to the memory array, processor, and power failure detection circuit during a power failure. This is usually accomplished through the use of the trickle charge circuit illustrated in Figure 3, although numerous variations on this circuit exist. System interconnects are not shown in order to clarify the power connections.

In this circuit, diode D1 isolates the battery E1 from all but the system's RAM array, processor, and power failure detection circuit when the dc power supply has failed. The processor and power failure detection circuit must also have the battery backup in order to detect when the main power is restored and to keep track of whether the system is in the battery backup mode or normal operating mode. When the dc power supply is active, diode D2 and current limiting resistor R1 allow a small amount of current to be diverted into recharging the battery. If a non-rechargeable battery is used, resistor R1 can be eliminated. In order to prevent the battery from discharging during a scheduled power shutdown, a switch should be in series with the battery so that the backup circuit is disconnected when the system is deliberately powered off after all critical data has been written to some less volatile storage medium (e.g., floppy disk, hard disk, tape).

POWER FAILURE DETECTION CIRCUIT

The function of the power failure detection circuit is to monitor the ac power source. If the main power fails, this circuit generates an ACFAIL interrupt signal to the processor, which will store its internal status and put the memory in the

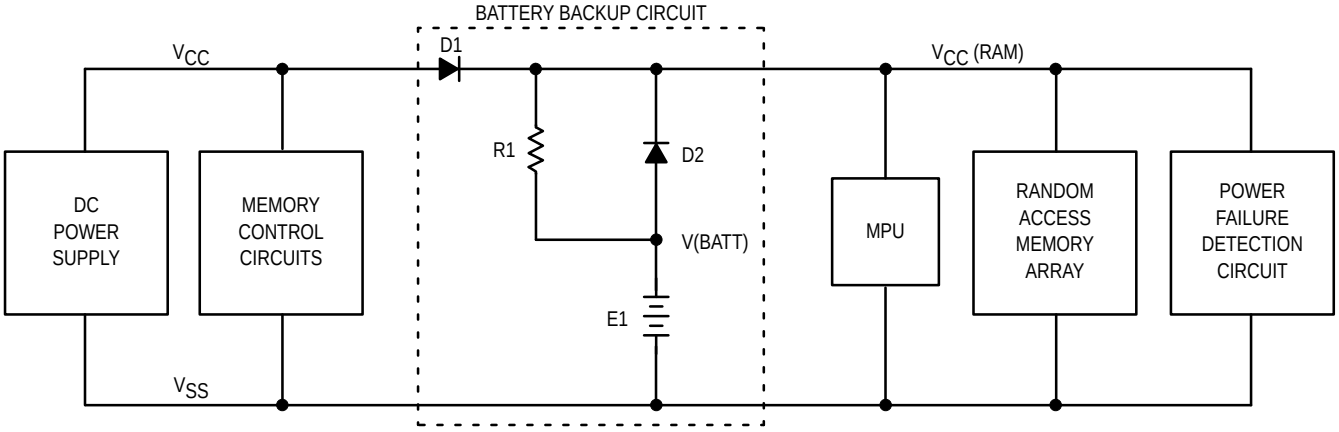

Figure 3. DC Power Bus for Complete System
Showing the Processor, Memory Array, and Power Failure Detection Circuit on the Battery Backup Node

self-refresh mode. Because of the necessary urgency in the event of a power failure, the signal issued to the processor in such an event is a non-maskable interrupt (NMI) of the highest priority.

Just as with the battery backup circuit, a wide variety of circuits exist for power failure detection. A simple power failure detection circuit is shown in Figure 4. It is recommended that the signal from the power supply into the power failure detection circuit be drawn from a separate winding of the transformer than that going to V_{CC}. This will avoid possible interference with the voltage regulation of the system.

In this circuit, the zener diode provides the reference level to the Schmitt trigger inverter, which fires if the ac power drops below a certain threshold. Resistor R1 and the zener reference voltage $V_{(REF)}$ should be chosen so that there is enough margin to the minimum system operating voltage for the power fail code to complete processing before the power loss propagates through the dc power supply, and V_{CC} falls below the system operating voltage. This margin must be greater than the execution time of the power fail code, which is on the order of 15 μs for the code illustrated in the following section. Concerns about this propagation delay can be dispelled through the use of an uninterruptable power supply (UPS), which can provide system power for a short time. An R-C network may also be included in parallel with the zener diode to prevent system shutdown if the ac power source goes down for only a few cycles. The trigger will then only fire if the power fails for more than a time constant. The hysteresis of the Schmitt trigger supplies additional margin.

Since the power failure detection circuit must continue to function during a power failure, its components need to have an operating range from the backup battery voltage to the normal system operating voltage and should also be of low power to minimize battery drain. Motorola's high performance Schmitt trigger inverter, the MC74HC9014, fulfills these requirements. If a high-to-low transition is required for the processor to begin the battery backup sequence, then a non-inverting Schmitt trigger should be used, such as the MC74HC9015.

SOFTWARE CONSIDERATIONS

The system's operating software must include code to accomplish the fault recovery process. From the standpoint of the processor, it is essential to save enough information to be able to return to the same point in program execution when power is restored. With the advent of components with low power standby modes, not only can essential data be saved, but also all variables and parameters may be recovered on return to normal operation.

Upon receipt of the ACFAIL signal from the power failure detection circuit, the processor will prepare the system for the battery backup operation. A low power processor from the MC68300 family will store its registers internally, send the memory array into the self-refresh mode, and make note that the system is now in the standby mode. Additional power can be saved by disabling circuitry that will be unused during the backup operation, such as the periodic interrupt timer, voltage controlled oscillator (VCO), and phase-locked loop (PLL).

Upon restoration of power, the ACFAIL signal is reset and the processor begins the fault recovery process. After the internal status of the processor is restored and the power to the external logic (especially the memory control circuits) reaches an operational level, the memory array can then return to the normal operating state. It is prudent to perform a refresh of the memory array as a part of the fault recovery process in order to ensure that no refresh parameters are violated.

As system complexity grows (for example when an operating system is being used), more complex measures must be taken to ensure proper fault recovery than if all software is written in assembly language. When the ACFAIL is detected, the operating system must shut down active processes and close files in an orderly fashion for full recovery after power is restored. Likewise, systems that implement some functions of operating systems like multitasking and scheduling, or access files on permanent storage devices, must close those processes or files to ensure proper recovery after the fault is repaired. The shutdown software must also keep a record of the status of the processes and files before the fault so that

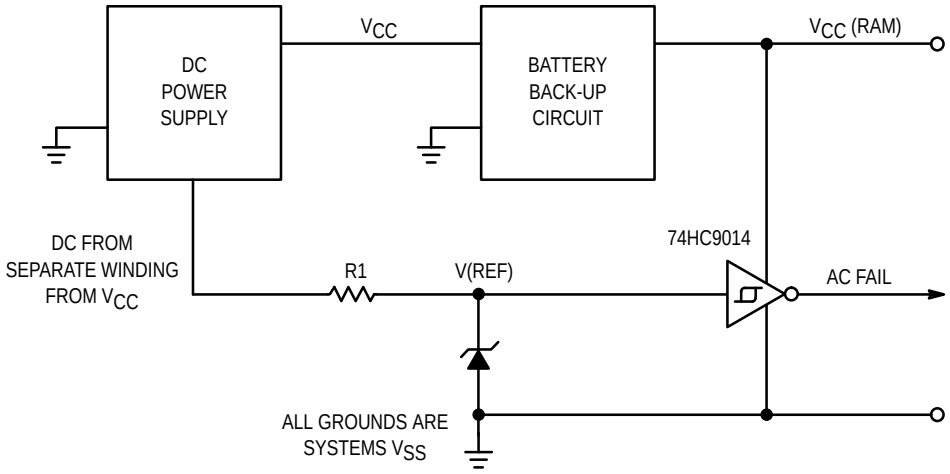

Figure 4. A Simple Power Failure Detection Circuit
(Note that the Schmitt trigger is also powered by the backup battery when the main power is down.)

they can be reopened on recovery. Consideration of the software or firmware necessary for such tasks is beyond the scope of this application note, but the user must take them into account nonetheless.

The code to perform a simple fault recovery for the MC68xxx family of processors follows. On reception of a power failure interrupt, the processor should execute, at a minimum, code similar to the following:

```
MOVEM.L     A0–A7,D0–D7,FAILREGS     Save regular registers and supervisor stack pointer.
                                     Note that the number of registers may vary
                                     depending on the type of processor being used.
MOVE.W      SR,FAILSR                Save status register.
MOVE.L      USP,A0                   Get user stack pointer
MOVE.L      A0,FAILUSP               and now save it.
RESET                                Reset all system peripherals.
STOP                                 The CPU is now waiting to be reset
                                     for the duration of the power failure.
```

When the ac fault disappears, the fault recovery routine should contain code at the end of the routine similar to the following:

```
TAS         FAILSAVE                 Get value of state register and clear it through
                                     an indivisible read-modify-write cycle, while
                                     setting the Z bit of the CCR.
BEQ         JMP                      Skip if OK.
MOVE.L      FAILUSP,A0               Load user stack pointer
MOVE.L      A0,USP                   and put in register.
MOVE.W      FAILSR,SR                Reload status register.
MOVEM.L     FAILREGS,A0–A7,D0–D7     Reloading the registers causes the CPU to
RTE                                  reload the stack frame that was saved on the
                                     power fail interrupt; program execution
                                     continues as if no fault occurred.
JMP         CLR.W  FAILSAVE          Clear semaphore in state register and continue
                                     power up code.
```

Note that the above code is generic for the MC68xxx family, and the number of internal status registers may vary. A low power processor from the MC68300 family can greatly simplify this code and shorten execution time, since it can store the status registers internally and initiate a low power stop.

SUMMARY

When critical data is being stored in a volatile RAM array, it is important to retain that data in the event of a power failure by having the RAM powered by a backup battery. It is also desirable after the occurrence of a power failure to be able to recover after power is restored through the process of fault recovery. From the standpoint of the processor, it is essential to save enough information to be able to return to the same point in program execution when power is restored. With the advent of self-refreshing DRAMs and processors with low power standby, not only can essential data be saved, but also all variables and parameters can be recovered, and the system returned to normal operation.

For a system to accomplish a fault recovery, additional circuitry is required beyond that of a system with no backup. A battery backup circuit switches between the main power and the battery; a power failure detection circuit senses a power loss and initiates the interrupt to the processor sending the system into the standby mode. The power failure detection circuit and processor must also be powered by the backup battery during a fault.

A wide variety of circuits exist for these additional requirements, and this application note has touched on only a few. As battery backup systems become more common, vendors are responding by including many of these requirements in their systems. For example, the VME bus specification defines an implementation of power failure detection. In the event that the power supply used in an application does not include the circuitry for battery backup operation, the required components can be obtained through Motorola.

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