AN1235

A Set Top Closed-Caption Decoder

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INTRODUCTION

Designed primarily for the hearing impaired, closed captioning is applicable to many other applications. While the hearing impaired may benefit the most from the closed caption service, viewers without hearing problems can also benefit. The ability to read and hear the program or movie dialog will help both the young and the illiterate learn to read. Just being able to have the service available in noisy surroundings such as sporting events is attractive. The service is also expected to provide dual language capability in the near future. This feature can increase the literacy of the individual by providing a method for studying a foreign language. Being able to read in one language and hear the equivalent in a second language is an attractive method for learning a second language.

HISTORY

The present closed captioning technology has its beginnings in 1971. The National Bureau of Standards was studying the possibility of encoding real time clock information on line 1 of the vertical blanking interval (VBI). Engineers at the American Broadcasting Company recognized the technology as a way of transmitting closed captioning. ABC captioned an episode of “The Mod Squad” and showed it to a group of hearing impaired people near the end of 1971. The reaction of the test audience was so enthusiastic the NAB (National Association of Broadcasters) began studying ways of establishing a national closed captioning system. The Health Education and Welfare department provided funding for the development of encoders for the broadcast industry and low cost decoders for use by viewers while PBS provided the initial expertise for the design of this equipment.

In 1976 the Federal Communications Commission (FCC) set aside line 21, field 1 of the VBI specifically for closed captioning. ABC, NBC, and PBS agreed to participate in the closed captioning service. The National Captioning Institute (NCI) was created to provided an organization to produce captions and promote the service. In 1980 the closed captioning for the hearing impaired officially made its debut as a nationwide service.

Although it was hoped public pressure would drive the development of the technology, the service languished until Congress, after many hearings and the assurance that cost would be small, passed the Television Decoder Circuitry Act of 1990. This legislation requires all TVs sold after July of 1993 that have screens larger than 13 inches have circuitry for decoding line 21 closed captioning.

EEG Enterprises, a long time pioneer in the closed caption industry, partnered with Motorola to produce the MC144143 Closed Caption Decoder IC. The device provides an economical solution for decoding and displaying closed captioning on TV. The MC144143 may be designed into existing circuitry to produce TVs and VCRs capable of decoding and displaying closed caption data or it may be used to build a stand alone decoder for TVs presently in use.

HOW CLOSED CAPTIONING WORKS

Line 21 of field 1 of the NTSC VBI contains the closed caption information. The structure of the line 21 is shown in Figure 1. The information contained in line 21 contains not only raw data but also timing information. A “color burst” is present on the “back porch” of the horizontal sync pulse and seven cycles of the 503.5 kHz “run–in clock” burst is transmitted following the color burst information. Immediately following the run–in clock is a 4.15 µs interval for stabilizing of the data collection clock and locking and with the run–in clock burst. Following this “timing” interval is a start bit followed by 16 bits of digital information transmitted as two 8–bit words formatted per the USA Standard Code of Information Interchange (USASCII;x3.4–1967) with odd parity. The clock rate of 503.5 kHz is 32 times the horizontal sweep frequency.

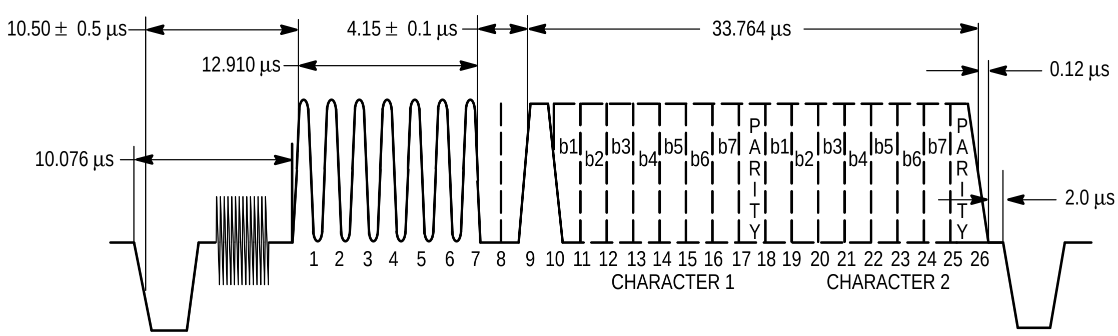


Figure 1. NTSC Line 21 Timing

MOTOROLA

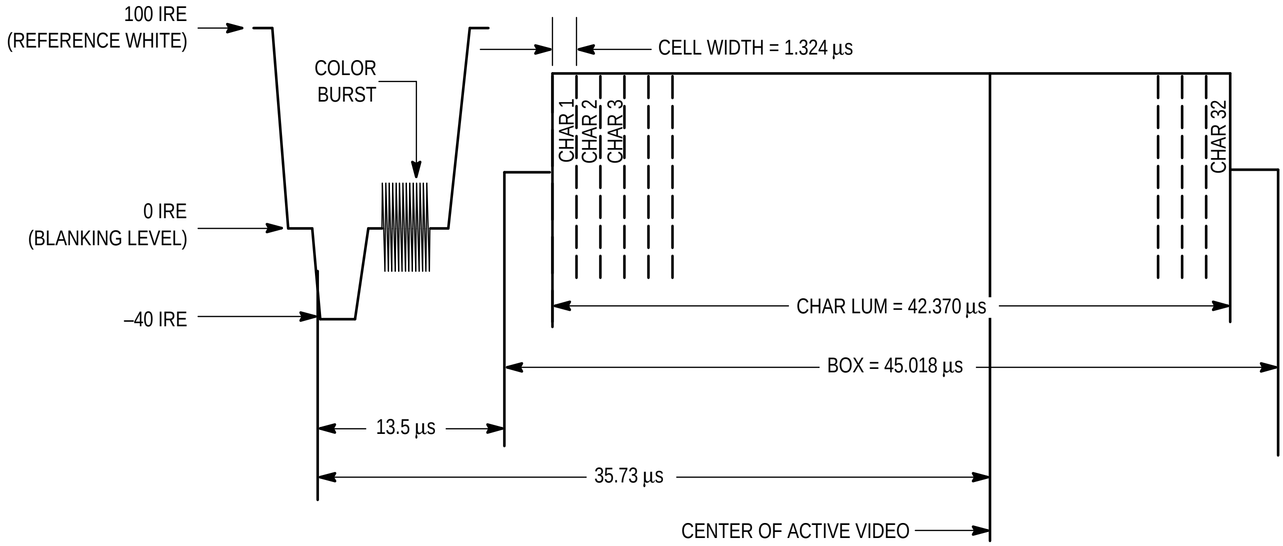


Figure 2. Character Box Timing

The data format chosen for the closed caption system is a modified ASCII table. The normal 7–bit ASCII table defines two types of characters, non–printing control characters used for command execution and printable text characters. The non–printing control codes have been expanded to include additional commands necessary for the smooth operation of the system. The asterisk, back slash, up carat, underline, apostrophe, brackets, and tilde were replaced with accented foreign characters to facilitate the display of non–English languages. In addition, 15 additional characters were defined by special character commands. Refer to the MC144143 data sheet for a description of these characters and the control codes used for positioning, text manipulation, and processor instructions.

THE MC144143

The heart of the Closed Caption Decoder discussed here is the MC144143. This device contains all of the circuitry necessary for detecting line 21, slicing and decoding the digital data from line 21, and organizing the data into a format presentable for NTSC TV display. It contains a character ROM containing all of the modified ASCII characters defined by the FCC specification for closed captioning. The display is a character ROM based type with the ability to place text anywhere on the TV screen as defined by the line 21 control codes.

The MC144143 is a line–21 closed–caption decoder intended for use in television receivers or set–top decoders conforming to the NTSC standard. The capability for processing and displaying all of the latest standard line–21 closed–caption format transmissions is included. The device requires a closed–caption encoded composite video signal, a horizontal sync signal, and an external keyer to produce captioned video. RGB outputs are provided, along with a luminance and a box signal, allowing simple interface to both color and black–and–white TV receivers.

SECTION 1

The simplified decoder operation is shown in Figure 3. The MC144143 decoder circuitry along with an analog switch (video mux) is sufficient to decode the line 21 information and integrate the information into the TV display. The MC144143 decodes the line 21 information and from this information determines what text will be displayed and where on the screen it will be displayed. The output of the decoder chip is a luminance (or RGB) video signal representing only that part of the display where the text is to be displayed. The “BOX” signal is a control signal which tells the analog switch when text is to be displayed.

The video signal is routed to both the MC144143 and one input of the analog switch. Unless text information is present (indicated by the BOX output), the video signal will be passed through the analog switch unaffected. When the BOX signal indicates the presence of text information, the analog switch (video mux) selects the “LUM” signal (luminescence or brightness), from the MC144143 and passes this signal to the output. This switching always occurs within the line. Normal video is presented at the output of the analog switch before any text appears on a line and after the text ends on that line. This is to ensure that sync and color burst information are unaffected by the decoding and display process.

A typical application circuit is shown in Figure 4. The values shown on the schematic are the recommended values for most applications. (For specific implementations and for loop filter calculations, refer to the MC144143 data sheet.) The video buffer may be of any design capable of driving a 470 ohm load with voltage gain of one. The video line driver design depends on the particular application (output impedance, output voltage, etc.) for its design and may or may not include DC restoration as one of its features. The analog switch may be as simple as a pair of DMOS transistors or a complete analog switch such as the MC74HC4053.

Display storage is accomplished with an on–chip RAM. A modified ASCII character set, which includes several non–English characters, is decoded by an on–chip ROM. An on–screen character appears as a white or colored dot matrix on a black background.

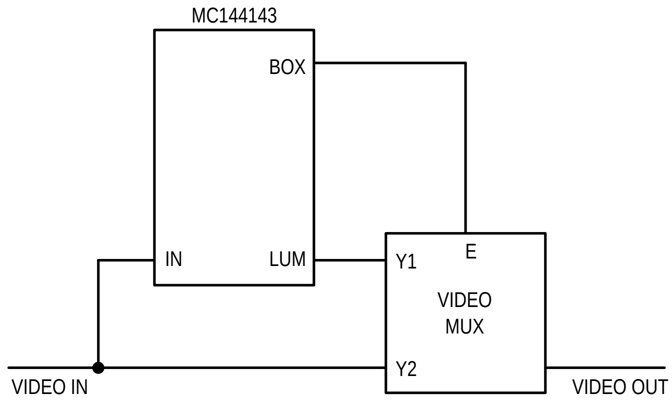
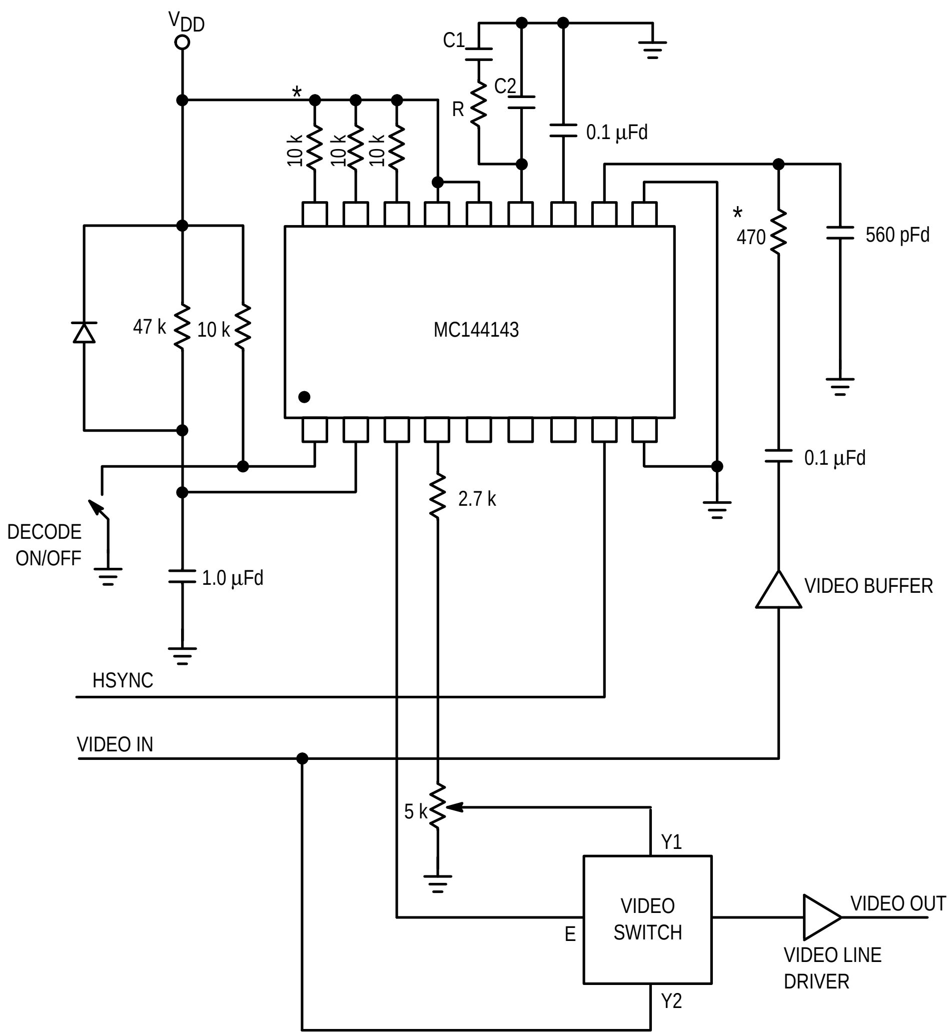


Figure 3. Simplified Decoder



* Decouple V_{DD} to V_{SS} with 0.1 µFd low ESR caps between pins 14, 15 and 9, 10 keeping leads as short as possible.

Figure 4. Typical Application Circuit

Captions (video–related information) can be up to four rows appearing anywhere on the screen and can be displayed in two modes: roll–up or pop–on. With roll–up captions, the row scrolls up and new information appears at the bottom row each time a carriage return is received. Pop–on captions work with two memories. One memory is displayed while the other is used to accumulate new data. A special command causes the information to be exchanged in the two memories, thus causing the entire caption to appear at once.

When text (non–video related information) is displayed, the rows contain a maximum of 32 characters over a black box which overwrites the screen. Eight rows of characters are displayed in the text mode.

An on–chip processor controls the manipulation of data for storage and display. Also controlled are the loading, addressing, and clearing of the display RAM. The processor transfers the data received to the RAM during scan lines 21 through 42. The operation of the display RAM, character ROM, and output logic circuits are controlled during scan lines 43 through 237. Several functions of the MC144143 are controlled via a port which may be configured to be serial or parallel.

Characters are displayed as white or colored, dot–matrix characters on a black background. The characters are described by a 6–by–9 dot pattern within a character cell which is 8 dots wide by 13 dots high. This provides a one–dot border of black around each character and provision for one row for underline, offset by a row of black, between the character and the bottom edge of the cell. Character luminance has normally been set at 90 IRE units and the surrounding black box at 10 IRE units.

The Character ROM contains a ***dot–matrix*** pattern of each character. Each ***dot*** from the character ROM represents a single picture element or ‘pixel’ and each picture ‘dot’ is made up of a square of four pixels. Pixels 1 and 2 are generated during field one and pixels 3 and 4 during field two. Alternate rows and columns are read out of each field to produce an interleaved and rounded character. A display row contains a maximum of 32 characters plus a leading and trailing blank box, each a character cell in width, making the overall width of a display row 34 x 8 = 272 dots. Successive display rows are butted together, so that the total display is 195 dots high.

The black box (34 character cells wide by 195 dots high) results in a box size of 45.018 µs in width by 195 TV scan lines in height. A scan line is two adjacent picture lines. The first line is generated during field one and the second line is generated during field two. When centered in the video display, this box starts 13.5 µs after the leading edge of H in scan line 43 and extends to scan line 237. This places the display approximately within the safe title area for NTSC receivers. Character width is 42.37 µs and is approximately centered on the screen, resulting in a leading and trailing 1.32 µs black border.

For additional information on line 21 programming, loop filter calculations, EMI (electromagnetic interference) suppressions, and other MC144143 features, see the MC144143 data sheet.

THE SET TOP CONVERTER OPERATION

The closed caption set top decoder (Figure 6) is composed of two sections. The decoder section, composed of the MC144143, MC555, MC74HC4053, and the MC14576 with their associated circuitry. The decoder section accepts a composite NTSC signal input, decodes the line 21 information, mixes the normal composite video with the displayable closed caption text and buffers the output for monitor input or RF modulator input. The second section contains the MC1374 RF Modulator IC and its associated circuitry.

The MC144143 decoder circuit is the same as shown in the MC144143 data sheet. Of particular importance is the network tied to pin 13 and that associated with pin 11. The input circuitry of pin 11 of the MC144143 is a low pass filter for minimizing noise to the input clamp circuit and the network connected to pin 13 is the PLL loop filter network. Neither of these circuits should be modified without a good understanding of clamp circuits and PLL operation (see loop filter calculation section of the MC144143 data sheet).

The bandwidth of line 21 is limited to approximately 600 kHz. The 470 ohm resistor and the 560 pF capacitor connected to pin 11 of the MC144143 form a 600 kHz low pass filter. For most applications this is adequate. Some measure of improvement in noise immunity can be achieved by using a π type LC filter adjusted for 470 ohms impedance, but the cost of the components usually does not justify the improvement in performance. The input of the MC144143 is itself enough noise resistant for most applications.

The network connected to pin 13 of the MC144143 determines how the VCO within the decoder IC will respond to the video input signal. The VCO in the decoder IC must be able to handle a wide range of signal conditions. At one extreme is the weak or “snowy” picture. The decoder must be able to decode line 21 down to a condition where the picture borders on the unwatchable. In addition the text must be presented with a minimum of “jitter”. At the other extreme is the necessity of decoding “bad” tapes; those from poor recordings or from rental stores where the tape has been stretched from repeated playing.

When presented with a weak signal, the VCO within the PLL circuitry of the MC144143 will be continually bombarded with noise which will tend to cause the VCO to bounce around. This is corrected by reducing the value of the resistance in the loop filter while increasing the capacitance in series with this resistance. This must be adjusted along a precise curve dictated by a set of complex equations (see loop filter calculation section of the MC144143 data sheet). Although these values can be arrived at empirically, it is time consuming and requires sophisticated testing equipment. Acceptable values for reasonable jitter with weak signals are 3.3K ohms to 4.7K ohms for R24 with a value for C5 of about 0.1 µF. The usual value for C6 is 3300 pF.

The disadvantage of using the lower resistance values (R24 = 3.3K ohms) is stability problems encountered when using a VCR to display old or poorly recorded tapes. This difficulty is traceable to the design of the VCR recording mechanism. To record and playback video information, the VCR must be able to record one field as a single continuous track. This is done by spinning the record/playback head and wrapping the tape around the head mechanism so that the head is in contact with the tape for about 180 degrees of rotation. The information is then recorded as a diagonal strip of information on the tape. Two or more heads are mounted to the rotating mechanism and the signal switched between the heads so that one records/plays back the even fields and the other the odd fields. Head switching occurs normally in the last few lines of a field; usually 5 to 10 lines before the end of the field but may occur on some recordings during the VBI (vertical blanking interval).

Herein lies the problem. As the tape is repeatedly played the tape will stretch. This is aggravated during the head switch line where the stretching causes the line containing the head switch "transient" to be longer. Additionally, poor equipment or misadjustment can cause excessive head switch "transients". Errors due to tape stretching and head switch "transients" of more than 15 µs can be observed in the normally 64 µs line length.

The error introduced by the head switch is referred to as a "transient" because it occurs only once per field; at the point of head switching. The VCO sees this transient as a jerk which causes the frequency to jump. The length of time necessary to return to its correct frequency is determined by the values chosen for the loop filter. For low values of R (3.3K or less), the VCO in the MC144143 may not be able to return to its correct operating frequency before line 21 is encountered. If its frequency is not correct, it will not decode the line 21 data. Values for R of 6.8K to 8.2K or higher with values of C5 less than 0.082 µF will ensure that nearly all tapes will be decoded, however, excessive jitter may result when very weak and/or noisy signals are decoded.

Pin 8 of the MC144143 performs a unique function. The frequency control for the decoder IC is a VCO in a PLL type of circuit. The reference frequency for the PLL operation is derived from the sync stripped from the composite video by the sync detector circuits within the MC144143. As long as composite video is provided, the VCO will be locked to the horizontal sync signal.

During normal operation, a video signal will not always be available. When changing TV channels or when the VCR is not on, no video will appear at the input of the decoder. In these cases, the VCO would drift due to lack of reference input. The designers of the chip realized this and added an additional input for a second reference frequency; this is pin 8.

Pin 8 does not function the same as the reference signal derived from the video signal. Its purpose is only to keep the VCO within a range that will allow the PLL circuitry to "pull–in" and lock to the horizontal sync of the composite video signal. Normally this signal is derived from the sweep circuits of the TV receiver. In the set top closed caption decoder circuit we use a 555 timer circuit to generate a 15 kHz signal which functions as a frequency control when a video signal is absent.

The question invariably arises, "Why not use the output of the VCR or the video signal itself as an input for this pin?" The answer lies with the previous discussion of the VCR operation and the effects of the head switch. The video signal can be decoded and the sync stripped off and used as an input to pin 8 but the circuitry would be at least as complicated as the 555 circuitry and with VCR operation, the head switch results in an excessive amount of jitter as the VCO is jerked around during the switch.

Q2 is a simple video buffer and 600 kHz filter for the video input to the MC144143. An integrated circuit current buffer could be used; however, none can approach the cost of a simple emitter circuit using the venerable 2N3904 (or equivalent). The filter itself is the two components R18 and C10 whose function was discussed previously. As pointed out in the discussion of the MC144143, a more sophisticated filter such as an LC filter could be used but probably wouldn't improve performance enough to offset the added cost.

The MC74HC4053 is four single pole double throw analog switches. The speed of this device is adequate for pixel by pixel switching of NTSC generated video. Although only one of the four switches is needed and the required operation could be obtained from discrete DMOS FETs, it is still probably the cheapest. The "BOX" output of the MC144143 is used to control the switch and determines whether the decoded closed caption text or normal video appears at the output of the '4053. This switching is done intraline so that normal video sync and color burst information are not interrupted by the decoder. Normal video is always present at the beginning of every line and at the end of every line. Closed caption text is present only within the line and only during the lines chosen during the encoding. The position of the text is always predetermined at the time of encoding of the video signal.

U3, the MC14576C, is a dual video amplifier. The on–chip gain–selling resistors set the noninverting gain of the MC14576C to 6 db. The (A) section is used as a buffer/video clamp. The (B) section is a line driver output for monitor connection. The extra circuitry connected to the (A) section is necessary because of the nature of the video signal. The composite video signal is a non–symmetrical voltage. The positive peaks of the waveform do not equal the negative peaks. While this is necessary to convey the video information, it does pose a problem that must be addressed. The dc level of the video waveform is continually changing. If some method is not used (i.e., a dc restoration circuit for example), the intensity of the closed caption text will vary line by line and be determined by the background brightness. Q1 and associated circuitry reduce this condition to an acceptable minimum.

Input video from J1 is passed to pin 3 of U3A by the video switch U4. C3 will charge through R3 causing the voltage on pin 2 of U3A to rise. Since this pin is the inverting input of the op amp, the output voltage, pin 1, will fall. When this voltage drops to approximately 0.7 V, Q1 is turned on clamping the output of U3A and preventing the voltage from dropping any lower. The video input at pin 3 of U3A will result in an output where clamping occurs at the negative sync tips. This maintains the dc value essentially constant, varying only minimally during the VBI.

THE RF MODULATOR

If viewing on a standard TV is to be expected, a RF modulator must be incorporated into the circuitry. This device accepts the output of the decoder plus audio obtained from a separate source (such as the audio output of a VCR) and produces a TV signal (usually on channel 3 or 4). The PC board layout provides a space which may be allocated for RF modulator circuitry. The RF modulator chosen may be a general purpose stand alone type, a PCB mountable module, or an IC such as the MC1374. An optional audio amplifier (shown in Figure 5) may be incorporated where the standard VCR audio output is insufficient to drive the audio input of the RF modulator chosen.

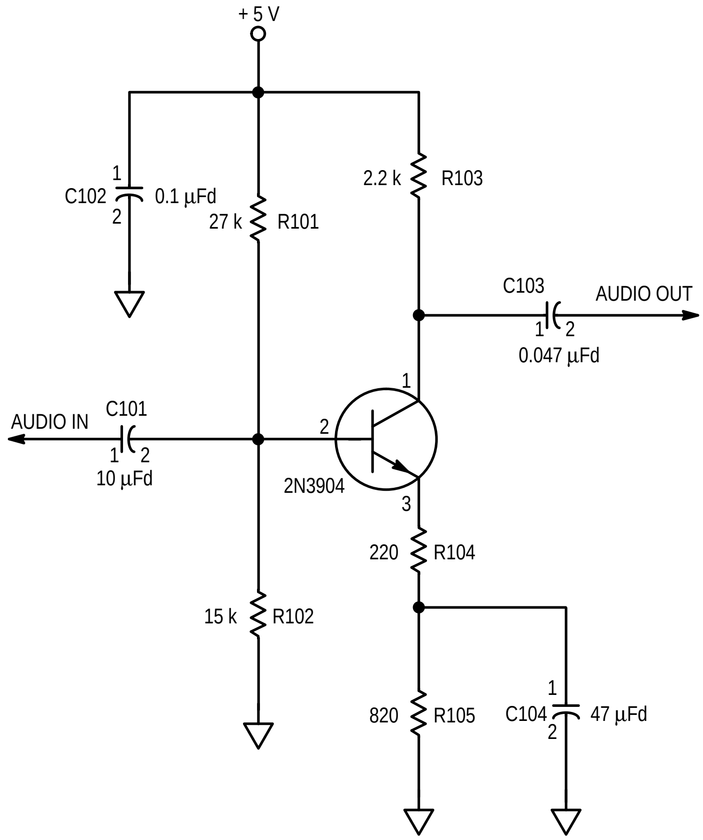


Figure 5. Optional Audio Amplifier

The MC1374 and associated circuitry can form the RF modulator for the decoder. Video information from the decoder and audio from the VCR modulate the carrier generated by the MC1374 to produce a TV signal receivable on channel 3 or 4 by a NTSC television receiver. For a complete description of the MC1374 operation, please refer to the data sheet for the MC1374 and/or the AN829 application note.

POWER SUPPLY

Power for the set–top–decoder is obtained from any convenient AC source whose RMS value is between 10 Vac and 20 Vac. The AC is rectified by diode D4 and filtered by the electrolytic capacitor C24. An inexpensive MC7805 voltage regulator is used to obtain the necessary 5 V supply voltage. Additional filtering is provided by the electrolytic capacitor C23.

In cases where weak channel reception of channel 10 is expected. EMI may occur due to the digital nature of the MC144143. A ferrite bead (RFB) has been placed in series with the V_{DD} pins along with a 0.1 µFd capacitor to suppress this EMI. This is sufficient for the PC board layout shown at the end of this document, but if a double sided or single sided PC board design without ground plane is contemplated, it is recommended the EMI information in the MC144143 data sheet be referred to prior to design.

REFERENCES

1. “Closed Caption Decoder”, Motorola Data Sheet MC144143/D.
2. “Color TV Modulator with Sound”, Motorola Data Sheet MC1374/D.
3. “Triple 2–Channel Analog Multiplexer/Demultiplexer”, Motorola Data Sheet MC74HC4053/D.
4. “Dual Video Amp for 5 V Operation – “C” Version”, Motorola Data Sheet MC14576C/D.
5. “Timing Circuit,” Motorola Data Sheet MC1455D/D.
6. “Fixed–Voltage, 3–Terminal Regulator for Positive Polarity Power Supplies”, Motorola Data Sheet MC7805/D.

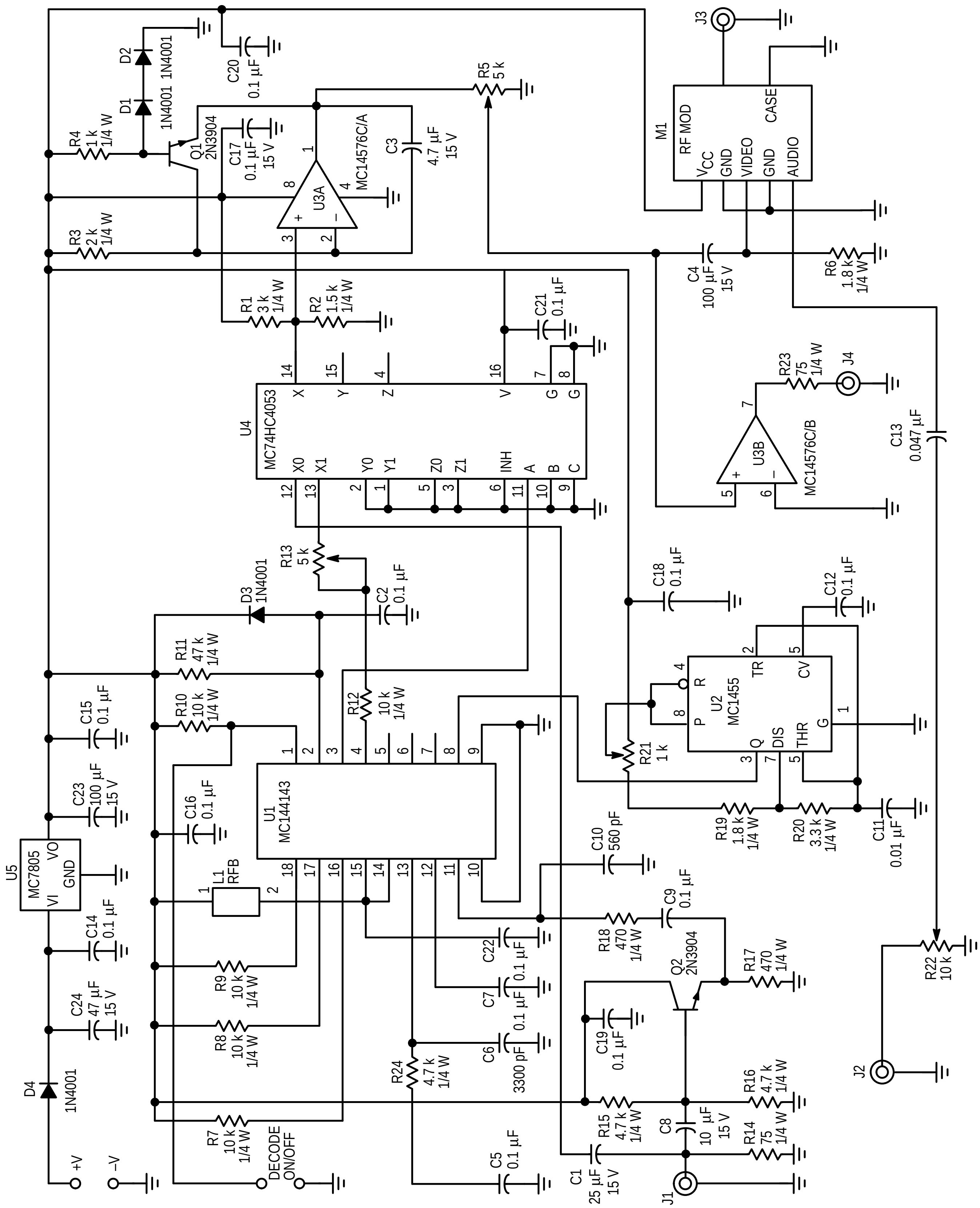
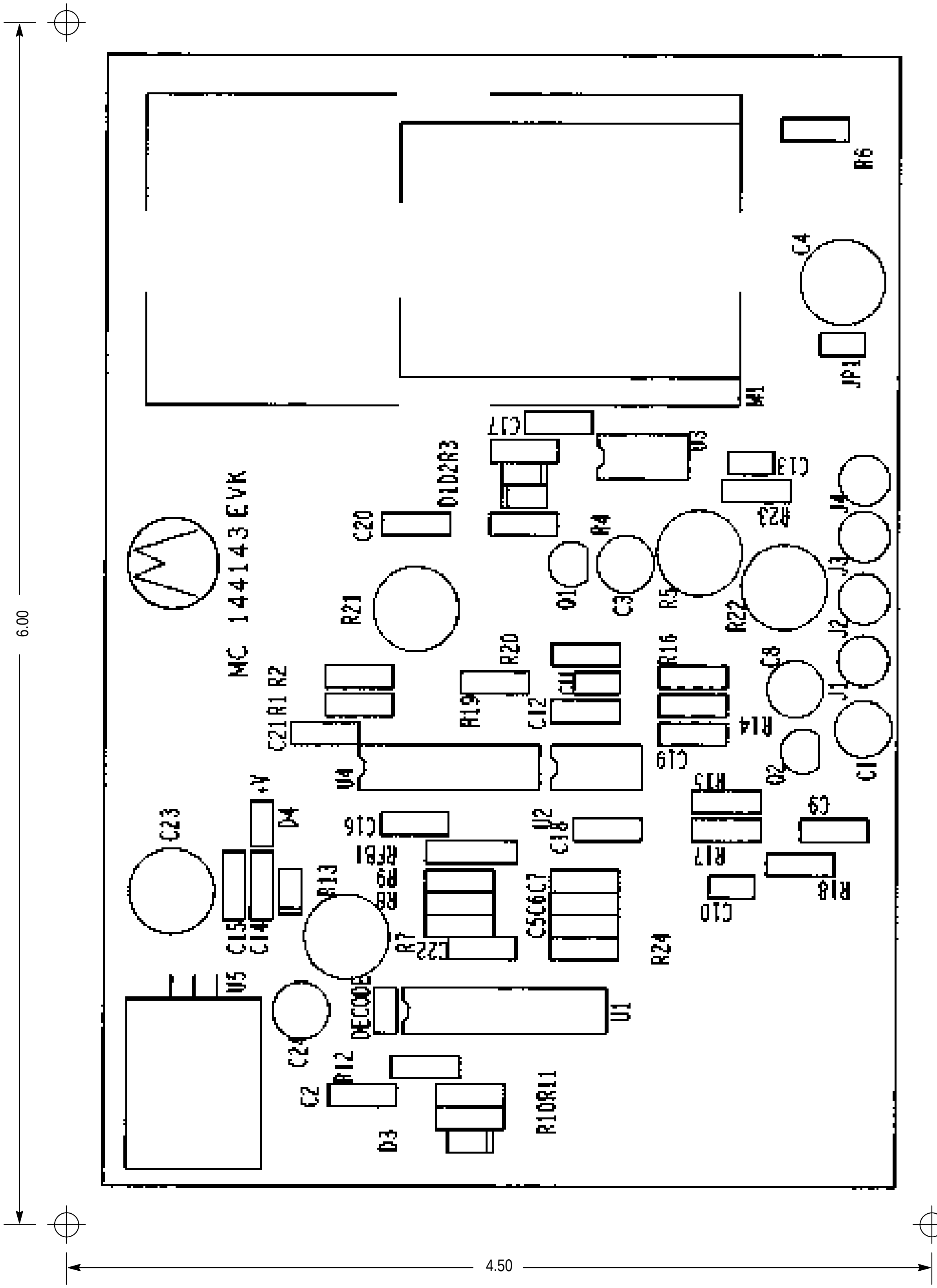
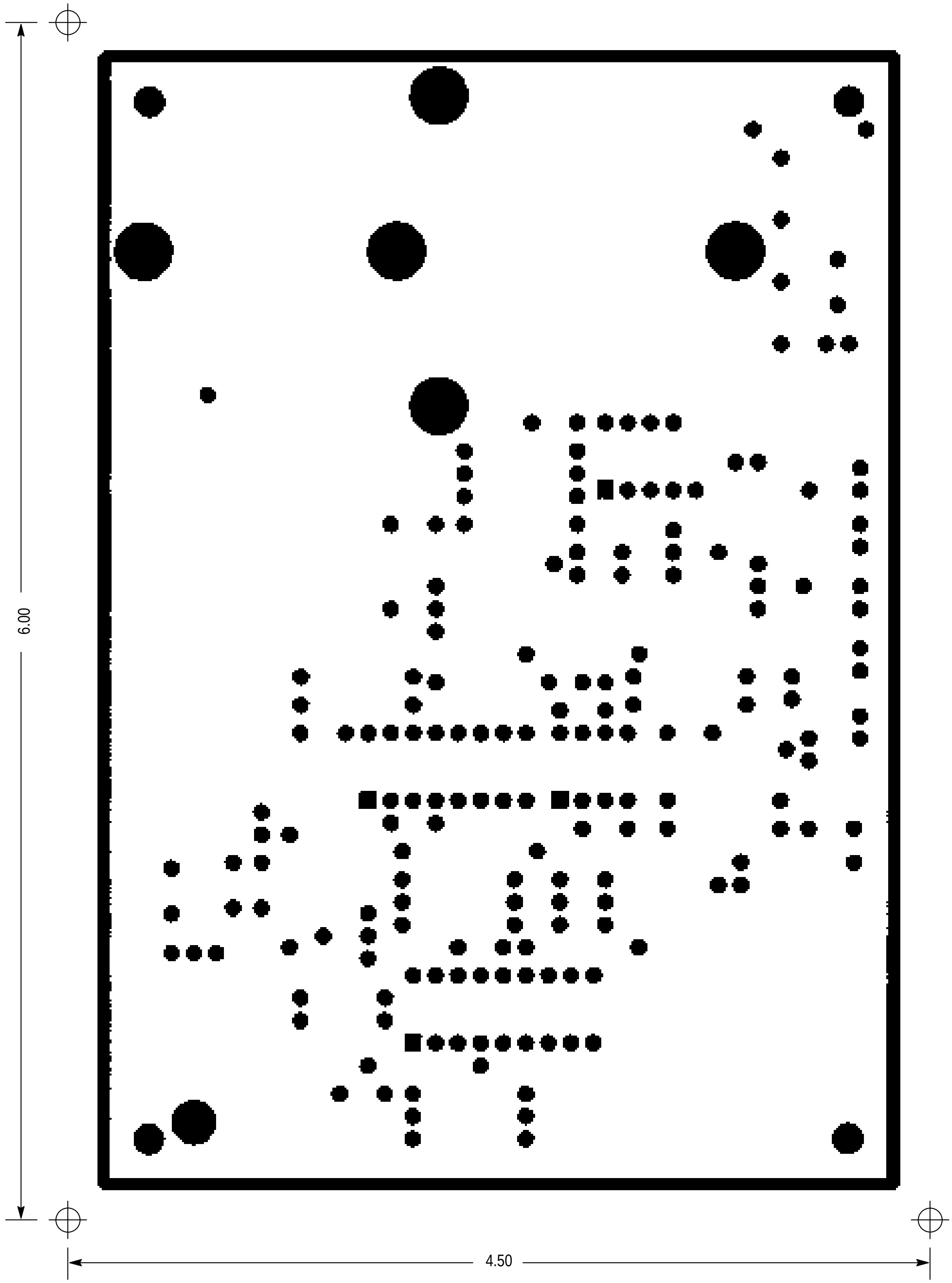


Figure 6. Set Top Decoder Schematic

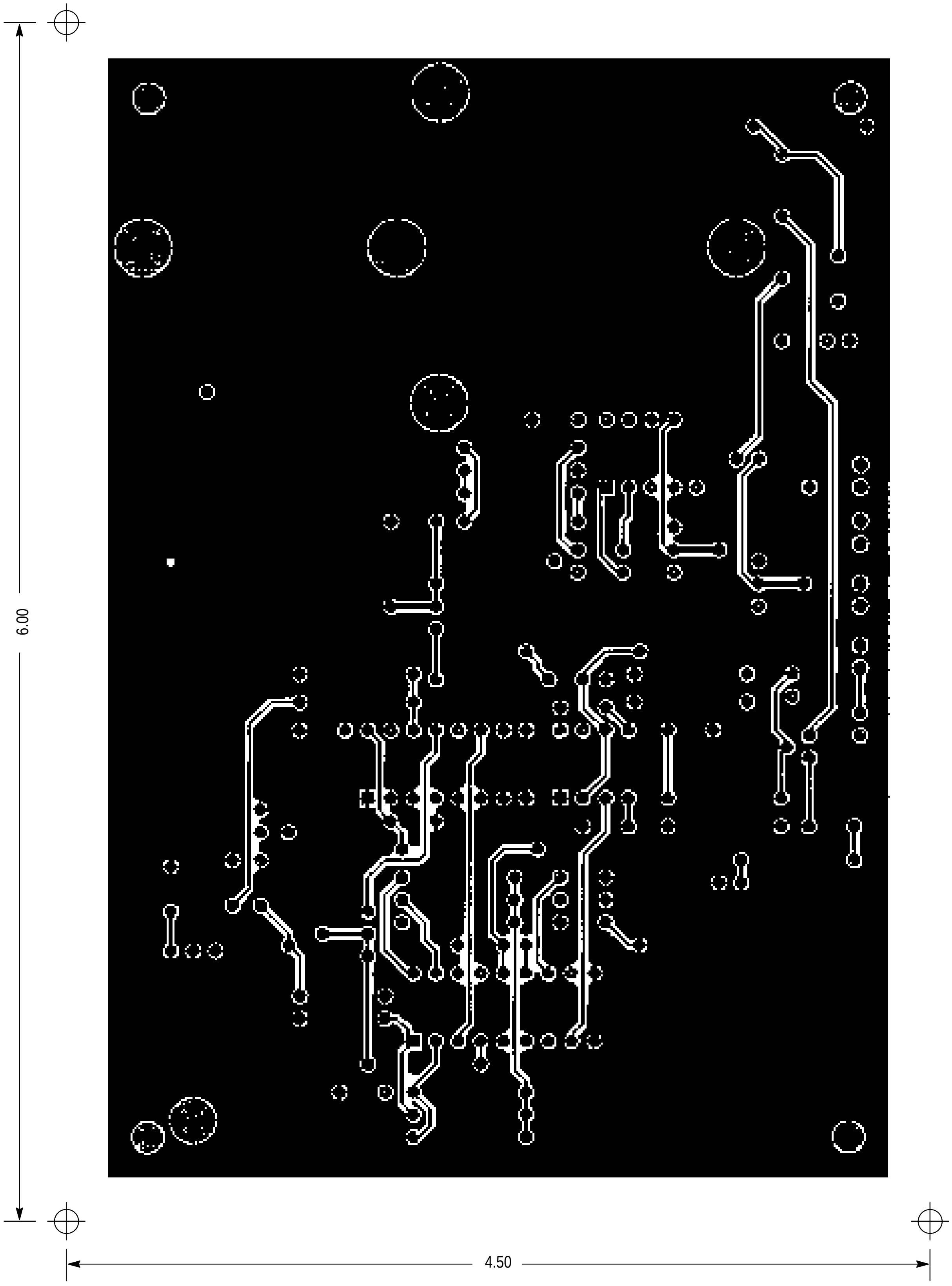
COMPONENT SIDE SILKSCREEN



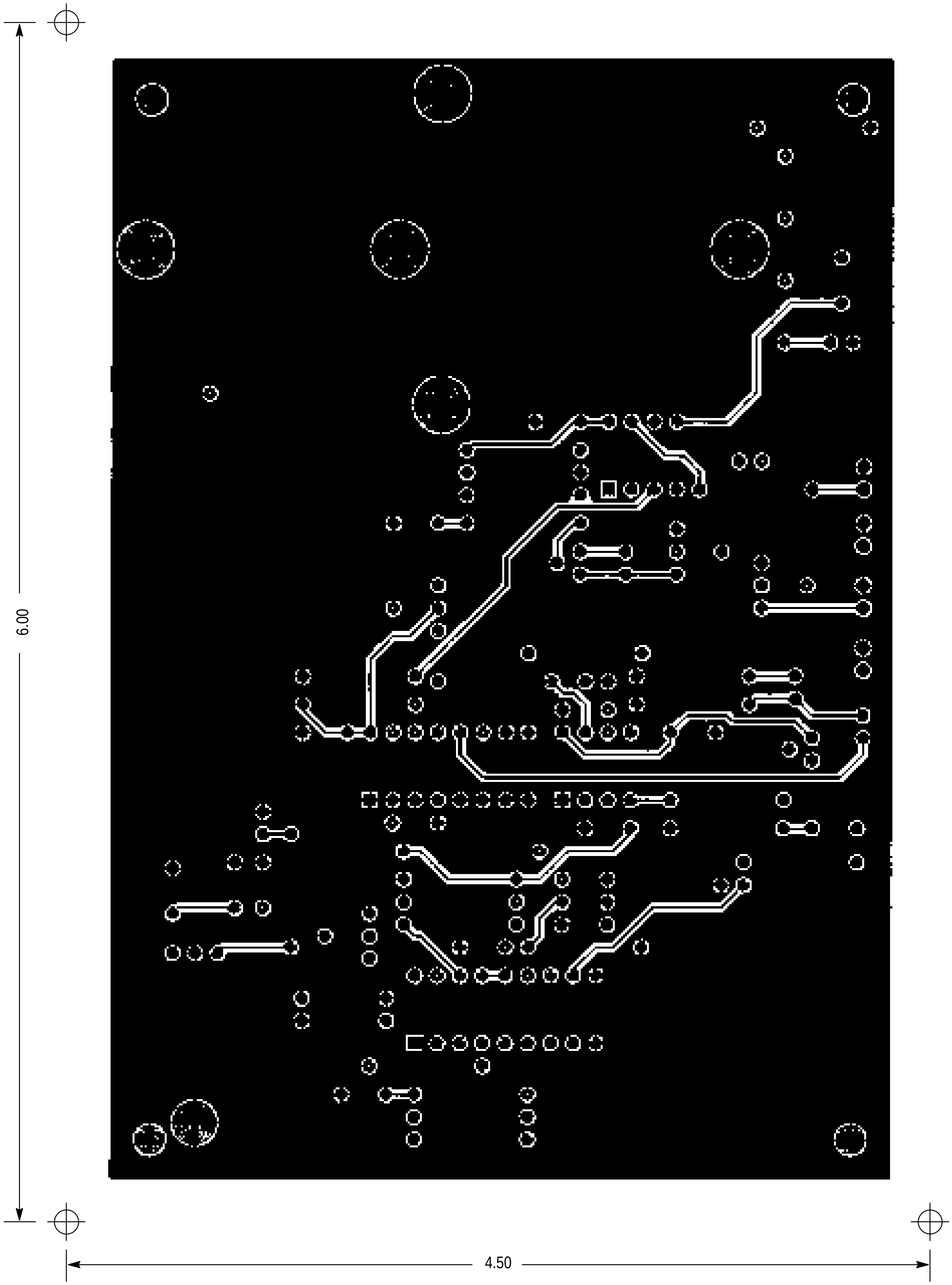
COMPONENT SIDE SOLDERMASK



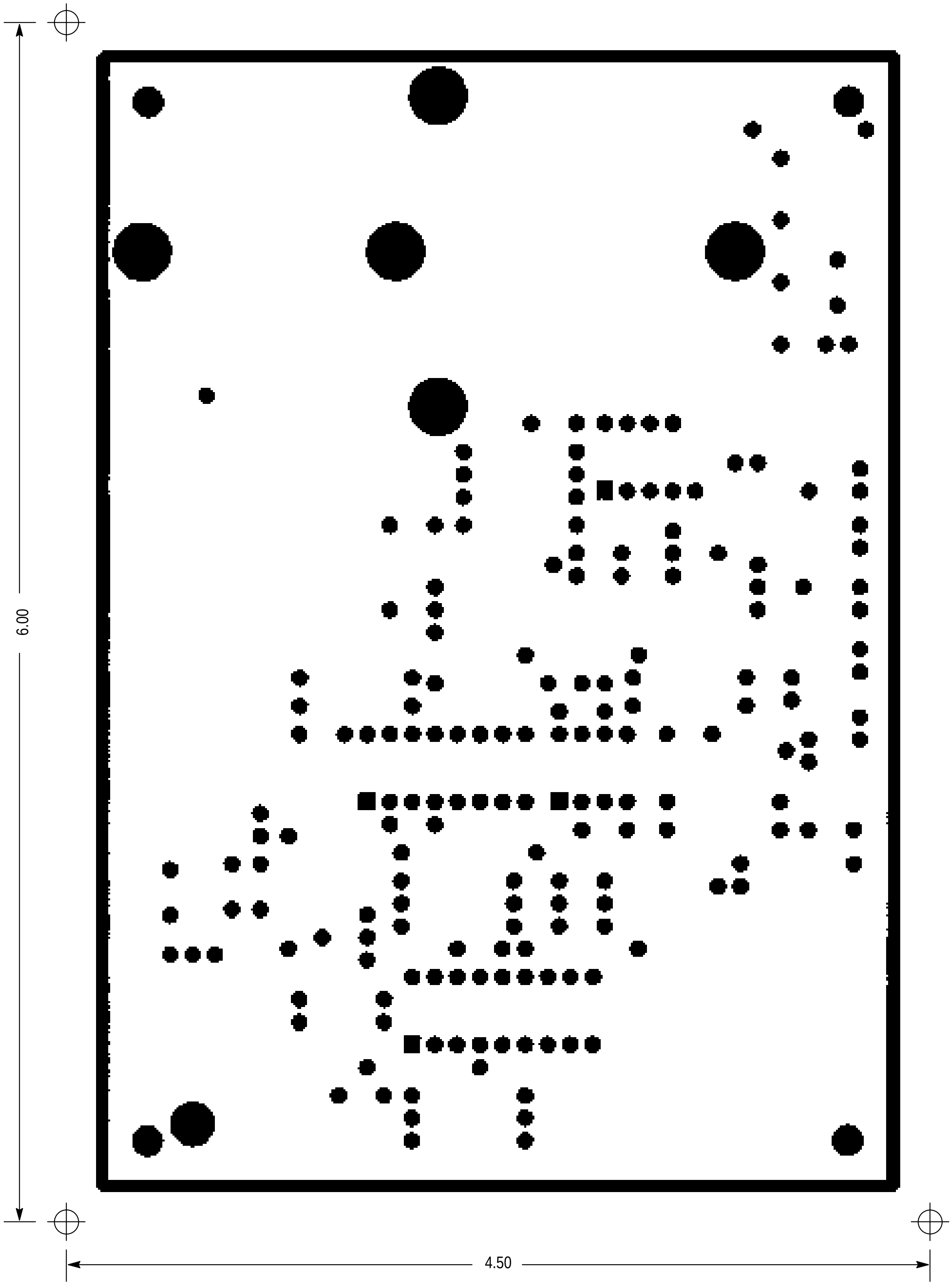
TOP, SIGNAL 1, LAYER 1



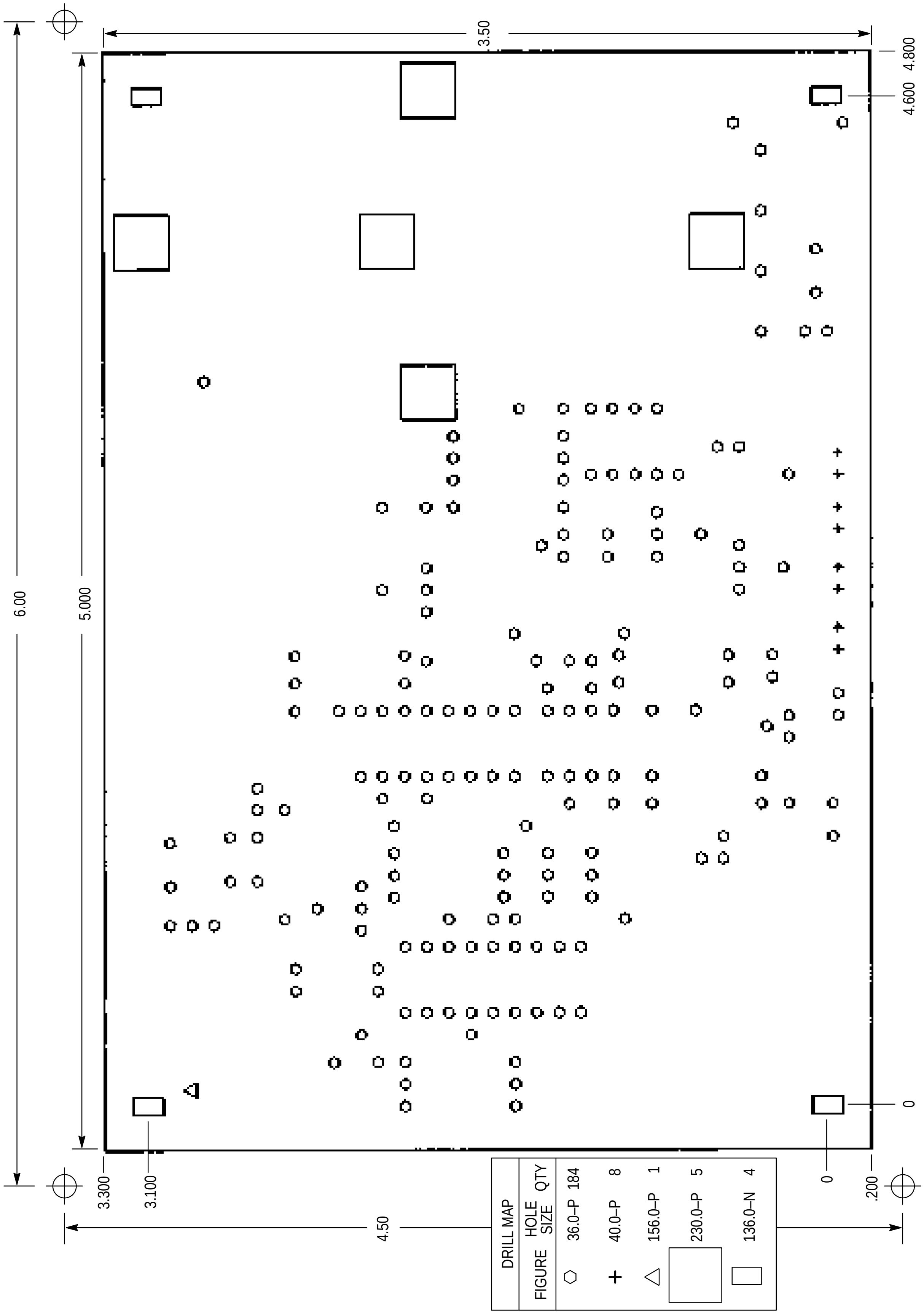
BOTTOM, SIGNAL 2, LAYER 2



SOLDER SIDE SOLDERMASK



DRILLMASTER



TV SET TOP CLOSED–CAPTION DECODER PARTS LIST

Item	Quantity	Reference	Part
1	1	R19	1.8 k
2	5	J1, J2, J3, J4, + V	
3	1	C1	25 μF
4	13	C2, C5, C7, C9, C14, C15, C16, C17, C18, C19, C20, C21, C22	0.1 μF
5	1	C3	4.7 μF
6	2	C4, C23	100 μF
7	1	C6	3300 pF
8	1	C8	10 μF
9	1	C10	560 pF
10	1	C11	0.01 μF
11	1	C12	0.1 μF
12	1	C13	0.047 μF
13	1	C24	47 μF
14	3	D1, D3, D4	1N4001
15	1	D2	1N4001
16	1	Decode	On/Off (SPST Switch)
17	1	L1	RFB (Ferrite Bead)
18	1	M1	RF Mod
19	2	Q1, Q2	2N3904
20	1	R1	3 k
21	1	R2	1.5 k
22	1	R3	2 k
23	2	R4, R21	1 k
24	2	R5, R13	5 k
25	1	R6	1.8 k
26	6	R7, R8, R9, R10, R12, R22	10 k
27	1	R11	47 k
28	2	R14, R23	75
29	3	R15, R16, R24	4.7 k
30	2	R17, R18	470
31	1	R20	3.3 k
32	1	U1	MC144143
33	1	U2	MC1455
34	1	U3A	MC14576B/A
35	1	U3B	MC14576B/B
36	1	U4	MC74HC4053
37	1	U5	MC7805

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