AN1243

Output Loading Effects on Fast Static RAMs

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INTRODUCTION

This review describes the ac loading used for testing. Component test engineers should pay careful attention to the test conditions and derating curves for deviations from the specified load. This information is also applicable for system engineers calculating required device speed for a given environment. This information will help the user make the appropriate choice of device performance for their needs.

As device access times decrease, so do output transition times. With faster rise and fall times come additional problems associated with output and signal path impedances. In any system running at frequencies where the propagation delay of a signal path (t_{pd}) is greater than 1/2 of the total signal transition time, transmission line effects will be seen on the signal. This results in overshoot and undershoot at the load end of a conductor, which can cause problems in testing, or in actual use of the device. This discussion gives a brief overview of the factors contributing to these effects, and the measures that can be used to predict or eliminate them. For a detailed discussion of both PC board layout considerations and applicable transmission line theory, consult the *MECL System Design Handbook*, publication HB205/D, Motorola, Inc., 1983.

DEFINITION OF TERMS

t_{pd} — Propagation delay in seconds
L_0 — Inductance in henries/meter
C_0 — Capacitance in farads/meter
R_L — Load resistance in ohms
$R_{DS(on)}$ — Resistance from drain to source of a FET device when on
R_O — Output resistance in ohms. For CMOS devices, this is the $R_{DS(on)}$ resistance of the output devices.
R_{OH} — Output resistance for a high, or 1, signal from the device
R_{OL} — Output resistance for a low, or 0, signal from the device
ρ_L — Reflection coefficient of the load end of a signal
ρ_S — Reflection coefficient of the source end of a signal, the device output
V_L — Termination voltage of the load resistor in a transmission line termination network

TRANSMISSION LINE OVERVIEW

What is a transmission line and how does it affect output waveforms? In simple terms, a transmission line is a signal path that exhibits a characteristic impedance. The type of lines discussed in this paper are primarily microstrip (Figure 1) and stripline signal paths (Figure 2) found in most PC boards today. The inductance and capacitance of these lines are a function of the line thickness and width in combination with the dielectric properties of the PC board material and the distance of the line from the ground plane. The impedance of the line is determined by these characteristics and the additional distributed capacitance from other devices on the line.

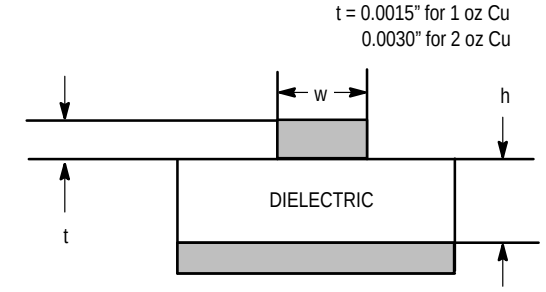

Figure 1. Microstrip Signal Path

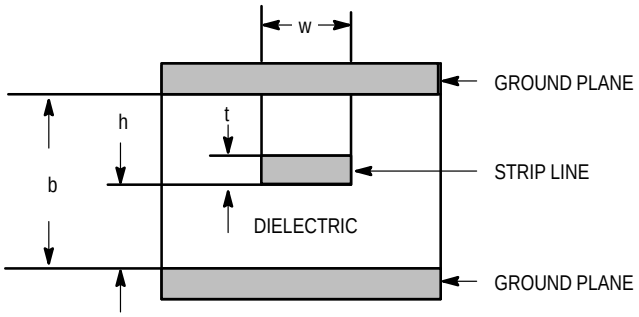

Figure 2. Stripline Signal Path

The characteristic impedance of a microstrip or stripline path is given by the formula $Z_0 = \sqrt{L_0 / C_0}$. The propagation delay of the path, t_{pd}, is $t_{pd} = \sqrt{L_0 / C_0}$ x length = $Z_0 C_0$ x length. For example, the propagation delay of a microstrip line on G10 epoxy/glass material is approximately 1.76 ns/ft, while the delay for a stripline is about 2.27 ns/ft.

The effect of a transmission line on a device output depends on the electrical length of the line. In all cases, a signal traveling down the line will be affected at the end of the line if it is not terminated with a resistor of the characteristic impedance of the line. The amount of effect is determined by the reflection coefficient of the load, ρ_L, where:

$$\rho_L = \left(\frac{R_L - Z_0}{R_L + Z_0}\right) \quad (1)$$

This reflection occurs at a time t_{pd} after a change at the source of the signal. A similar reflection occurs at $2t_{pd}$ after this new signal has returned from the load to the source, and is determined by the source reflection coefficient, ρ_S, where:

$$\rho_S = \left(\frac{R_O - Z_0}{R_O + Z_0}\right) \quad (2)$$

R_O is the output resistance of the device. In the case of an electrical line length with t_{pd} less than 1/2 of the rise/fall time of the output signal, the transmission line effects are seen as a delay of the signal transition times. This is caused by the load reflection returning to the source during the actual signal transition and being included in the duration of the signal. For the case of an electrical length with t_{pd} greater than 1/2 of the rise/fall time of the output signal, the reflection effects may be seen directly. In severe cases, signal overshoot or undershoot can cause an invalid level to be seen at the load end at $3t_{pd}$.

The formulas for determining reflection coefficients require knowledge of the output impedance of the device, the characteristic impedance of the signal path, and the termination resistance. The goal of termination is to guarantee that the output signal at the receiving end (load) has enough margin to keep reflection effects from causing a false level to be detected. In an ideal case, the termination resistance is equal to the characteristic impedance of the line, and therefore, no reflection is generated at the load. In that one case, the impedance mismatch at the source is of importance only for signal rise time, V_{OH} and V_{OL} considerations.

The effect of additional distributed capacitance on a transmission line is a reduction in impedance resulting in little change to t_{pd}. This additional capacitance does, however, change the signal transition times resulting in a longer rise and fall time.

OUTPUT BUFFERS

The schematic drawing for a typical CMOS TTL output buffer is shown in Figure 3. Figure 4 shows the equivalent circuit as actually implemented in many devices. The actual values for R_{OH} and R_{OL} vary from design to design but the range of values is similar.

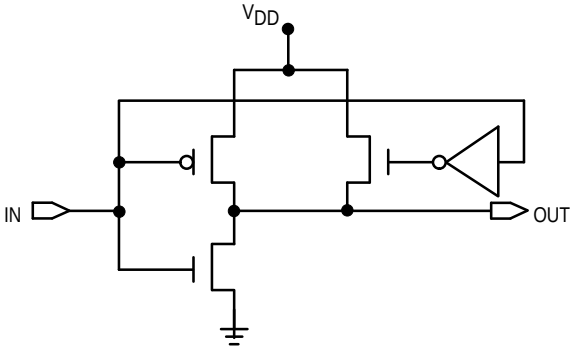

Figure 3. Typical Output Buffer

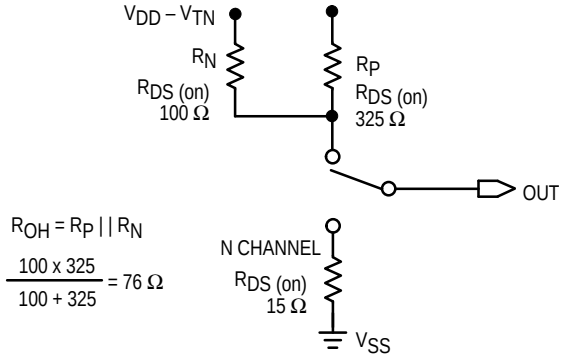

Figure 4. Effective Circuit

As can be seen from Figures 3 and 4, the output impedance of a TTL output buffer is different for high and low output signals. This relation, along with the choice of V_{DD} level, termination resistance, and voltage determine the output high and low levels the part will produce in the system. In a dc condition with R_L = 50 Ω = and V_L = 1.5 V, the output voltages would be:

$$V_{OL} = V_{SS} + (V_L - V_{SS})\left(\frac{R_{OL}}{R_{OL} + R_L}\right)$$

$$V_{OL} = 0\ V + (1.5\ V - 0\ V)\left(\frac{15\ \Omega}{15\ \Omega + 50\ \Omega}\right)$$

$$V_{OL} = 0.35\ V \qquad (3)$$

$$V_{OH} = V_L + \left(V_{DD} - V_L - V_{TN}\ \frac{R_P}{R_P + R_N}\right)\left(\frac{R_L}{R_L + R_{OH}}\right)$$

$$V_{OH} = 1.5\ V + \left(4.4\ V - 1.5\ V - 1.2\ V)\ \frac{325\ \Omega}{100\ \Omega + 325\ \Omega}\right)\left(\frac{50\ \Omega}{50\ \Omega + 76\ \Omega}\right)$$

$$V_{OH} = 2.33\ V \qquad (4)$$

TRADITIONAL TTL OUTPUT LOAD SPECIFICATIONS

The output loading typically specified in the industry until now is shown in Figure 5. The load consists of a resistor network and capacitance. The values for the network were chosen to present a dc load of 8 mA during an output low condition ($V_{OL} \leq 0.4$ V) and – 4 mA for an output high ($V_{OH} \geq 2.4$ V). A 5 V supply was chosen as the termination supply and a divider network was calculated to provide the specified currents. In addition, a lumped capacitive load of 30 pF was added to the output to represent input loading from other devices. In actual practice during testing, the load used is a Thevenin equivalent as shown in Figure 6, with capacitance being provided by the 50 Ω transmission line connection to the test head and the test fixture capacitance.

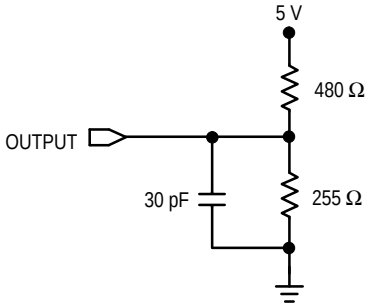

Figure 5. Typical TTL Load

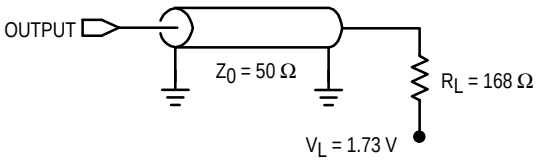

Figure 6. Thevenin Equivalent Test Load

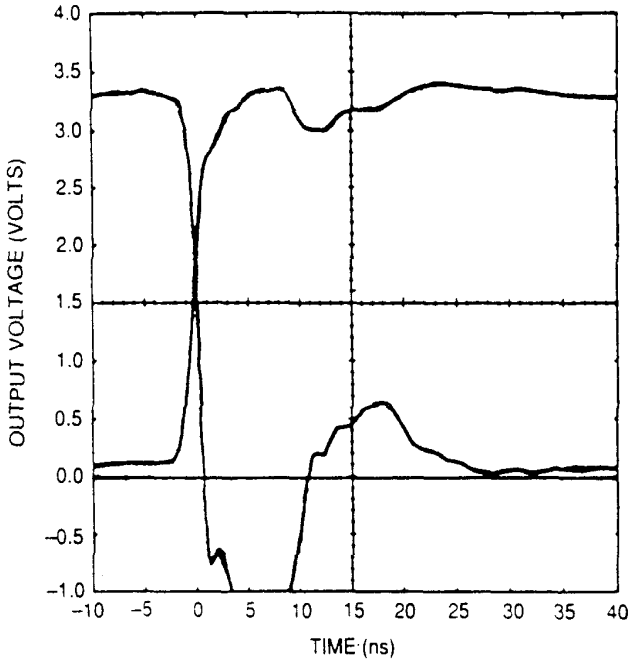

Figure 7. Output Waveforms with Thevenin Equivalent Test Load

The calculated performance of the setup would be that of a transmission line with a Z_0 of 50 Ω terminated to an R_L of 168 Ω at a V_L of 1.73 V. This would be ρ_L = (168 Ω – 50 Ω) / (168 Ω + 50 Ω) = 0.54. This means that the ΔV at the load would be 154% of the source ΔV. Using the example output buffer with V_{DD} = 5.0 V, the dc V_{OL} would be 0.14 V and the incident V_{OH}, using the 50 Ω from Z_0 in place of R_L, would be 2.67 V, giving a ΔV of 2.53 V. The means that for a low to high going signal at the source, at time t_{pd} later, the load would go to V_{OL} + ΔV + (ΔV x 0.54), or 4.01 V.

Figure 7 shows the actual measured waveform at the load end of a test fixture as described in Figure 6. The t_{pd} of the signal path is measured using a TDR (time domain reflectometer) to be approximately 4 ns. Notice the reflection effects at each multiple of t_{pd} on both waveforms. The actual measured waveforms differ from predicted results due to inductance in the ground and V_{DD} path of the device being tested.

In a testing environment, the t_{pd} is subtracted from the time measured to give the actual output delay of the device (access time). Because of this, the distortions at the device output are of no concern. The ringing at the load end, however, can cause severe problems when trying to accurately test the speed of the parts. In the past, the access time has been measured from some mid–level voltage which is centered between the high and low output swing. This has the effect of giving the most noise margin to ringing output signals. However, this maximum noise margin does not guarantee that problems will not arise.

NEW HIGH FREQUENCY AC TEST LOAD

In order to properly test and guarantee the ac performance of these fast static RAMs, it is necessary to change the conditions for ac loading to a load that will allow accurate evaluation of the device parameters. Because of this, the specified ac load is now a transmission line terminated with a resistor of the characteristic impedance of the line to a load voltage (see Figure 8).

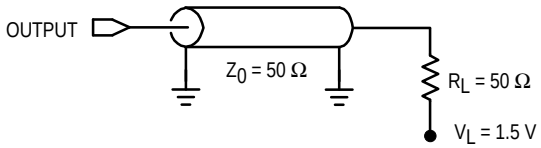

Figure 8. New High Frequency AC Test Load

The calculated performance of this load in a normal test environment would be ρ_L = (50 Ω – 50 Ω) / (50 Ω – 50 Ω) = 0.0. This means that the ΔV at the load would be the same as the source ΔV with no signal reflection.

As seen in Figure 9, using a transmission line terminated to a load supply through a resistor equal to the characteristic impedance of the line produces a load waveform that matches the source signal. Additionally, under ideal conditions, no reflection effects are produced with this load. This results in the maximum possible noise margin for both test and system environments. In this test setup, power supply inductance causes some output noise which is seen at the load.

Figures 10 and 11 are derating curves for calculating the effects of varying C_0 and R_L. These curves are based on typical device performance and are not intended to be absolute worst case specifications.

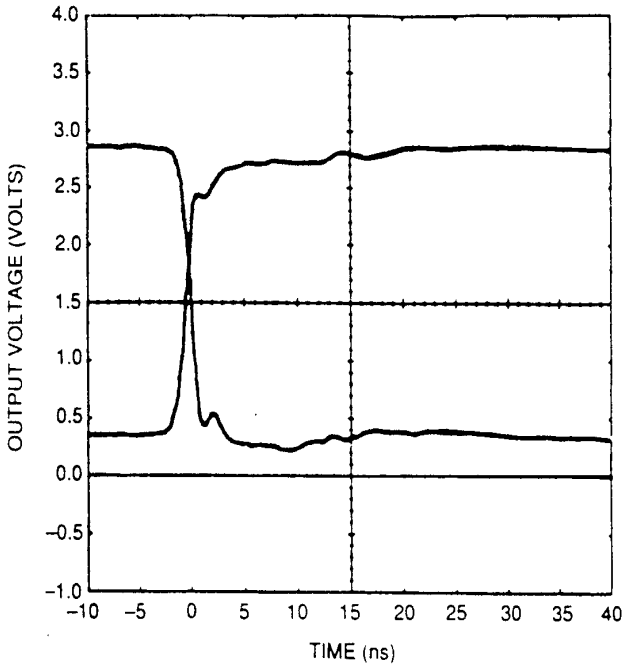

Figure 9. Output Waveforms with High Frequency AC Test Load

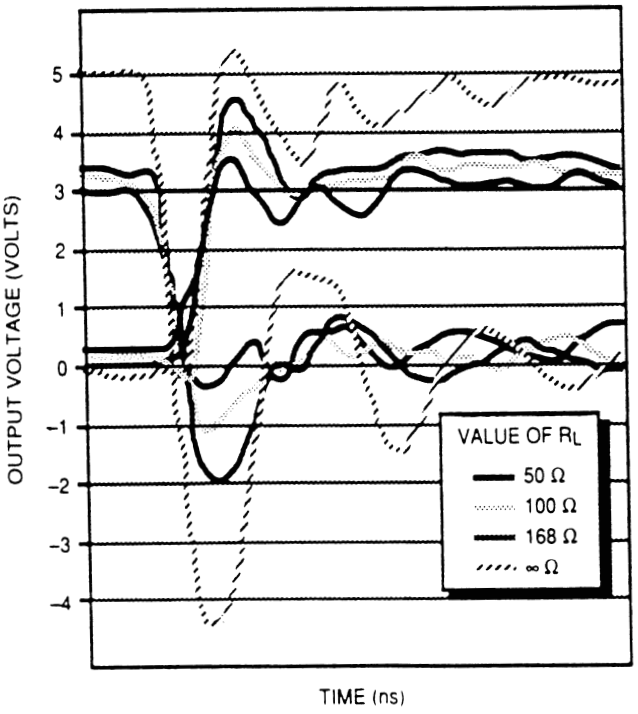

Figure 10. Output Voltage as a Function of R_L

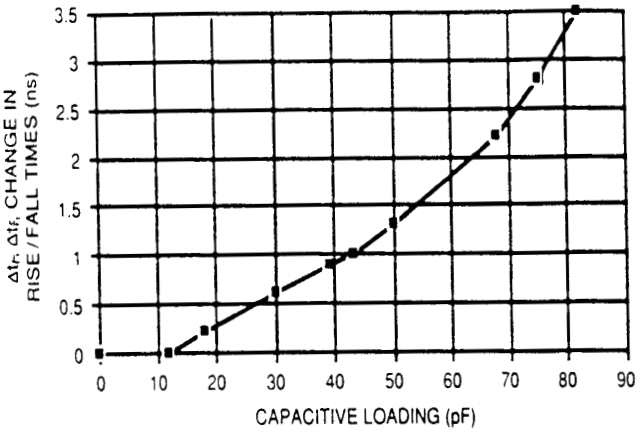

Figure 11. Change in Output Rise and Fall Times for Lumped Capacitive Loads

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