AN1265

Configuring the MPC2605 Integrated L2 Cache with the MPC106

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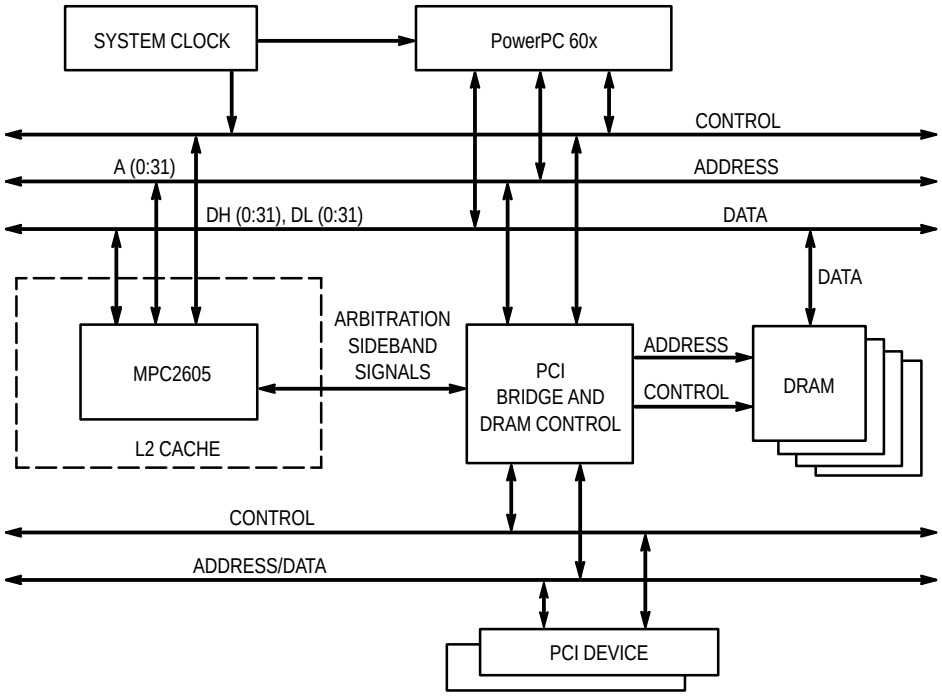
An L2 cache has become a requirement for most computers, especially for RISC architectures such as the PowerPC™ family of microprocessors. Adding an L2 cache to the system is one of the easiest ways to significantly increase the performance of the processor. Several factors contribute to the need for an L2 cache: faster processor speeds that are multiples of the system bus frequencies, so that an L1 miss results in several processor wait cycles, while data are retrieved from the main memory; larger applications with code or data that does not fit in the L1 cache; and large penalties for going to main memory due to speed differences between DRAM main memory and SRAM L2 cache.

So, what is the best L2 cache design? Optimally, it would be one that never misses a processor read request, and one that can provide data as fast as the processor can handle it. This is not possible, realistically (at a reasonable cost, at least). However, a close approximation is possible with a good design. The MPC2605 is an integrated secondary cache for PowerPC microprocessor–based designs and has all the features that an optimally designed L2 cache should have. The MPC2605 is the fastest L2 cache available for the PowerPC 60x bus. Due to its integration of logic, tag, and data on the same silicon, it can respond to a read hit with a 2–1–1–1 burst at 66 MHz. This alone is a 17% read hit performance improvement over a 3–1–1–1 L2 cache. The MPC2605 can also provide subsequent bursts as fast as 1–1–1–1. It is also a copy–back (write–back) design, meaning that it will shorten a processor write to the speed of the L2 instead of the speed of main memory. Additionally, it is four–way set associative, which significantly increases the odds of a read hit over an equivalent sized direct mapped cache. The set associativity also decreases the odds of thrashing, a scenario in which the cache is constantly being rewritten from main memory because different main memory addresses are mapped to the same cache address.

SYSTEM BLOCK DIAGRAM



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REV 9
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CONNECTING THE MPC2605 TO THE MPC106

The MPC2605 is designed to work in conjunction with the Motorola MPC106 PCI Bridge/Memory controller. The following describes a one–chip MPC2605 solution (256K bytes) in conjunction with a MPC106 chip and a single PowerPC processor.

All data, address, and parity bits (if used) are tied to the respective pins on the MPC106 and 60x.

The CFG0, CFG1, and CFG2 pins are tied low. CFG3 and CFG4 are tied high.

Certain control lines are tied between the MPC106 and all MPC2605 chips. $\overline{\text{HIT}}$ on the MPC106 is tied to $\overline{\text{L2 CLAIM}}$ on the MPC2605; $\overline{\text{BRL2}}$ to $\overline{\text{L2 BR}}$; $\overline{\text{BGL2}}$ to $\overline{\text{L2 BG}}$; and $\overline{\text{DBGL2}}$ to $\overline{\text{L2 DBG}}$. A pullup resistor to V_{DD} should be tied to $\overline{\text{L2 CLAIM}}$ and $\overline{\text{L2 BR}}$. The resistor value should be in the 2K to 10K range.

The 60x control lines that must go to the MPC2605 chips include: $\overline{\text{AACK}}$, $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{CI}}$, $\overline{\text{HRESET}}$, $\overline{\text{TA}}$, $\overline{\text{TBST}}$, $\overline{\text{TS}}$, TSIZ0 – TSIZ2, TT0 – TT4, and $\overline{\text{WT}}$. All other input control lines may be tied high, unless other chips in the system use them.

$\overline{\text{FDN}}$ should be tied between all MPC2605 chips along with a pullup resistor. $\overline{\text{TRST}}$ should be tied low or tied to $\overline{\text{HRESET}}$ for normal operation.

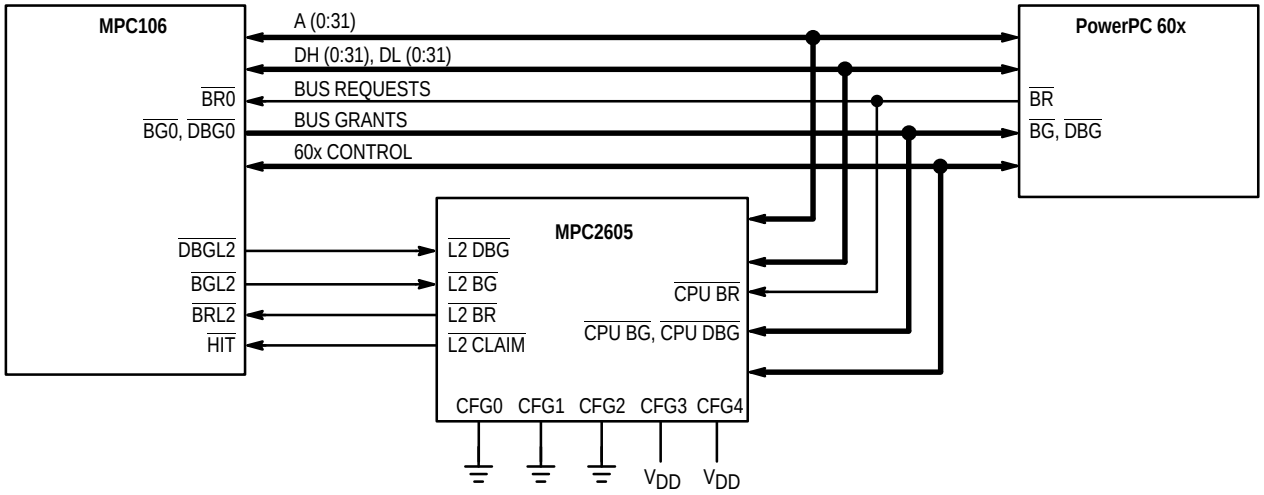
AP and $\overline{\text{APE}}$ are connected if address parity is used. To enable address parity on the MPC2605, $\overline{\text{APEN}}$ is tied low.

Note that $\overline{\text{APE}}$ should not be connected if address parity is not used. $\overline{\text{APE}}$ may generate incorrect signals when $\overline{\text{APEN}}$ is tied high.

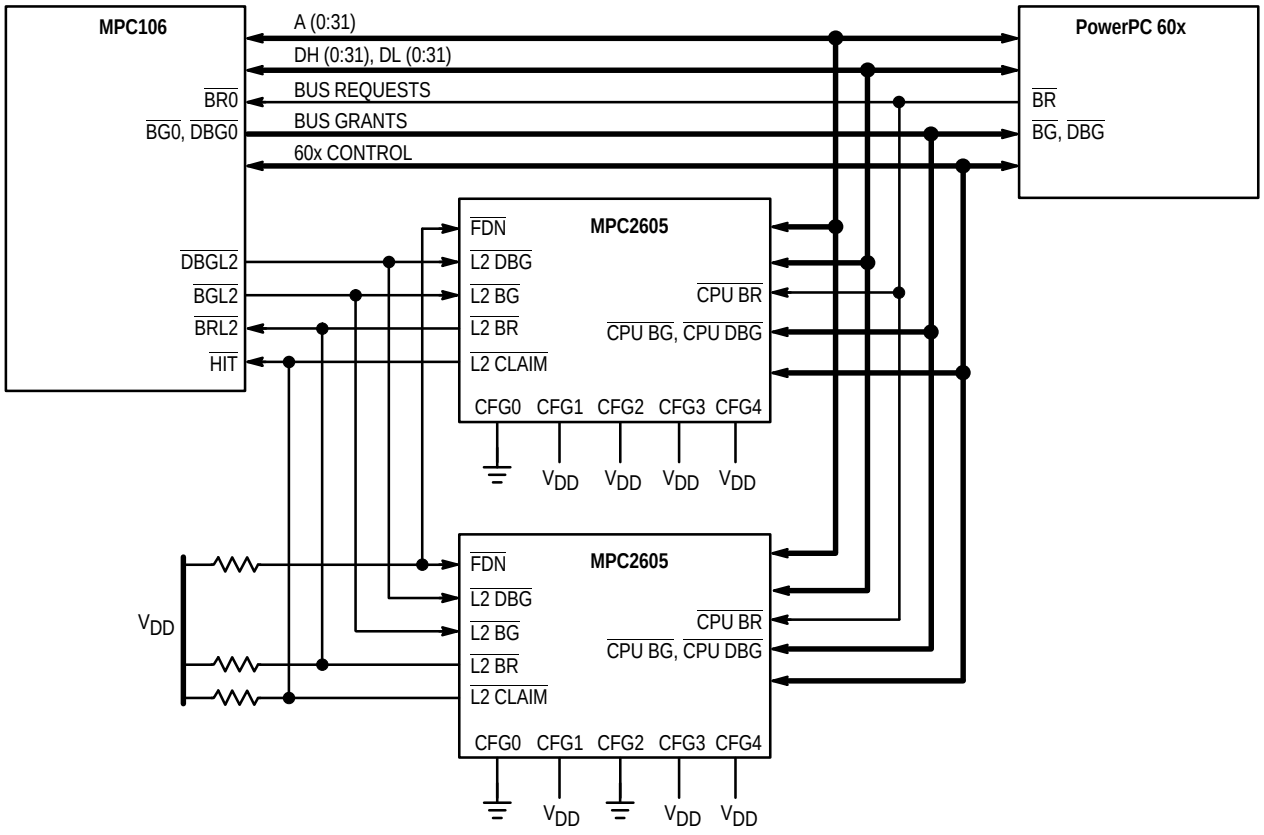
$\overline{\text{L2 CI}}$ is a sideband signal that allows the user to turn off the cache beside the PPC–controlled $\overline{\text{CI}}$.

$\overline{\text{GBL}}$ is an output–only signal, but the MPC2605 drives only a high signal.

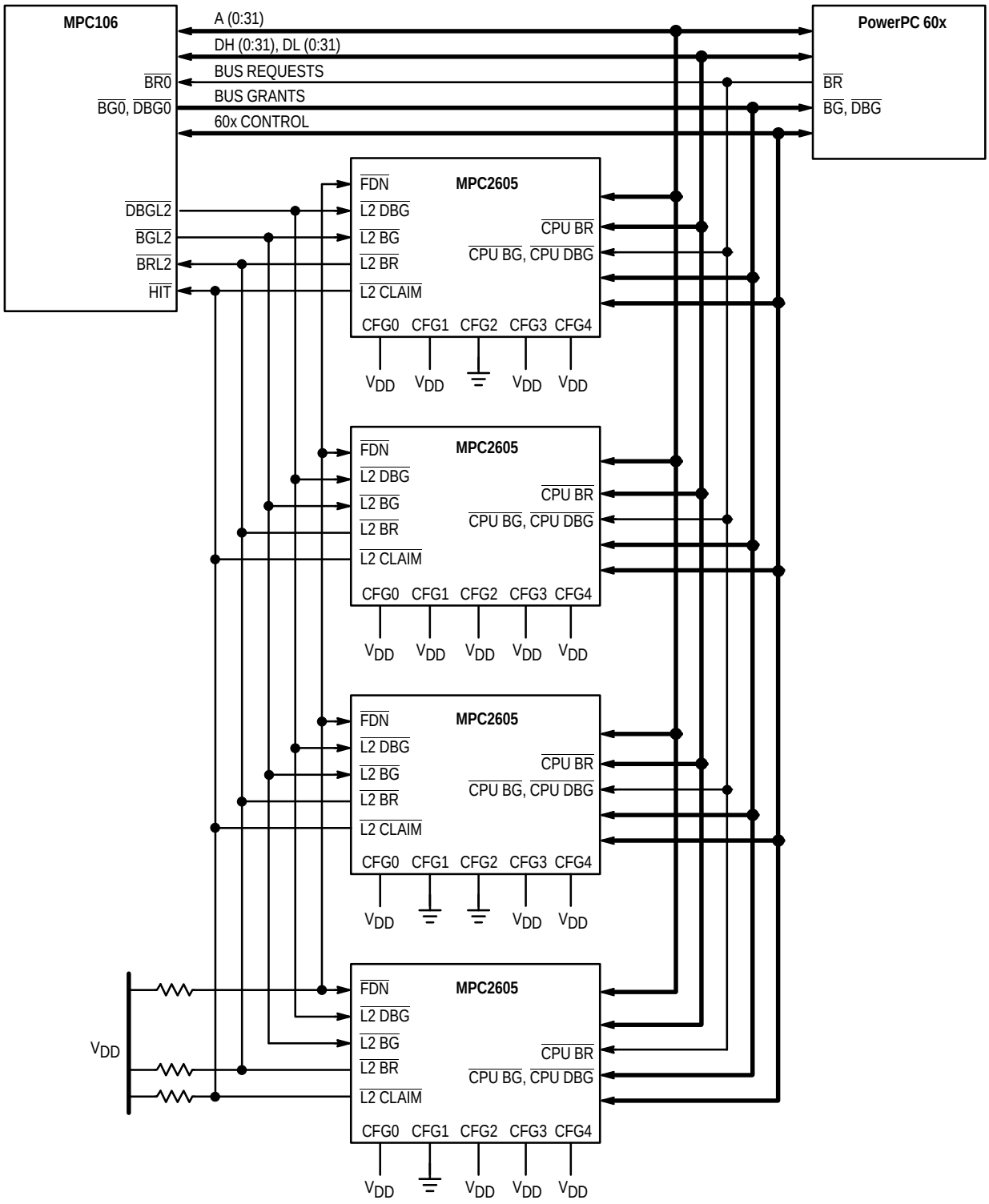
SYSTEM BLOCK DIAGRAM FOR A 256KB MPC2605 SOLUTION



SYSTEM BLOCK DIAGRAM FOR A 512KB MPC2605 SOLUTION



SYSTEM BLOCK DIAGRAM FOR A 1MB MPC2605 SOLUTION



CONFIGURATION REGISTER BITS

Certain bits in the processor interface configuration register in the MPC106 have to be set to work with the MPC2605. Note: These configuration changes must be made before the MPC2605 asserts $\overline{\text{L2 CLAIM}}$ for the first time.

1. CF_APHASE_WS (1..0) must be set to 00.
2. CF_LOOP_SNOOP must be set high. (Default)
3. CF_L2_HIT_DELAY (1..0) must be set to 01.
4. The setting of CF_FAST_L2_MODE should be set to match the processor after a reset.
5. The best performance is achieved by having the MPC106 park the data bus. This can be done by setting CF_APARK and CF_DPARK to 1 and setting CF_BREAD_WS to 0.
6. Since the MPC2605 has its own cache controller, the controller on the MPC106 must be disabled. This is accomplished by setting bit CF_EXTERNAL_L2 = 1. (Default)
7. For a uniprocessor system, bits CF_L2_MP (1..0) = 00. For MP systems, CF_L2_MP (1..0) should be set to 11. (Default)
8. CF_CBA_MASK (31..24) must be set to 0xFF.
9. In a system using a 603 running in 1:1 bus mode, CF_BREAD_WS must be set to 1 in normal bus mode or 2 in no–$\overline{\text{DRTRY}}$ mode.

The registers L2_CACHE_MISS_INHIBIT, L2_UPDATE_INHIBIT, and CF_FLUSH_L2 in the MPC106 have no effect on the MPC2605. To obtain this functionality on the MPC2605, they must be generated by some other device.

INITIALIZATION

To ensure proper initialization, the $\overline{\text{HRESET}}$ pin on the MPC2605 should be tied to the same line that connects to the $\overline{\text{HRESET}}$ pin on the processor. This will cause the MPC2605 and the processor to be reset at the same time. Once $\overline{\text{HRESET}}$ is pulled high, the MPC2605 begins an internal configuration sequence that lasts about 4000 cycles. During this time, the MPC2605 will ignore all bus transactions.

CONNECTION LIST

The following MPC2605 signals must be connected to the 60x bus as shown, regardless of whether the MPC2605 is being used with the MPC106.

60x BUS SIGNALS

MPC2605 Signals	60x Bus Signals
A (0:31)	A (0:31)
$\overline{\text{AACK}}$	$\overline{\text{AACK}}$
$\overline{\text{ABB}}$	$\overline{\text{ABB}}$
AP (0:3)	AP (0:3) (if used)
$\overline{\text{APE}}$	$\overline{\text{APE}}$ (do not connect if not used)
$\overline{\text{ARTRY}}$	$\overline{\text{ARTRY}}$
$\overline{\text{CI}}$	$\overline{\text{CI}}$
CLK	SYSCLK (the 60x bus clock)
$\overline{\text{CPU BG}}$	$\overline{\text{BG0}}$
$\overline{\text{CPU BR}}$	$\overline{\text{BR0}}$
$\overline{\text{CPU DBG}}$	$\overline{\text{DBG0}}$
$\overline{\text{CPU2 BG}}$	Tie high (if uniprocessor), $\overline{\text{BG1}}$ (if MP)
$\overline{\text{CPU2 BR}}$	Tie high (if uniprocessor), $\overline{\text{BR1}}$ (if MP)
$\overline{\text{CPU2 DBG}}$	Tie high (if uniprocessor), $\overline{\text{DBG1}}$ (if MP)
DH (0:31) DL (0:31) DP (0:7)	DH (0:31), DL (0:31), and DP (0:7) (optional)
$\overline{\text{DBB}}$	10K pullup
$\overline{\text{GBL}}$	$\overline{\text{GBL}}$
$\overline{\text{HRESET}}$	$\overline{\text{HRESET}}$
$\overline{\text{L2CI}}$	$\overline{\text{L2CI}}$ (if present, else tie to V_{DD})
$\overline{\text{SRESET}}$	$\overline{\text{SRESET}}$
$\overline{\text{TA}}$	$\overline{\text{TA}}$
$\overline{\text{TBST}}$	$\overline{\text{TBST}}$
$\overline{\text{TEA}}$	$\overline{\text{TEA}}$
$\overline{\text{TS}}$	$\overline{\text{TS}}$
TSIZ (0:2)	TSIZ (0:2)
TT (0:4)	TT (0:4)
$\overline{\text{WT}}$	$\overline{\text{WT}}$

MPC2605 TO MPC106 INTERFACE

The following is a list of MPC2605 pins and how they should be connected when used with the MPC106.

MPC2605 Signals	Connect to:
Arbitration Sideband Signals	
$\overline{\text{L2 BR}}$	$\overline{\text{BRL2}}$ (MPC106)
$\overline{\text{L2 BG}}$	$\overline{\text{BGL2}}$ (MPC106)
$\overline{\text{L2 CLAIM}}$	$\overline{\text{HIT}}$ (MPC106)
$\overline{\text{L2 DBG}}$	$\overline{\text{DBGL2}}$ (MPC106)
ASYNCHRONOUS SIGNALS Not Supplied by the MPC106. If these are not supplied by any other chip in the system, they should be tied in the following manner.	
$\overline{\text{L2 MISS INH}}$	Tie High
$\overline{\text{L2 TAG CLR}}$	Tie High
$\overline{\text{L2 UPDATE INH}}$	Tie High
$\overline{\text{L2 FLUSH}}$	Tie High
$\overline{\text{PWRDN}}$	Tie High
Configuration and Testability Pins	
CFG (2:0)	Configuration pins for 256KB, 512KB, or 1 MB sizes (use data sheet for connectivity)
CFG3	Tie High
CFG4	Tie High
TCK	JTAG
TDI	JTAG
TDO	JTAG
TMS	JTAG
$\overline{\text{TRST}}$	JTAG
Interchip Communication	
$\overline{\text{FDN}}$	Tie between all MPC2605 chips and to pullup

NOTES

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