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PowerPC™

Application Note

PowerPC Microprocessor Clock Modes

The PowerPC™ microprocessors offer customers numerous clocking options. An internal phase-lock loop synchronizes the processor (CPU) clock to the bus or system clock (SYSCLK) at various ratios. These ratios allow the designer to utilize the following options:

- Low-speed, low-cost memory systems with economical, low-cost processors.
- Low-speed, economical memory systems isolated from very high-speed processor cores and internal cache.
- High-speed, performance oriented memory systems with maximum achievable processor core and internal cache frequencies.
- Embedded systems with unusual bus speeds dictated by system requirements other than the processor.

This document is divided into two parts:

- General information—This section discusses a variety of issues including:
  - — PowerPC microprocessor clocking operation
  - — PowerPC device numbering methodology
  - — Various test issues and methodology
  - — Special timing considerations
- Appendixes—This section provides several graphs of PowerPC microprocessor clock relationships.

In this document, the term “MPC60x” is used to denote a 32-bit microprocessor from the PowerPC architecture family, including the PowerPC 602™, PowerPC 603™, PowerPC 603e™, PowerPC 604™, and PowerPC 604e™ microprocessors. MPC60x processors implement the PowerPC architecture as it is specified for 32-bit addressing, which provides 32-bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits (single-precision or double-precision).

Part 1 General Information

This section provides information on a variety of issues concerning the PowerPC microprocessors. These include clocking operations, device numbering methods, various test issues, and special timing considerations.

1.1 PowerPC Microprocessor Clocking Operation

Inside each PowerPC microprocessor is a phase-lock loop circuit similar to that shown in Figure 1. A voltage controlled oscillator (VCO) is precisely controlled in frequency and phase by a frequency/phase detector which compares the input bus frequency (SYSCLK frequency) to a submultiple of the VCO output (VCO frequency). As shown in Figure 1, the VCO frequency has been divided twice before comparison. The M divider divides VCO frequency down to the CPU frequency. The N divider divides CPU frequency down to be matched in frequency and phase to SYSCLK. Thus, there are three frequencies related by two divider ratios. The designer must properly choose the divider ratios and the input SYSCLK frequency to control the other two frequencies.

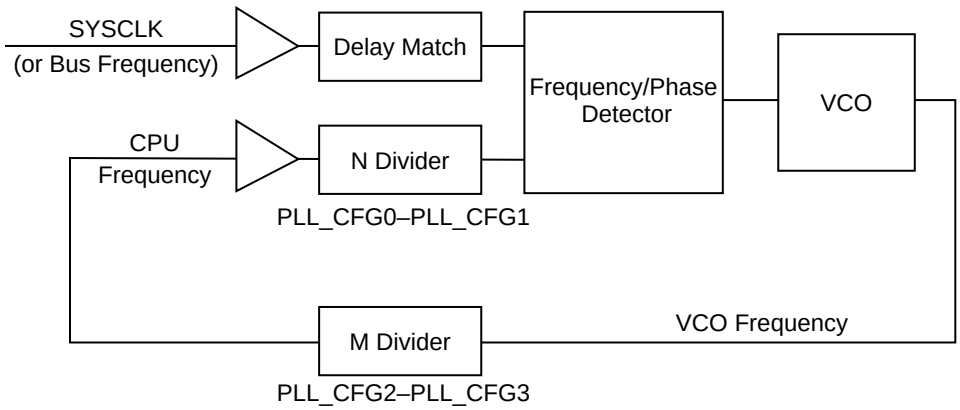


Figure 1. PowerPC Microprocessor Phase-Lock Loop

Table 1 calls out the M and N divider ratios that are supported on various PowerPC microprocessors. The ratio of CPU to SYSCLK frequencies, which is set by the N divider, is often referred to as the bus mode (for example, 1:1 bus mode and 2:1 bus mode). The M and N divider ratios are set by the system designer through the PLL configuration (PLL_CFG) input signals to the microprocessor. Table 1 shows which bus modes are supported on each processor. The 603e, for example, is the first processor to support seven different bus modes.

Note that the 603e is implemented in both a 2.5-volt version (PID 0007v PowerPC 603e microprocessor, or PID7v-603e) and a 3.3-volt version (PID 0006 PowerPC 603e microprocessor, or PID6-603e).

Table 1. Supported M and N Divisors

	M Divider				N Divider										
Divisor	Bypass	2	4	8	1	1.5	2	2.5	3	3.5	4	4.5	5	5.5	6
Bus Mode					1:1	3:2	2:1	5:2	3:1	7:2	4:1	9:2	5:1	11:2	6:1
Device Number Suffix					A	B	C	D	E	F	G	H	I	J	K
Device Applicability															
MPC602	x	x	x	—	x	—	x	—	x	—	—	—	—	—	—
MPC603	x	x	x	x	x	—	x	—	x	—	x	—	—	—	—
MPC603e (PID6-603e)	x	x	x	x	x	x	x	x	x	x	x	—	—	—	—
MPC603e (PID7v-603e)	x	x	—	—	—	—	x	x	x	x	x	x	x	x	x
MPC604	x	x	x	x	x	x	x	—	x	—	—	—	—	—	—
MPC604e	x	x	x	x	x	x	x	x	x	—	x	—	—	—	—
MPC105	x	x	x	x	x	—	x	—	—	—	—	—	—	—	—
MPC106	x	x	x	x	x	—	x	—	x	—	—	—	—	—	—

Figure 2 provides a graphical representation of the three frequencies and divider ratios presented.

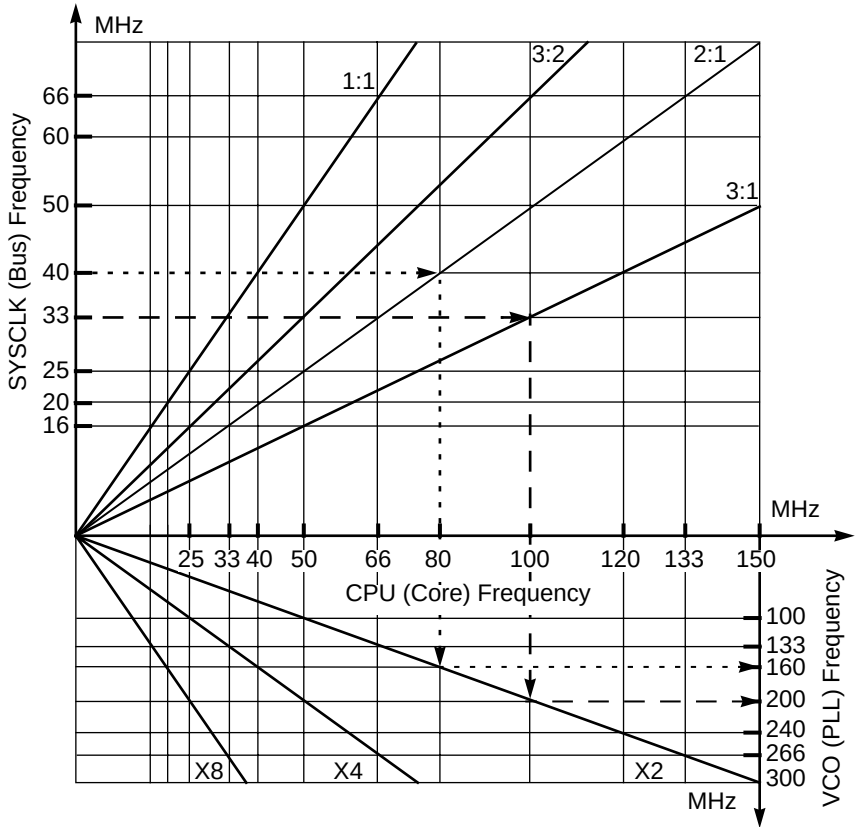


Figure 2. Sample Graph of Clock Relationships

In the graph, the horizontal scale represents the CPU or processor core frequency. SYSCLK, or bus frequency, is represented on the left vertical scale in the top half of the graph. The relationship between SYSCLK and CPU frequency, the N divider or bus mode, is plotted on the heavy solid lines in the top half of the graph.

The VCO frequency is represented on the right vertical scale in the bottom half of the graph. The relationship between VCO frequency and CPU frequency, the M divider, is plotted on the heavy solid lines in the bottom half of the graph.

Note that the vertical scales are different between the top and bottom halves of the graph in order to provide more detail in the critical top half. The bottom half of the graph is used to check that the M and N dividers have been properly chosen to keep the VCO frequency within its specified range of operation.

The graph of Figure 2 is used in the following manner:

- Enter the top half with SYSCLK frequency from the left axis and move horizontally to the bus mode line selected by the PLL_CFG input signals.
- Descend vertically to the CPU frequency.
- Continue descending to the M divider line selected by the PLL_CFG signals.
- Move horizontally to the right to read the VCO frequency determined by this SYSCLK input, bus mode, and M divider.

The VCO output divided by M sets the CPU frequency but other circuitry in the processor probably limits the upper maximum of the CPU frequency of operation range. Therefore, both the VCO frequency and the CPU frequency determined from the graph must be checked against the appropriate hardware specification to see that they are within the range specified for the device in question.

An example of the clock relationships is plotted on the graph of Figure 2 as the heavy dashed line. The example shows that a 33.33-MHz SYSCLK input signal would require a 3:1 CPU:SYSCLK ratio to achieve a processor core frequency of 100 MHz. The 100-MHz CPU frequency is set by dividing the VCO frequency by two. The VCO will then operate within its specified operating range at 200 MHz.

As another example, the lighter dotted line on the graph reveals an alternate operating point of 40-MHz bus, 80-MHz CPU, and 160-MHz VCO using the 2:1 bus mode and the X2 VCO divider. The slower CPU frequency in the second example may appear less desirable, but the higher SYSCLK can result in faster accesses from external memory. The higher 40-MHz bus speed and associated faster external memory may cost more to implement, but applications with a low hit rate in the internal first-level cache might perform better with a lower CPU frequency and faster bus to external memory. This is the kind of trade-off which the flexibility of the PowerPC clocking modes provides.

The appendixes provide clock relationship graphs for the various PowerPC microprocessor family members. They may prove useful to the designer in relating CPU and VCO frequencies to SYSCLK and the PLL_CFG signals. These graphs should be used in conjunction with the hardware specifications which show the permissible range of operation of SYSCLK, CPU, and VCO frequency for the specific microprocessor.

Microprocessors are marketed based on the highest CPU frequency (horizontal scale) attainable. The upper limit of CPU frequency of operation is limited by internal speed paths or input/output timing as discussed in Section 1.3, “Timing Specification Tutorial.” The range of operation of the VCO and the dividers supported, will allow a wide range of CPU frequencies up to the maximum for a wide range of input (SYSCLK) frequencies.

1.2 Device Numbering Methodology

The application flexibility afforded by the wide range of CPU and SYSCLK frequencies has created confusion in specifying and ordering the appropriate microprocessor. Motorola provides for the device type, package type, CPU or processor frequency, and bus mode to be called out in the device number (as shown in Figure 3).

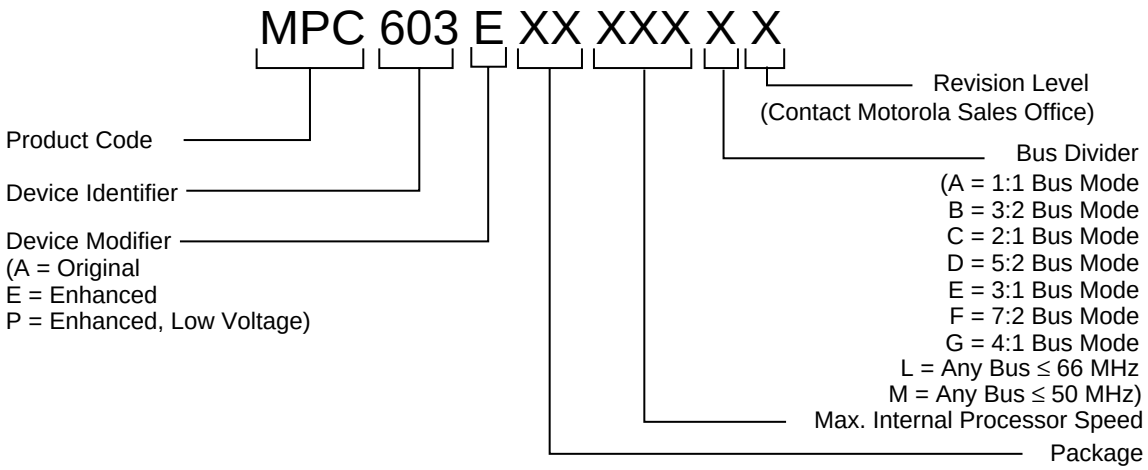


Figure 3. Motorola PowerPC Device Numbering Scheme

While a device may be purchased which is designated by only one of the many possible bus modes, the functionality of all dividers (and hence bus modes) designed into a device is present on all devices. Only a manufacturing defect, a timing concern, or a testing issue could limit operation in other modes. As shown in Figure 3, the “L” and “M” designations mean the part works in any supported bus mode. The M designator reflects a timing concern which limits the maximum bus frequency to 50 MHz or less. The L designates any bus of 66 MHz or less. To provide maximum flexibility, device numbers acknowledging that a part works in all modes has been added for most Motorola produced microprocessors.

Manufacturing defects in the divider circuits of an otherwise functional device are extremely rare.

1.3 Timing Specification Tutorial

A simplified logic diagram of a single path through a synchronous digital microprocessor will be used to discuss the relationship of electrical timing to CPU frequency. In Figure 4, clocked latches separate combinatorial logic which accomplishes the logic function of each stage of computing. An input buffer couples an input signal to the first latch and an output buffer couples the last latch to the output signal.

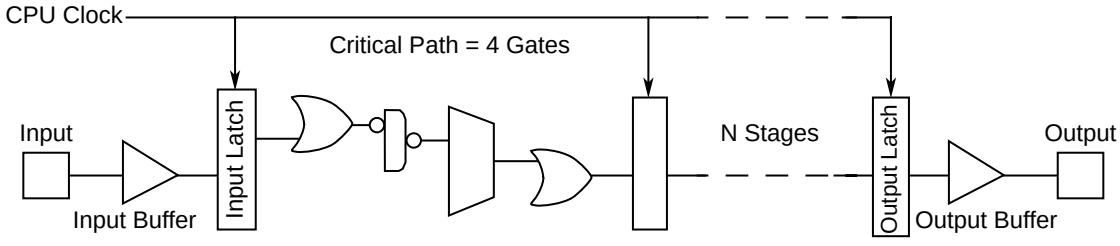


Figure 4. Simplified Synchronous Microprocessor Logic

A hypothetical distribution of gate delays across all variations in process parameters that may occur in manufacturing this device is shown in Figure 5. All gates in this simplified example are assumed to exhibit the same potential distribution of gate delays. A very fast device will have gate delays of 2 nanoseconds (ns) in the example, while a very slow device will have gate delays of 3 ns. The distribution is normally distributed around 2.5 ns. Note that a real microprocessor has many different sizes of logic gates with different gate delays to optimize for speed versus power consumption, but that complicates this simple example.

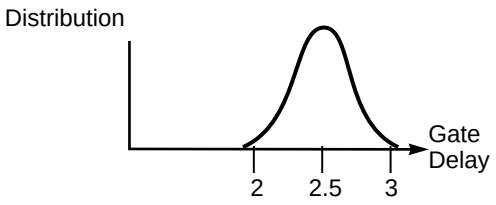
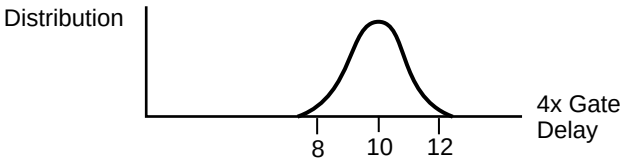


Figure 5. Hypothetical Distribution of Gate Delay with Process Variation

The maximum CPU frequency is determined by some critical path through the combinatorial logic. In Figure 6, this will be assumed to be the four gates shown. Their combined gate delays vary from 8 ns to 12 ns from the fastest to slowest processing. (For one silicon wafer, all gates could be expected to be similarly affected by process variations.) Signals cannot propagate through this critical path any faster than 8 ns (125 MHz) or any slower than 12 ns (83.33 MHz). Fifty percent of the devices should meet 100-MHz minimum operating frequency but only a very few would run at 125 MHz.



Notes:
1. fmax CPU = 125 MHz
2. fmin CPU = 83.33 MHz

Figure 6. Potential Critical Path Delay through Four Hypothetical Gates

Ideally, devices that meet the targeted CPU operating frequency will also meet input/output timing requirements. In fact the input/output timing specifications are set so that this is the likely outcome. After all, there are thousands of logic paths with millions of gates throughout the processor. If all of these paths meet their timing requirements, the performance of several dozen input/output buffers should not be the limiting factor. Therefore, input and output timing specifications are determined predominantly by what the buffers can be expected to deliver. Note that they may be modified somewhat where the external system timing requirements dictate a different specification.

In this example, on the slowest silicon an input signal must arrive a minimum of 3 ns (input setup time) before the clock edge in order to propagate through the input buffer and be present at the input to the input latch when it is clocked; see Figure 7. Because of the propagation delay, even on the fastest silicon a signal could actually be removed (negative input hold time) as early as 2 ns minimum before the clock edge and due to propagation delay through the input buffer, it would still be captured at the input latch. Generally, however, input hold time is specified to be a minimum of 0 ns hold time rather than a negative number.

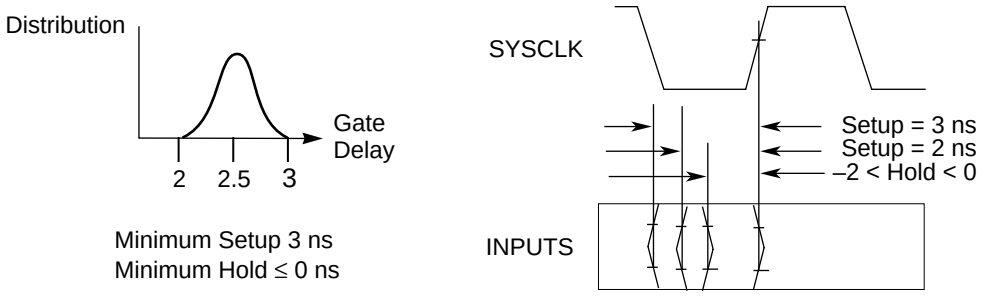


Figure 7. Input Buffer Gate Delay Related to Input Timing

On the slowest silicon an output signal will propagate through the output buffer and be present at the output pin a maximum of 3 ns (output valid or launch time) after the clock edge; see Figure 8. On the fastest silicon the output of the output latch could change at the clock edge and it would be a minimum of 2 ns (output hold time) before its change would propagate through the output buffer and be seen at the pin.

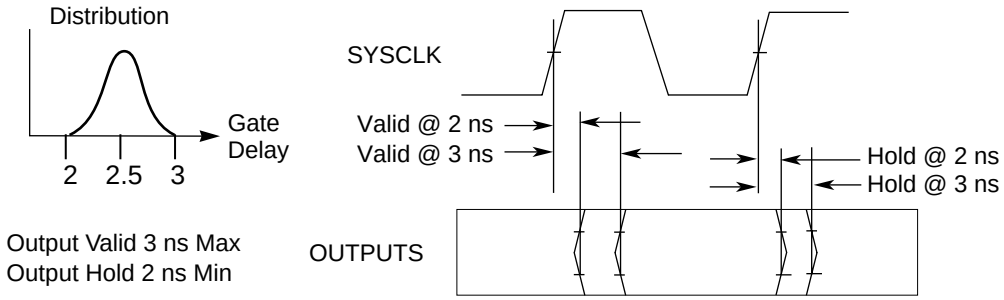


Figure 8. Output Buffer Gate Delay Related to Output Timing

As fabrication processes improve over time and gate delays decrease, output hold time which is the minimum gate delay through the output buffer, is the only parameter which does not “improve” from the system designer's perspective. If the external circuitry required the 2-ns minimum hold time to drive other circuitry in the system, having the signal speed up and invalidating sooner is not an improvement. As a result, the specification may be set slightly lower, perhaps at a 1 ns hold time, to allow for future process speed improvements.

Note that these input/output timing specifications are related to the same gate delay variation that governed maximum CPU frequency. They do not vary with the frequency of the bus clock (SYSCLK) that is supplied to the processor and is phase locked to a submultiple of the CPU frequency. Input/output timing can be specified to correspond to the gate delays required to achieve a given CPU frequency. In this hypothetical example, a minimum gate delay of 2.5 ns was required in the four critical path gates to achieve 100-MHz operation. Therefore, a similar 2.5 ns gate delay in the input and output buffers could be expected for a 100-MHz processor as well. A 125-MHz processor, on the other hand, would have very fast gates of 2 ns and would provide better input/output timing. (This is true in every respect except output hold time which would decrease or get worse as described previously).

In early versions of PowerPC microprocessor specifications, input/output timing was associated with SYSCLK times instead of CPU times. For the reason described above, input/output timing specifications for most of the devices have been changed; they are now specified by maximum CPU frequency.

1.4 Testing Issues

PowerPC microprocessors endure extensive tests before certification as ready for sale to customers. The devices are exercised with millions of test cases, over extremes of voltage and temperature, to guarantee the highest possible quality and reliability in the end application. However, real world limitations like test time and tester memory limit the number of possible test cases that can be tried on a device. Much of a microprocessor's functionality is "guaranteed by design" because, during design and verification, billions of test cases were successfully completed on models of the device or the device itself. During manufacture it is only necessary to exercise a sufficient number of tests to detect any defects introduced during manufacture or any process variations that would cause the device not to meet specification. It is not necessary to reverify the functional design.

Testing the complete functionality of a given device in all of the possible combinations of bus modes and VCO multipliers is not only prohibitively time consuming but it is also not necessary. Most of the logic of the device is confirmed in any bus mode. Only that part of the logic unique to the different bus modes themselves, such as the M and N dividers, needs to be confirmed in all modes. Therefore, the current Motorola PowerPC testing methodology exhaustively tests a device in one or two of the most frequently used bus modes and only minimally tests the remaining modes. Devices which pass all of these tests and meet the timing specifications for a given CPU frequency are marked as capable of operating in all bus modes—the "L" or "M" designations—at that CPU specification. If a customer desires exhaustive testing of a device in a unique bus mode (assuming it is different from what is normally tested) such a device can be ordered using a unique bus mode identifier. A customer should contact the local Motorola sales office regarding availability and pricing of such specially tested devices.

1.5 Special Timing Considerations

The flexibility of the many bus modes in the PowerPC microprocessors, encourages frequent switching of combinations of SYSCLK and CPU frequency, particularly during prototyping. In general, such configuration changes can be made during power down and will be effective after power-on reset. However, the following timing differences have been noted between the different bus modes and should be properly accounted for in system design or testing:

- MPC603—The address acknowledge ($\overline{\text{AACK}}$) signal may occur as early as one bus clock cycle after transfer start ($\overline{\text{TS}}$) or extended address transfer start ($\overline{\text{XATS}}$) is asserted unless the MPC603 is configured for 1:1 clock mode, then address acknowledge ($\overline{\text{AACK}}$) can be asserted no sooner that the second cycle following the assertion of $\overline{\text{TS}}$.
- MPC604—The following hold true:
  - The address bus busy ($\overline{\text{ABB}}$) and data bus busy ($\overline{\text{DBB}}$) signals go to high impedance one-half bus cycle after either $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is negated. However, if the MPC604 is configured for 3:1 clock mode then $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ go to high impedance two-thirds bus cycle after $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is negated. Or if the MPC604 is configured for 3:2 clock mode then $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ go to high impedance one-third bus cycle after the corresponding signal is negated.
  - The address retry ($\overline{\text{ARTRY}}$) and shared ($\overline{\text{SHD}}$) signals may be asserted by multiple devices, all of which restore it high. To avoid bus conflict, the signal is released to the high impedance state for a period, then driven high for a period, as follows:
    - 1:1 and 2:1 bus ratio—High-impedance for one-half bus cycle, high for one bus cycle, then high-impedance
    - 3:1 bus ratio—High-impedance for one-third bus cycle, high for two-third bus cycle, then high-impedance
    - 3:2 bus ratio—High-impedance for one-third bus cycle, high for one bus cycle, then high-impedance

- MPC604e—The following hold true:
  - The $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ signals go to high impedance for a fraction of a bus cycle (see Table 2) after either $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is negated.
  - The $\overline{\text{ARTRY}}$ and $\overline{\text{SHD}}$ signals may be asserted by multiple devices, all of which restore it high. To avoid bus conflict, the signal is released to the high impedance state for a fraction of a bus cycle (see Table 2), then driven high for exactly one bus cycle, then three-stated.

Table 2. Precharge and Three-state Widths for $\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$, $\overline{\text{ABB}}$, and $\overline{\text{DBB}}$

Processor to Bus Frequency Ratio	MPC604			MPC604e		
	$\overline{\text{ABB}}$, $\overline{\text{DBB}}$ precharge width in fractional bus cycles	$\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$		$\overline{\text{ABB}}$, $\overline{\text{DBB}}$ precharge width in fractional bus cycles	$\overline{\text{ARTRY}}$, $\overline{\text{SHD}}$	
		Pre-precharge three-state width in fractional bus cycles	Precharge width in bus cycles		Pre-precharge three-state width in fractional bus cycles	Precharge width in bus cycles
1:1	1/2	1/2	1	1/2	1/2	1
3:2	1/3	1/3	1	2/3	2/3	1
2:1	1/2	1/2	1	1/2	1/2	1
5:2	N/A	N/A	N/A	3/5	3/5	1
3:1	2/3	1/3	2/3	2/3	2/3	1
4:1	N/A	N/A	N/A	9/12	9/12	1

Part 2 Appendixes

The following pages provide graphs describing the relationships between SYSCLK, CPU frequency, and VCO frequency for the supported M and N dividers in each device. SYSCLK and CPU frequency are related by the value of the N divider or bus mode. CPU frequency and VCO frequency are related by the M divider. On early devices the M and N dividers were configured by PLL_CFG2–PLL_CFG3 and PLL_CFG0–PLL_CFG1, respectively. In later devices, PLL_CFG0–PLL_CFG3 are decoded to select both dividers. Table 3 provides a consolidated reference of the PLL_CFG0–PLL_CFG3 settings required to select the dividers.

Some combinations of PLL_CFG settings and SYSCLK input may select CPU or VCO frequencies which are not achievable or where proper operation is not guaranteed. The hardware specification for each device should be consulted to determine the range of CPU and VCO frequencies which are supported.

The MPC105 and MPC106 are included in Table 3 for reference. While not microprocessors, they use the same PLL circuitry as the PowerPC microprocessors to synchronize their internal core frequency to the PCI (Peripheral Component Interconnect) or bus clock

As a supplement to the graphs, this appendix provides a handy reference for the multiplication of the common values of bus frequency and every bus multiplier to arrive at CPU frequency. This is simply a multiplication table and should only be used with the other information provided in this application note for complete understanding.

Table 3. Consolidated PLL_CFG0–PLL_CFG3 Settings for Clock Dividers

		N Divider or Bus Mode										
M Divider	**Device**	**1:1**	**3:2**	**2:1**	**5:2**	**3:1**	**7:2**	**4:1**	**9:2**	**5:1**	**11:2**	**6:1**
X2	MPC602	Test*	—	0100	—	1000	—	—	—	—	—	—
	MPC603	0000	—	0100	—	1000	—	1100	—	—	—	—
	MPC603e (PID6-603e)	0000	1100	0100	0110	1000	1110	1010	—	—	—	—
	MPC603e (PID7v-603e)	—	—	0100	0110	1000	1110	1010	0111	1011	1001	1101
	MPC604	0000	1100	0100	—	1000	—	—	—	—	—	—
	MPC604e	0000	1100	0100	0110	1000	—	1010	—	—	—	—
	MPC105	0000	—	0100	—	—	—	—	—	—	—	—
	MPC106	0000	—	0100	—	1000	—	—	—	—	—	—
X4	MPC602	—	—	0101	—	—	—	—	—	—	—	—
	MPC603	0001	—	0101	—	1001	—	1101	—	—	—	—
	MPC603e (PID6-603e)	0001	—	0101	—	—	—	—	—	—	—	—
	MPC603e (PID7v-603e)	—	—	0101	—	—	—	—	—	—	—	—
	MPC604	0001	—	0101	—	—	—	—	—	—	—	—
	MPC604e	0001	—	0101	—	—	—	—	—	—	—	—
	MPC105	0001	—	0101	—	—	—	—	—	—	—	—
	MPC106	0001	—	0101	—	1001	—	—	—	—	—	—
X8	MPC602	—	—	—	—	—	—	—	—	—	—	—
	MPC603	—	—	—	—	—	—	—	—	—	—	—
	MPC603e (PID6-603e)	0010	—	—	—	—	—	—	—	—	—	—
	MPC603e (PID7v-603e)	—	—	—	—	—	—	—	—	—	—	—
	MPC604	0010	—	—	—	—	—	—	—	—	—	—
	MPC604e	0010	—	—	—	—	—	—	—	—	—	—
	MPC105	0010	—	—	—	—	—	—	—	—	—	—
	MPC106	0010	—	—	—	—	—	—	—	—	—	—

Table 3. Consolidated PLL_CFG0–PLL_CFG3 Settings for Clock Dividers (Continued)

		N Divider or Bus Mode										
M Divider	**Device**	**1:1**	**3:2**	**2:1**	**5:2**	**3:1**	**7:2**	**4:1**	**9:2**	**5:1**	**11:2**	**6:1**
Bypass	MPC602	0011	(SYSCLK drives processor core frequency directly; bus is in 1:1 mode; Input/Output timing relative to SYSCLK is not guaranteed)									
	MPC603	0011										
	MPC603e (PID6-603e)	0011										
	MPC603e (PID7v-603e)	0011										
	MPC604	0011										
	MPC604e	0011										
	MPC105	0011										
	MPC106	0011										
Clock-Off	MPC602	1111										
	MPC603	1111										
	MPC603e (PID6-603e)	1111										
	MPC603e (PID7v-603e)	1111										
	MPC604	1111										
	MPC604e	1111										
	MPC105	1111										
	MPC106	1111										

Note: 1:1 mode on the MPC602 is for testing purposes only.

Figure 9 provides the clock relationship for the MPC602.

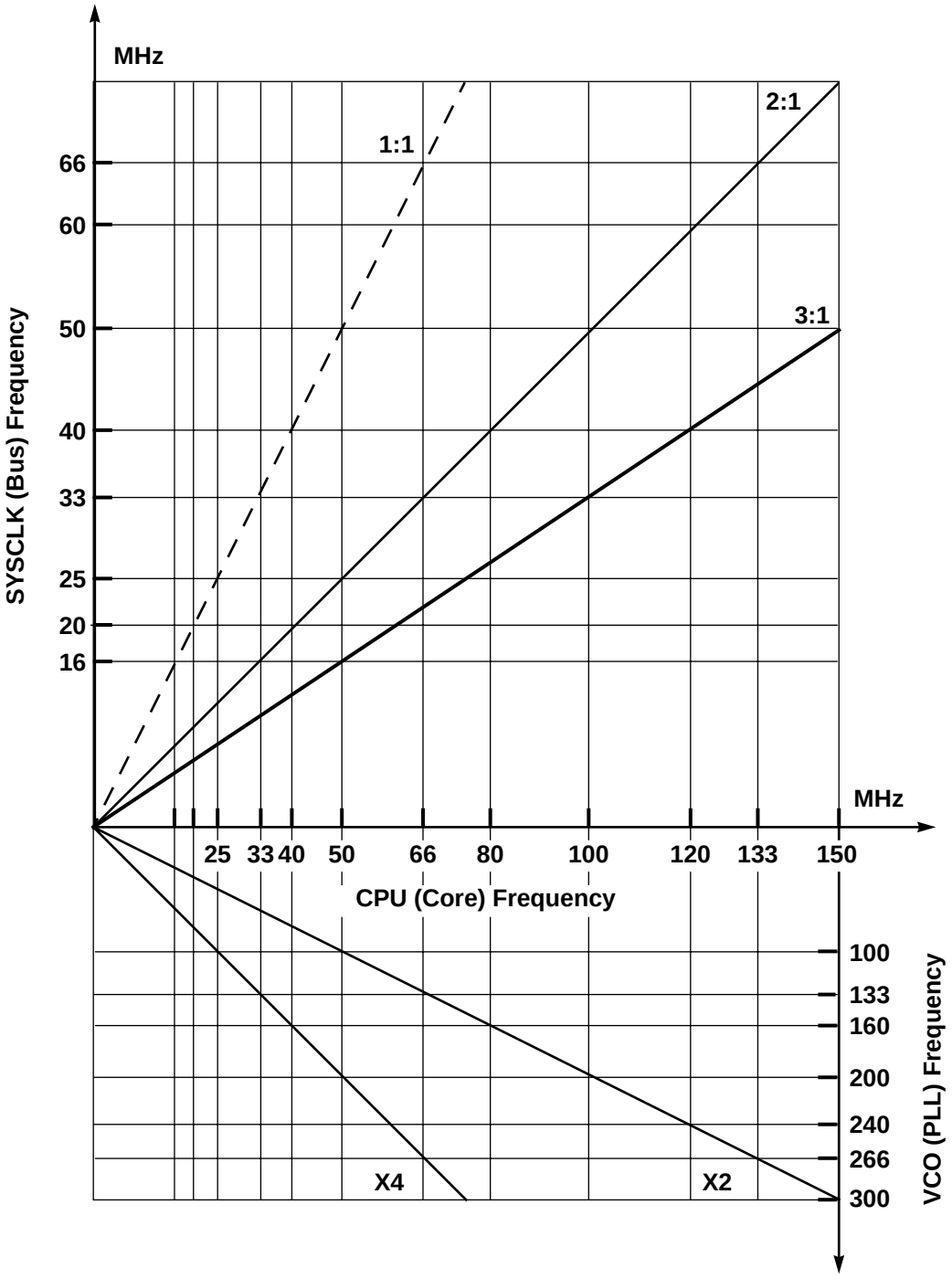


Figure 9. MPC602 Clock Relationships

Figure 10 provides the clock relationship for the MPC603.

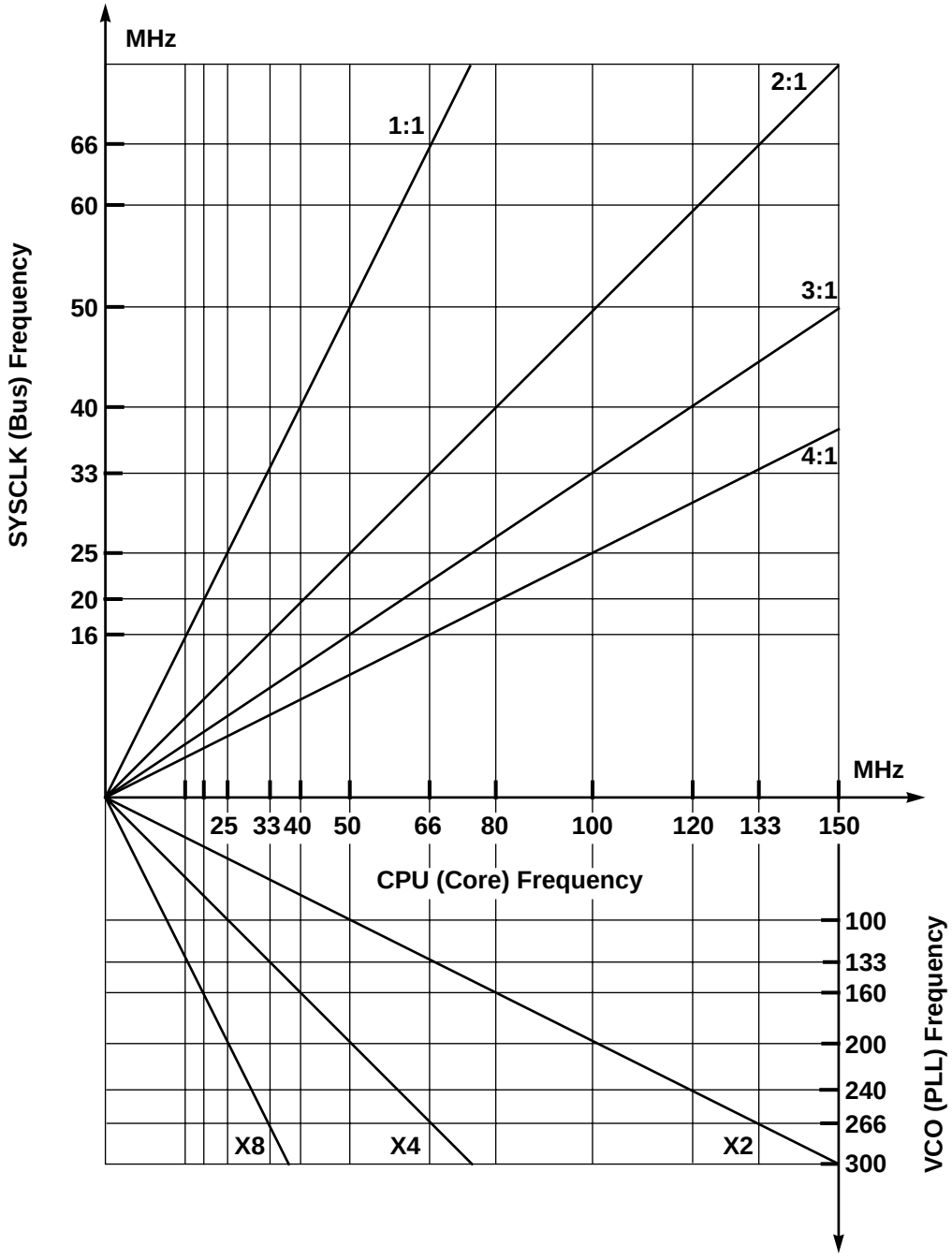


Figure 10. MPC603 Clock Relationships

Figure 11 provides the clock relationship for the MPC603e (PID6-603e).

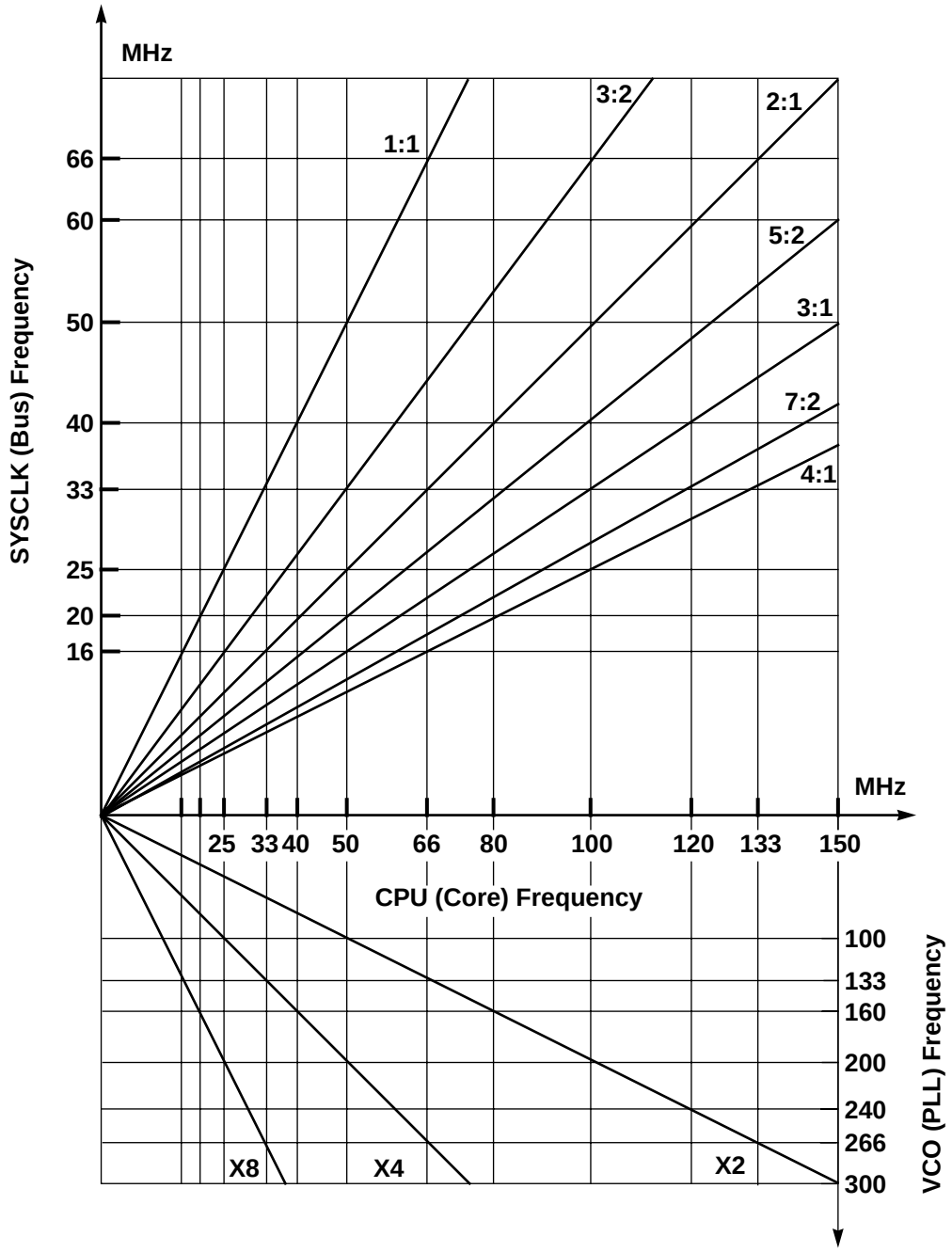


Figure 11. MPC603e (PID6-603e) Clock Relationships

Figure 12 provides the clock relationship for the MPC603e (PID7v-603e).

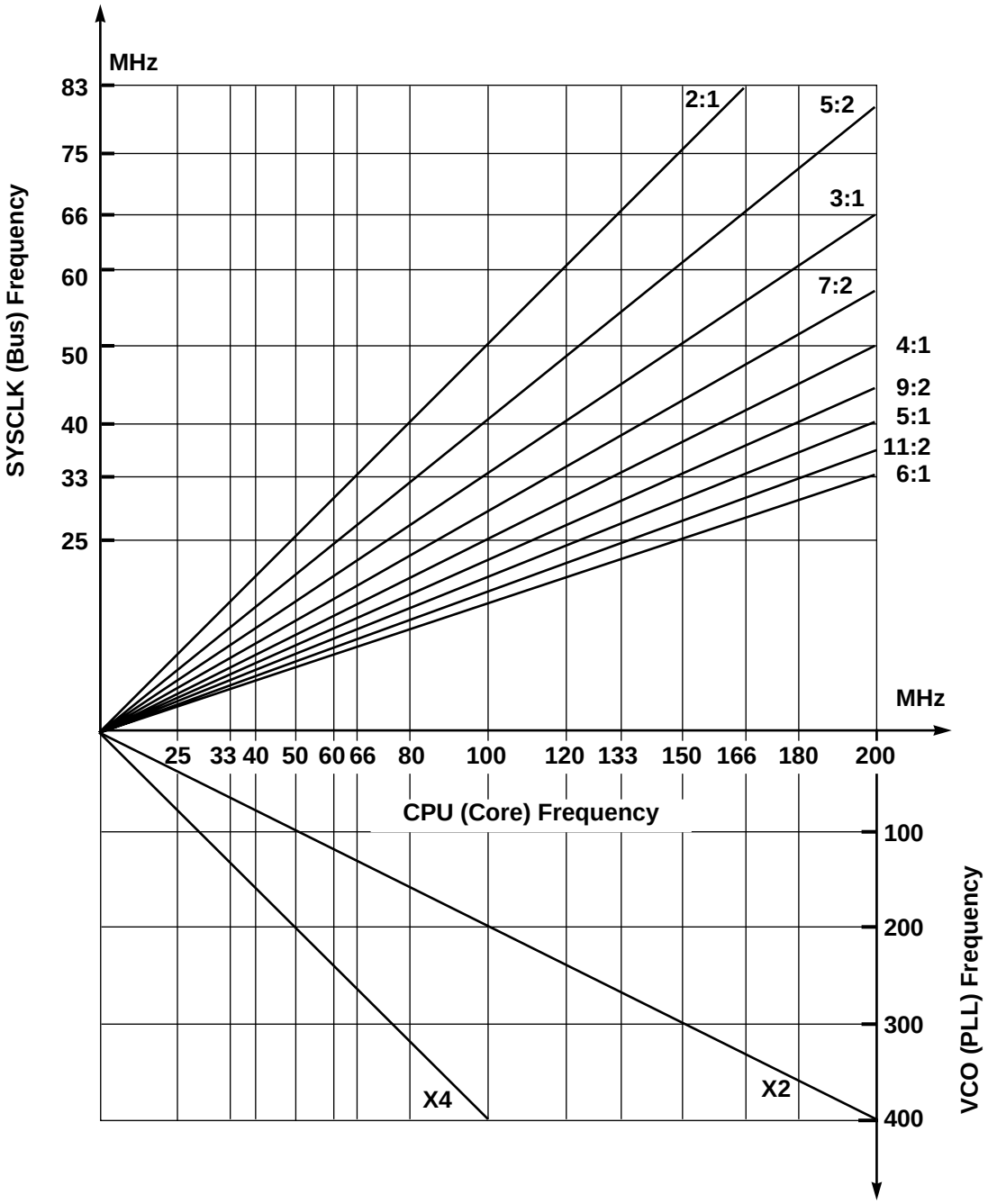


Figure 12. MPC603e (PID7v-603e) Clock Relationships

Figure 13 provides the clock relationship for the MPC604.

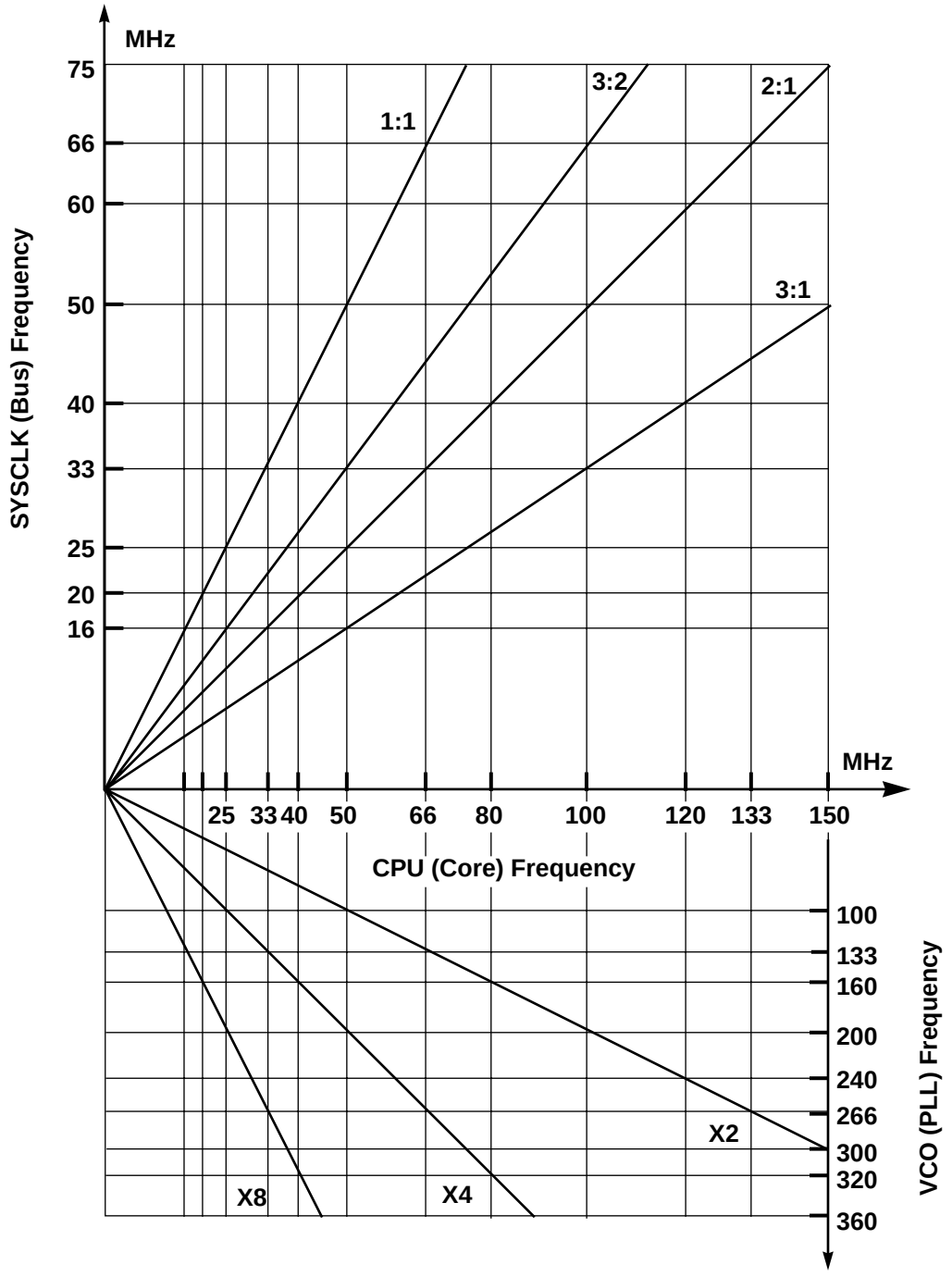


Figure 13. MPC604 Clock Relationships

Figure 14 provides the clock relationship for the MPC604e.

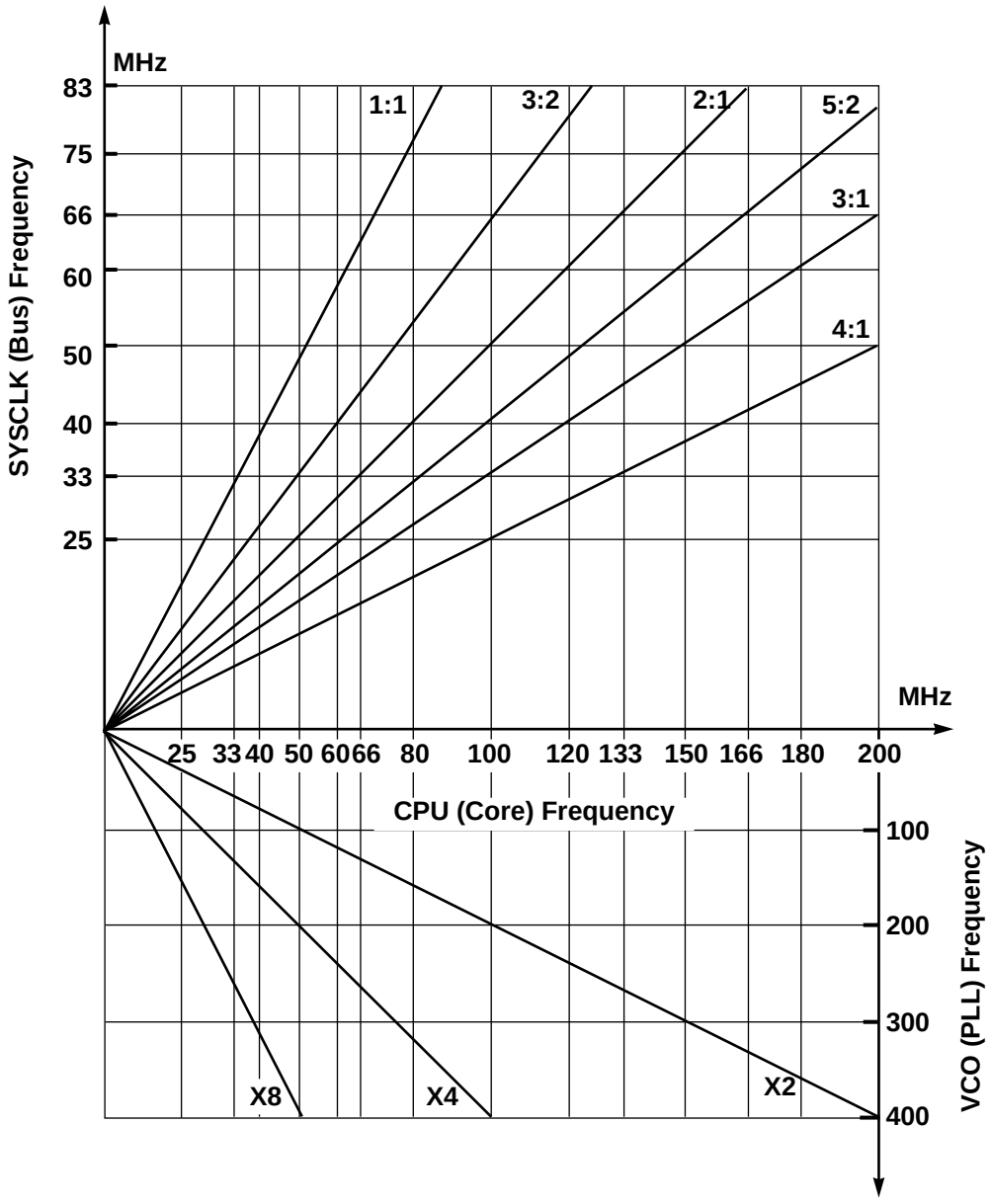


Figure 14. MPC604e Clock Relationships

Figure 15 provides the clock relationship for both the MPC105 and MPC106 microprocessors.

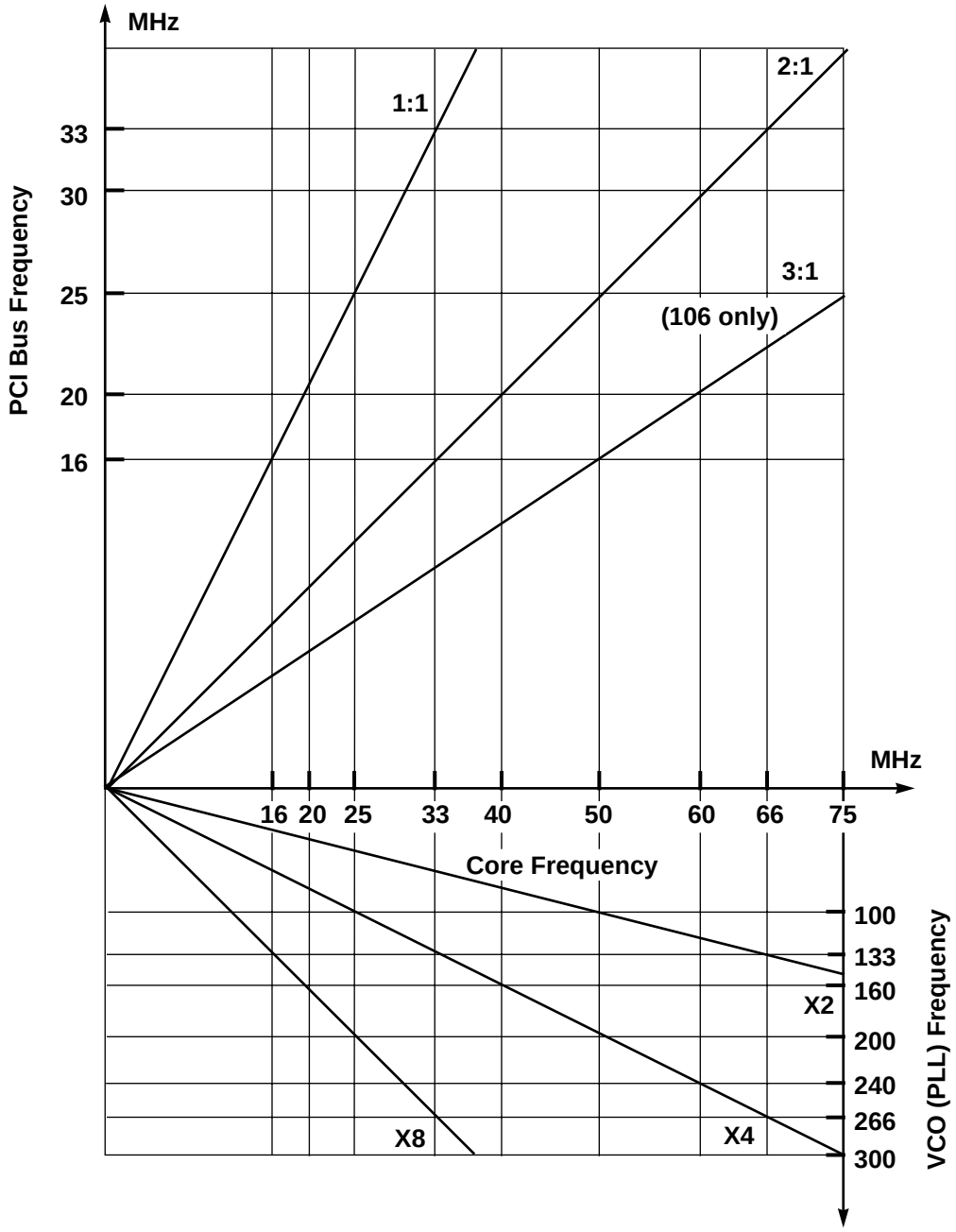


Figure 15. MPC105/MPC106 Clock Relationships

Table 4. CPU Frequencies for Common Bus Frequencies and Multipliers

	Bus to CPU Multiplier										
	1:1	**3:2**	**2:1**	**5:2**	**3:1**	**7:2**	**4:1**	**9:2**	**5:1**	**11:2**	**6:1**
Device Applicability											
MPC602	x	—	x	—	x	—	—	—	—	—	—
MPC603	x	—	x	—	x	—	x	—	—	—	—
MPC603e (PID6-603e)	x	x	x	x	x	x	x	—	—	—	—
MPC603e (PID7v-603e)	—	—	x	x	x	x	x	x	x	x	x
MPC604	x	x	x	—	x	—	—	—	—	—	—
MPC604e	x	x	x	x	x	—	x	—	—	—	—
Bus Frequency (MHz)	**CPU Frequency (MHz)**										
83.33	83	125	167	208	250	292	333	375	417	458	500
75	75	113	150	188	225	263	300	338	375	417	450
66.67	67	100	133	167	200	233	267	300	333	367	400
60	60	90	120	150	180	210	240	270	300	330	360
50	50	75	100	125	150	175	200	225	250	275	300
40	40	60	80	100	120	140	160	180	200	220	240
37.5	38	56	75	94	113	131	150	169	188	206	225
33.33	33	50	67	83	100	117	133	150	167	183	200
25	25	38	50	63	75	88	100	113	125	138	150

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