PowerPC™

Application Note
Spreadsheet Estimation of CPU-DRAM Subsystem Power Consumption

As the energy efficiency of computers becomes more important to consumers, the early estimation, preferably during the design phase, of system power consumption becomes vital. In addition, since the CPU-DRAM subsystem (comprising CPU, DRAM, DRAM controller, and address/data buffers) forms the core of many of today's desktop and portable computers, accuracy in the assessment of the power requirements of this block becomes even more important. Manual calculations of power consumption tend to be time-consuming and the possibility of introducing errors is great, especially with complex microprocessors that support a wide range of bus transactions and low-power modes. One solution for this dilemma is a spreadsheet. A spreadsheet can be used to automate the calculation, reducing both the time taken and the likelihood of errors. A spreadsheet can also provide a range of other data and can be used to vary parameters that would be hard to do practically, such as cache hit rates. In today's fast moving world of electronics, spreadsheets also have the advantage of being relatively easy to modify.

This document discusses a Microsoft® Excel 4.0 document—DRAMP.XLS (referred to as DRAMP). DRAMP can be obtained via the internet at the following World Wide Web Address—www.mot.com/powerpc/support/hw-design. DRAMP was created for the designers of low-power, uni-processor systems using PowerPC™ 60x microprocessors.

In this document, the term "601" is used as an abbreviation for the phrase "PowerPC 601™ microprocessor," the term "603" is used as an abbreviation for the phrase "PowerPC 603™ microprocessor," the term "604" is used as an abbreviation for the phrase "PowerPC 604™ microprocessor," and the term "60x" is used to denote a 32-bit microprocessor from the

(rotated text in right margin) CPU-DRAM Application Note

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PowerPC architecture family that conforms to the bus interface of the 601, 603, and 604 microprocessors. 60x processors implement the PowerPC architecture as it is specified for 32-bit addressing, which provides 32-bit effective (logical) addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits (single-precision and double-precision).

This spreadsheet, designed for FP-DRAM and EDO-DRAM, allows the power and energy characteristics of a 60x-DRAM subsystem to be easily estimated. Although there are restrictions on the types of subsystem architecture, DRAMP assumes the design architecture is as shown in Figure 1. In particular, at least one bank of buffers is used to buffer the CPU's data bus and a bank of buffers/latches is used to drive the memory array's address bus. It supports designs with up to twelve banks of page-mode DRAM, and integrates the energy characteristics of the DRAM controller into the overall output. Since DRAMP is targeted toward designers of low-power systems it assumes the processor's level-1 (L1) cache operates in copyback mode. It also assumes, for the sake of simplicity, that all transactions are L1 cache linefills or cast-outs, and allows the user to vary the ratio of these transactions. (This assumption is invalid if, unlike 60x microprocessors, the microprocessor does not operate a write-allocate policy.) Although the spreadsheet is primarily intended for designs that utilize discrete address and data bus buffers, it can also be used to analyze more highly integrated systems. Some of the key features which are supported are highlighted in following sections.
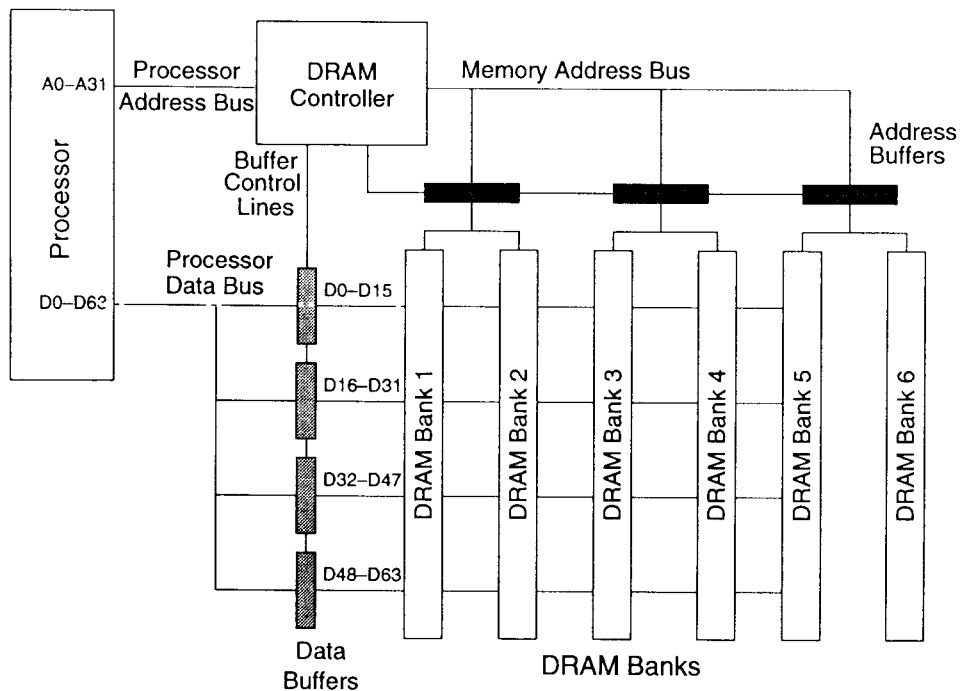

Figure 1. CPU-DRAM Block Diagram

1.1 Features Supported

The following features are supported in DRAMP:

- 601, 603, and 604 microprocessors
- Programmable bus timing for linefills and cast-outs
- Supports up to 12 banks of DRAM
- Address buffers of any width
- Mixed supply voltage systems
- CMOS technology-based address and data buffers

One of the aims in developing DRAMP was to allow an easy estimation of the CPU-DRAM subsystem's power consumption to be carried out during the initial design stages. For occasions where the quantity and organization of data and address bus buffers are not known, the spreadsheet can automatically calculate the details using one of two algorithms. Alternatively, if the level of buffering has already been determined, DRAMP can simply work with user-entered values. In order to decide which action to take, DRAMP looks for keywords in defined cell locations to control its operation. One of these locations, the "System-Address Bus Buffering" field allows three valid string entries—CNTRL, NUM, and FIXED. These strings perform as follows:

- CNTRL—The spreadsheet calculates the number of address bus buffers required (for a given memory topology) based on an algorithm that seeks to minimize address buffer control logic.

  In this mode, a buffer will not be used to drive an additional bank if it cannot drive the full-DRAM loading presented by that bank.

- NUM—The algorithm seeks to minimize the number of buffers required by loading them (in terms of bus capacitance) as fully as possible.

  In this mode, a new buffer is only added when driving an additional DRAM would exceed the current buffer's maximum capacitive loading. Since these two modes can produce dramatically different results (at least in terms of the numbers of buffers required), the user should compare them carefully to judge the benefits of each scheme.

- FIXED—The spreadsheet takes user-entered buffer numbers to calculate its results.

In general, a number of DRAM ICs are required to construct a memory bank whose data path width matches the processor's data bus. Because of this, the capacitive loading presented by each bank to the memory array's data bus is usually much less than that presented to the memory array's address bus. This loading difference allows a data bus buffer to drive more memory banks than an address bus equivalent. This fact is reflected in the spreadsheet's treatment of data buffers. As with address buffers, the spreadsheet can calculate the number required; however, in this instance, only one algorithm is required or used. If the "System-Data Buffer Configuration" field is set to CAP or FIXED they behave in the following manner:

- CAP—The spreadsheet calculates the number required based on an algorithm that maximizes the capacitive loading per buffer.
- FIXED—DRAMP takes user-entered values.

Table 1 and Table 2 show a portion of DRAMP with data for two sample 603-based systems (labelled 'System A' and 'System B'). Table 1 and Table 2 show the area of spreadsheet where the user enters processor and system characteristics, respectively.

Table 1. DRAMP Processor Characteristics (Input)

Processor Characteristics	System A	System B
Internal or CPU clock speed (MHz)	75	66
Bus width including parity [if used] (bits) (*1)	64	64
Internal (CPU)/bus clock ratio	2	2
Cache accesses/CPU clock (*8)	2	2
Cache sector/line size (bytes)	32	32
Power dissipation (64-bit data bus) mW/MHz	29	29
Power dissipation (32-bit data bus) mW/MHz	29	29
Power dissipation (internal access) mW/MHz	29	29
Power dissipation in DOZE mode (mW/MHz)	5	5
Power dissipation in NAP mode (mW/MHz)	2	2
Power dissipation in AC SLEEP mode (mW/MHz)	1	1
Power dissipation in DC SLEEP mode (mW)	1	1

Note: The data shown here represents estimates taken from hardware specifications. The system design variables do not represent a real system.

Table 2. DRAMP System Characteristics (Input)

System Design Variables	System A	System B
Evaluation period (µs) (stat)	500	500
Fraction of evaluation period available for power saving (%) (stat)	25	17
Average L1 cache miss rate to RAM (%) (stat)	10	10
Average number of cast outs/ L1 cache miss (%) (stat)	20	20
DRAM total required (MBytes) (*2)	8	8
Data bus cap loading CPU-data buffer I/F per pin (pF) (*5)	7	7
L1 cache cast-out duration (CPU bus clocks)	28	28
L1 cache linefill duration (CPU bus clocks)	28	28
Address Latch Configuration—NUM, CNTRL, or FIXED (*9)	NUM	NUM
Data Buffer Configuration—CAP or FIXED (*10)	CAP	CAP

1.2 The Spreadsheet Calculation

In terms of output, DRAMP generates both the total energy consumed and the average power dissipation for both the entire subsystem and for each type of component. In addition, intermediate data generated as a by-product of the calculation provides the user with valuable system information such as average burst frequency, average power consumption per DRAM IC, and average inter-linefill period.

The final results are based on a specified evaluation period. This duration is split into an active period and low-power period by a user-defined ratio. The power figures for both of these periods are worked out separately and summed to produce totals. The inclusion of a low-power period in the calculations allows the design to be exercised in a manner that represents the real-life operation of power-saving systems.

No accesses to DRAM are made during the low-power period, so the power consumption is simply the total quiescent consumption of the buffer and memory ICs plus the low-power mode consumption of the processor and DRAM controller. Since the 603 supports four power-saving modes (doze, nap, AC sleep, and DC sleep), DRAMP generates five sets of results based on the state of the processor during this period—the fifth set provides results for a processor not placed in a low-power mode.

Since not all the devices in the subsystem are necessarily exercised by every DRAM access, the active period figures are made up of an "employed" portion (corresponding to devices exercised by an access) and an "unemployed" portion (corresponding to devices that do not take part in an access). By subtracting the number of buffers/DRAMs in a bank from the total number in the design, the spreadsheet can calculate both the number of unemployed devices and their dissipation. The power dissipation of an employed DRAM or CPU is calculated by taking a value from the hardware specification and interpolating linearly to find the figure for a given frequency. The dissipation of an employed address/data buffer is based on the following equation.

$$PD_n = \underbrace{(I_{cc} \times V_{cc})}_{A} + \underbrace{(C_{pd} \times (V_{cc})^2 \times f_i)}_{B} + \underbrace{\sum_{n=1}^{n} (C_n \times (V_{cc})^2 \times f_o)}_{C}$$

where:

PD_n = Power dissipation of a buffer with n outputs

I_{cc} = Quiescent current consumption

C_{pd} = Power dissipation capacitance

C_n = Capacitive load on output n

V_{cc} = Supply voltage

f_i = Input frequency

f_o = Output frequency

This equation gives the power dissipation of a CMOS buffer with n outputs. The equation can be broken down into the following three components:

- Term A represents the non-frequency related (quiescent) power dissipation.

- Term B represents a dissipation related to the frequency seen at the buffer's inputs.

- Term C represents the dissipation due to the charging/discharging of capacitive loads by the buffer outputs.

A and B can both be calculated using user-entered values for the buffer's supply voltage, quiescent current, and power-dissipation capacitance. The spreadsheet calculates the average operating frequency of the DRAM's address and data buses (DRAMP equates the DRAM address bus frequency to twice that of the microprocessor's burst frequency) and this is the frequency which is used for both f_i and f_o. Although not all CMOS logic manufacturers specify the power consumption of their buffers in terms of a power-dissipation capacitance (C_{pd}), it is generally simple to derive this from details provided. Finally, since DRAMP provides total and average power results, a simplified version of term C is used in the spreadsheet.

1.3 CPU-DRAM Interactions

In a real system, the number of DRAM accesses made during a given interval will depend on many parameters, including the software being executed, the caching scheme adopted, and the DRAM access time. In order to simplify the implementation of the spreadsheet, three key assumptions have been made. While these assumptions will not hold true for many types of systems, they are considered valid for the market segment targeted by the spreadsheet (that is, simple, low-power, PowerPC microprocessor-based systems). The assumptions are as follows:

1. All DRAM is cached by the microprocessors' on-chip, L1, copyback cache.

2. There is no level-2 (L2) cache.

3. The DRAM is not shared with another microprocessor.

These three restrictions mean that the only bus transactions we need to consider (with respect to the DRAM block) are L1 cache linefills and cast-outs. By determining the frequency of these transactions we can calculate most of the subsystem's power and energy characteristics. The effect of software is modelled through two user-entered parameters—the L1 cache miss rate and the ratio of cache misses to cast-outs. From this miss-rate and the average number of L1 accesses per clock, the spreadsheet can determine the average period between L1 cache linefills. User-entered cast-out and linefill timing together with the miss-to-cast-out ratio allows calculation of the average linefill and cast-out frequencies. From these two frequencies, the average operating frequencies of the DRAM address and data paths can be determined, thus enabling the dissipation of address buffers, data buffers, and DRAM to be calculated

1.4 Spreadsheet Organization

The DRAMP spreadsheet is organized very simply, a single column is used to represent a single CPU-DRAM configuration. This allows easy side-by-side comparisons to be performed over a wide range of statistics. Labels down column A indicate the data to be entered on a given row. This data falls into two clear categories—either device-specific hardware specification information or system characteristics. Following the user-entered data is an intermediate results section which can be easily collapsed if the user is only interested in the final output. Final results, including total energy consumption and average power dissipation, are provided for the subsystem as a whole and for each type of component, thus allowing the designer to assess the impact of each choice of component. The format of the final system results section is shown in Table 3.

Table 3. DRAMP Final Results (Output)

System—Final Results	System A	System B
Total energy dissipation during active period (μJ)	1618	1694
Total energy dissipation without low-power modes (μJ)	2088	1984
Total energy dissipation using doze mode (μJ)	1858	1853
Total energy dissipation using nap mode (μJ)	1809	1823
Total energy dissipation using AC sleep mode (μJ)	1749	1782
Total energy dissipation using DC sleep mode (μJ)	1701	1751
Average power dissipation during active period (W)	4.31	4.08
Average power dissipation without low-power modes (W)	4.18	3.97
Average power dissipation using doze mode (W)	3.72	3.71
Average power dissipation using nap mode (W)	3.62	3.65
Average power dissipation using AC sleep mode (W)	3.50	3.56
Average power dissipation using DC sleep mode (W)	3.40	3.50

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Document Comments: FAX (512) 891-2638, Attn: RISC Applications Engineering.
World Wide Web Address: http://www.mot.com/powerpc/

Ⓜ **MOTOROLA**   ◊ 1ATX35241-0 PRINTED IN USA 2/96 IMPERIAL LITHO 22034 5 000 RISC YGAHAA   **AN1272/D**