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APPLICATION NOTE

AN1508

High Frequency Design Techniques and Guidelines for Bipolar Gate Arrays

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INTRODUCTION

Data processing system clock rates have seldom exceeded 600 MHz. ECL gate arrays can easily meet all requirements for these system speeds. More recently, optical fiber transmission systems have accelerated the need for very high speed (1 to 10 Gb/s) multiplexers, demultiplexers, and line driver outputs. Digital circuits operating over 1 GHz have primarily been implemented as custom silicon or GaAs circuits. In general, silicon process technologies are preferred because of lower cost, a large number of manufacturers, higher reliability, and smaller delay and threshold variations over process, voltage, and temperature (PVT). To achieve the lowest development cost and shortest design cycle, semicustom gate arrays are preferred. However, the performance of ECL gate arrays was typically under 1 GHz. In the past few years, bipolar process improvements have made it possible to efficiently operate ECL gate arrays at frequencies up to 2.5 GHz.

OBJECTIVE

This application note will discuss present design techniques and guidelines regarding high frequency (>1GHz) digital bipolar (ECL & ETL) gate arrays. Section 1 provides information for the selected array type. Section 2 will discuss I/O and package frequency limitations and techniques for maximizing performance. Section 3 provides internal macro information and methods for achieving 2.5 GHz macro operation. Sections 4, 5, and 6 discuss general high speed design guidelines, clock distribution techniques, and high frequency design examples, respectively. Lastly, section 7 summarizes the use of bipolar gate arrays at high frequencies.

1. ASIC SELECTION FOR HIGH SPEED APPLICATIONS

To provide the reader with descriptive examples and current information, Motorola's MCA3 ETL (**E**CL & **T**TL **L**evels) arrays have been selected for representing a production ready high frequency bipolar gate array family. These arrays contain an internal ECL core with universal I/O cells capable of ECL to TTL and TTL to ECL translation. They have been used to implement 2.5 GHz counters, multiplexers, and demultiplexers.

The complete MCA3 array family is summarized in Table 1-1. In addition to the three ETL arrays, two ECL (ECL I/O) arrays capable of operating up to 1.66 GHz are manufactured. The maximum MCA3 ETL array operating frequencies are shown in Table 1-2.

Refer to the MCA3 ETL Series Design Manual[1] and the MCA3 ECL Series Design Manual[2] for a complete description of these products.

Table 1-1 MCA3 Family Array Types and Features

Array	Equivalent Gates	Min Addressable Units	Universal I/O Cells	Die Size (mils)	Packages
MCA750ETL	858	96	42	139x168	64 QFP
MCA3200ETL	3570	440	120	276x276	160 QFP 169 PGA
MCA6200ETL	6915	900	168	352x352	224 PGA 328 TAB
MCA2200ECL	2412	272	192[a]	212x212	135 PGA
MCA10000ECL	12402	1656	424[a]	385x385	235 PGA 289 PGA 360 TAB

a. Includes dedicated input and output cells.

Table 1-2 MCA3 ETL Maximum Array Operating Frequencies

Signal Type		Max. Freq.(MHz) (50% Duty Cycle) Single-ended	Max. Freq.(MHz) (50% Duty Cycle) Differential
ECL / PECL	Input	2500 [a]	2500
	Output	1600	2500
TTL	Input	250	
	Output	100 [b]	

a. Input Frequencies up to 2.5 GHz can be obtained with a sinusoidal AC coupled single-ended input.
b. With a load of 15 pF.

2. PACKAGE, I/O MACRO, AND VOLTAGE LEVEL CONSIDERATIONS

2.1 PACKAGE

Typical bipolar gate array packages are the multilayer PC board type, plastic quad flat pack (QFP) and the multilayer ceramic pin grid array (PGA), with both wire and TAB bonding. At high frequencies, crosstalk and reflections in these packages become substantial and imperative to chip performance. Several techniques such as pin selection, package design and signal termination can be adopted to minimize these effects.

Motorola's MicroCool™ 64 QFP and 160 QFP packages have controlled 50 ohm transmission lines between the package perimeter and the die. A multilayer printed circuit (PC) board is used in the construction of these packages. The result is a package that allows higher input and output frequencies. Exposed on top of these packages is a heat slug. The die is mounted upside down on the bottom of the heat slug thus providing excellent thermal characteristics.

2.1.1 Pin Selection

Fundamental guidelines for high frequency pin selection are:

1) For QFP packages, the package pins toward the middle of each side generally result in the lowest total input capacitance since the package leads are shortest and the metal length on the chip from the die pad to the input or output is near the minimum.

2) For PGA packages, the package pins in the inner rows toward the middle of each side generally have the lowest capacitance since the package leads are shortest, however, the metal length on the chip from the die pad to the input or output circuit may not be near the minimum. Die pads located towards the center of each edge of the chip typically have the least amount of metal connecting the I/O cell. To select package pins with the lowest capacitance, the designer should analyze both the package pin location and die pad position as discussed above.

3) Signal leads that are adjacent to high frequency signal leads and on the same package signal plane may be grounded or set to a DC supply voltage (i.e, V_{CC}, V_{TT}, or V_{EE}). This will aid in electrically isolating the high frequency signals from the adjacent leads thus reducing crosstalk.

2.1.2 Package Design

A high speed package should have a low dielectric constant e_r (<4). A reduction in e_r lowers the capacitances related to signal-line discontinuities and results in improved signal bandwidth, propagation velocity, and attenuation[3]. Multi-layer packages are essential, primarily due to: 1) reducing the inductance of the ground path (V_{CC}); 2) controlling the signal line impedance; and 3) reducing crosstalk among signal interconnects. Typically the characteristic impedance is designed for 50 ohms and best if controlled within ± 5%. Controlled impedance design requires controlled values for the ratios of conductor dimensions to the dielectric thickness. The 64 QFP package used for the MCA750ETL array has signal line impedances of 50 Ω ± 2 Ω while the 160 QFP for the MCA3200ETL array is 50 Ω ± 4 Ω.

2.1.3 Signal Termination

Signal reflections are produced when discontinuities such as impedance mismatches are encountered. One discontinuity is the stub capacitance produced by the package, bonding pad and input circuit.

The stub capacitance is reduced by eliminating the package lead capacitance. This can be accomplished by making the package lead part of the transmission line by designing the package lead with a characteristic impedance of 50 ohms. An equation from the MECL System Design Handbook[4] can be used to calculate the reflected waveform due to the stub capacitance, C_t. The equation was normalized with substitution of E_1 = 1.0 volt and 1.2 T_r was substituted for T_1 (0 to 100% rise time).

$$E_{ref} = \frac{Z_o C_t}{2.4 T_r}\left(1 - e^{-2.4\frac{T_r}{Z_o C_t}}\right) \qquad (2.1)$$

For a T_r = 400 ps, the reflected voltage is approximately 5.2% for a 1.0 pF stub capacitance. When using the one pin method, a pin capacitance of 3.5 pF produces an 18% reflection.

An equation can be derived for the maximum frequency in order to maintain sufficient noise margin for the receiver. The derivation assumes that the transmission line is terminated at the end of the line with a resistance value equal to the characteristic impedance of the transmission line. A stub capacitance is assumed parallel to the termination resistor. The parallel combination of the load resistor, R_L, and the stub capacitance, C_t, results in the equivalent load impedance, Z_L:

$$Z_L = \frac{R_L\left(\frac{1}{j\omega C_t}\right)}{R_L + \left(\frac{1}{j\omega C_t}\right)} = \frac{R_L}{j\omega R C_t + 1} \qquad (2.2)$$

the reflection coefficient at the load is:

$$P_L = \frac{Z_L - Z_O}{Z_L + Z_O} = \frac{\left(R_L - Z_O\right) - j\omega R Z_O C_t}{\left(R_L + Z_O\right) + j\omega R Z_O C_t} \qquad (2.3)$$

letting $R_L = Z_O$ and $M = \omega Z_O C_t = 2\pi f Z_O C_t$

$$P_L = \frac{-jM}{(2 + jM)}\frac{(2 - jM)}{(2 - jM)} = \frac{-M(M + 2j)}{4 + M^2}$$

solving for the magnitude of P_L

$$|P_L| = \frac{M}{4 + M^2}\sqrt{M^2 + 4} = \frac{M}{\sqrt{M^2 + 4}} \qquad (2.4)$$

solving for M by squaring both sides of the equation

$$P_L^2 = \frac{M^2}{M^2+4} \quad \text{then} \quad M = \frac{2|P_L|}{\sqrt{1-P_L^2}} = \frac{2}{\sqrt{\frac{1}{P_L^2}-1}}$$

substituting $2\pi f Z_O C_t = M$ and solving for f

$$f_{MAX} = \frac{1}{\pi Z_O C_t \sqrt{\frac{1}{P_L^2}-1}} \qquad (2.5)$$

From equation 2.4, P_L can be solved.

$$|P_L| = \frac{1}{\sqrt{1+\frac{1}{\left(\pi f C_t Z_O\right)^2}}} \qquad (2.6)$$

Equation 2.5 has proven useful for predicting the maximum input frequency for various package types and input configurations. Equation 2.6 has proven useful in predicting the attenuation of the signal at various input and output frequencies for various stub capacitances. The attenuation factor

$\left(\frac{V_{out}}{V_{in}}\right)$ is equivalent to $1-|P_L|$.

Package testing in the lab has verified that these equations correlate closely to the lab data results.

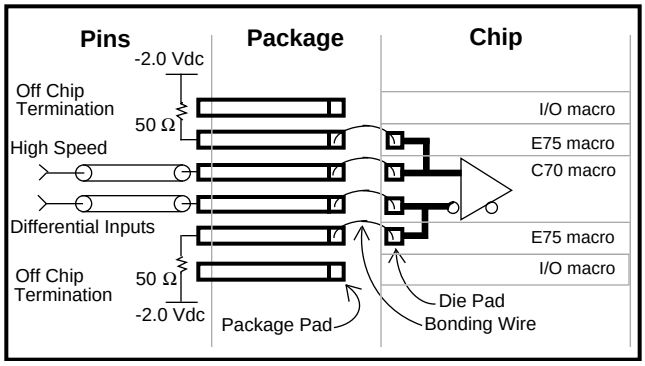


Figure 2-1 ECL Input with Two Pin Input Signal Termination

For high speed input signals, line termination closer to the die pad than conventional pin termination may be desired. The most readily available technique for improving line termination is through using two pins, one for the input signal, and the other for termination as illustrated in Figure 2-1. Through the use of the E75 macro (die pad to die pad metal strap), almost any two adjacent die pads on the MCA3 ETL arrays can be used to configure this termination. For a worst case scenario it can be calculated that the stub capacitance can be reduced by the input package capacitance minus the pin and pad capacitance. Figure 2-2 depicts the one and two pin termination models and shows the calculation for the stub capacitance of the four MCA3 ETL array packages.

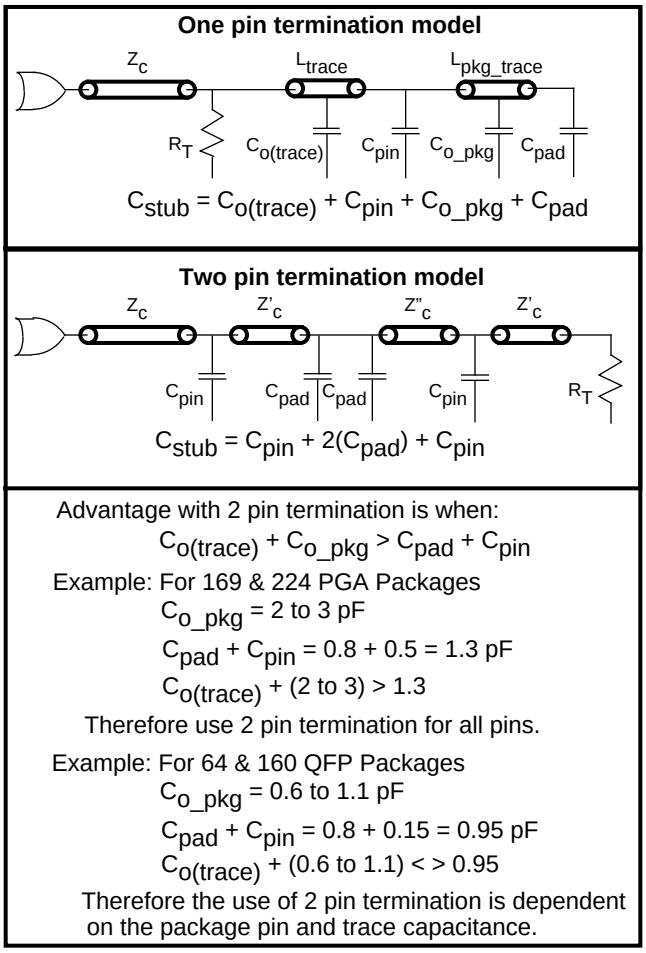


Figure 2-2 One and Two Pin Input Termination Models and Calculation

It can be realized that the stub capacitance for typical PGA packages with over 150 pins may be reduced by 0.5 to 2.0 pF. However, for the smaller QFP packages, the stub capacitance may increase by 0.35 pF or have only a small reduction. Therefore, this technique is only recommended for packages where the capacitance due to the package is about 1.5 or more times larger than the combined pad and pin capacitance.

A superior approach to the above technique is to employ the patented Low Reflection Input Configuration (LRIC)[5] method as shown in Figure 2-3. Once again two pins are used however this method joins the pins at the package pad rather than the die pad. Since the additional die pad capacitance is not present as in the above method, this technique further reduces the stub capacitance but at the cost of requiring special signal leads within the package.

Additional approaches for input signal termination include: (1) on-chip resistors and (2) termination resistors internal to the package. On-chip termination requires that the termination resistor be located on the die near the input signal die pad. In order to allow maximum flexibility in pin selection while using a gate array architecture, a termination resistor must be

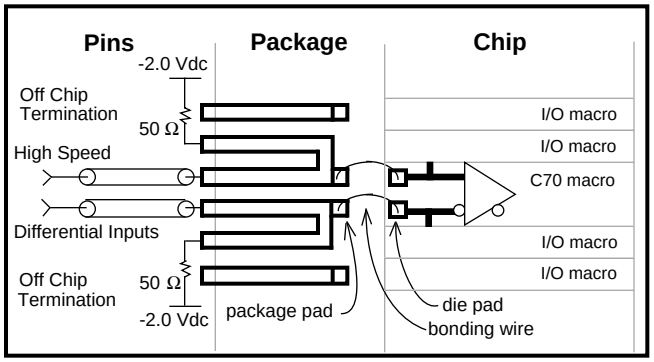


Figure 2-3 LRIC Structure

fabricated for each possible input pin.This can require a substantial amount of silicon since the resistor value is typically 50 ohms and every signal pad on the chip would require a resistor. A more restrictive approach may be to fabricate resistors only for selected pins. For either case, there is still the need to connect the resistor to V_{TT} (since -2.0 Vdc is generally not available on-chip) or use two resistors requiring substantially more power to provide the thevenin equivalent of 50 ohms to -2.0 Vdc. Two possible approaches for connecting the resistors to V_{TT} are the use of a pin for each termination resistor used or connecting several termination resistors together and bringing the net to one pin. The first method could easily be used in a gate array since a termination macro could be placed in the I/O cell adjacent to the terminated input signal. The termination macro would connect the termination resistor to the package pin for connection to V_{TT}.

The second approach, use of termination resistors in the package, will require less pins for termination as the number of terminated inputs increases on the chip. However, when the number of terminated inputs is few, more pins may be used since dedicated pins to V_{TT} are required. The dedicated pins are required since wide metal is needed to make the connection to all termination resistors due to the high current during switching. It should be realized that this second method will result in a higher inductance on the V_{TT} path since several pins and wide metal are used.

2.1.4 Considerations for Termination Resistors and Bypass Capacitors

ECL outputs need to be terminated with resistors at the end of the transmission line. The value of the resistor should match the characteristic impedance of the transmission line for lines that are longer than 0.8 inches or rise times of less than 300 ps (20-80%). MCA3 has the capability (except the MCA3 MCA2200ECL array) of having STECL (series terminated ECL) outputs and current source inputs. Parallel terminated resistors are needed for fanouts greater than one that must be distributed on the line. If a series terminated line is used, a delay penalty (equal to the delay of the loaded line) must be added to the signal.

Capacitors are required that are sensitive at both high and low frequencies. Therefore, two types of capacitors need to be used. Decoupling capacitors (low frequency) are placed close to the package on the mounting side of the PC board. Also, filter capacitors (high frequency, high Q, low dissipation factor) are needed. Up to seven power planes are required on the PC board in order to supply power to ECL, and TTL devices. The ECL and TTL planes must be separate in order to have acceptable noise. The power planes are V_{CCO} (ECL output ground), V_{CCE} (ECL logic ground), V_{EEE} (ECL -5.2 volt supply), V_{TT} (ECL -2.0 volt termination supply), V_{EE2} (ECL -3.4 volt supply for MCA10000ECL only), V_{CCT} (+5.0 volt TTL supply), and V_{EET} (TTL ground). The V_{CCO} and the V_{CCE} could possibly be combined into one power plane (5 total) when the design requires ETL (mixed ECL and TTL). Capacitors need to be connected between V_{CCO} and V_{TT}, V_{CCE} and V_{EEE}, V_{CCT} and V_{EET}, and V_{CCE} and V_{EE2}.

Two main transient time considerations must be given to the termination voltage supply, the instant local transient voltage time in the 0.5 to 10 ns region, and the longer term response of 10 ns to 10 ms. The current supplied by the capacitors must last up to 10 ms which is established by the recovery time of the power supply.

The equations used to calculate the amount of capacitance are as follows:

$$i = C\left(\frac{dV}{dT}\right) \tag{2.7}$$

$$i = N\left(\frac{V}{Z_O}\right) \tag{2.8}$$

solving for C in equation 2.7 and 2.8 results in

$$C = N\left(\frac{V}{Z_O}\right)\left(\frac{dT}{dV}\right) \tag{2.9}$$

where:
C = capacitance required
dT = time interval that the capacitor must supply the current
dV = maximum amount of noise (usually 50 mV)
i = total simultaneous transient current
N = number of outputs switching simultaneously
V = voltage swing of the signal (800 mV for ECL)
Z_O = characteristic impedance of the line

2.2 I/O MACROS AND VOLTAGE LEVELS

For operating at frequencies over 650 MHz or 1.0 Gb/s, differential I/O macros with higher than standard switch currents are recommended (see Table 3-1). For MCA3 ETL arrays, the switch currents of H macros (0.53 mA) and HI DRIVE macros (1.1 mA) are sufficient. The widths of all input signal pulses (40% to 60% duty cycle) should satisfy the criterion given in section 4.4 after pulse width shrinkage has been taken into account.

2.2.1 High Frequency Input

At frequencies above 650 MHz, the selection of input macros is determined by the attenuation caused by package capacitance, characteristic impedance and die pad capacitance losses that will reduce the signal amplitude at the macro input. These effects are a function of the specific input macro used, die size, package type, and location of the package pin. Figure 2-4 and Figure 2-5 show the required signal amplitude at a given frequency for single-stage and two-stage buffer in-

put for the four package types offered on MCA3 ETL arrays. A single-stage input refers to the use of an input macro driving an internal macro clock input. A two-stage input refers to the use of an input macro immediately driving a differential buffer or non-select input of a differential multiplexer macro.

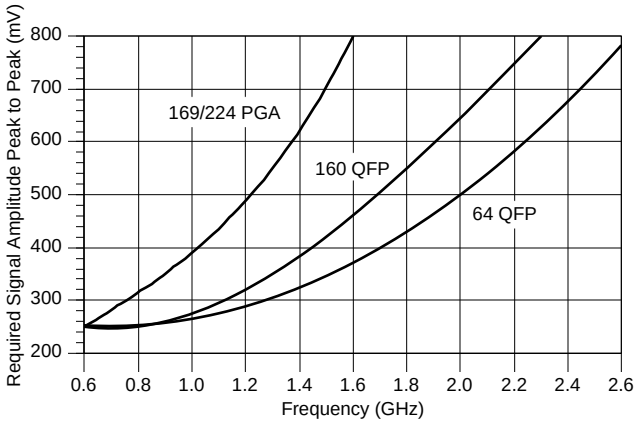


Figure 2-4 Minimum Differential Input Amplitude for Single-Stage Input Macro

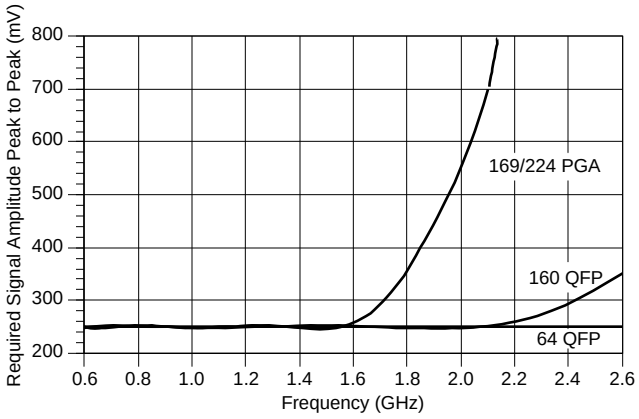


Figure 2-5 Minimum Differential Input Amplitude for Two-Stage Input Macro

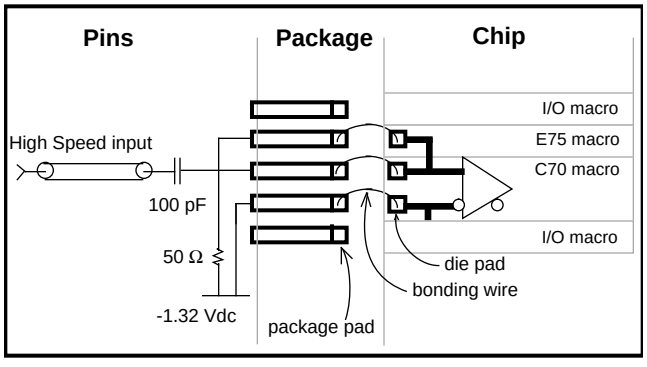


Figure 2-6 AC Coupled Single-ended Input With Off-Chip Termination

AC coupled single-ended input signals should be biased to V_{BB} (see Figure 2-6) and have amplitudes of twice the minimum differential amplitude plus 40 mV. Non-biased single-ended input signals should swing around V_{BB} (-1.32 Vdc) and have amplitudes of twice the minimum differential amplitude plus 120 mV.

2.2.2 High Frequency Output

Two common types of outputs used on ECL arrays are the emitter follower and open collector outputs. The emitter follower is by far the most popular, however, for high speed clock and data signals, pulse edges may be degraded[6]. Open collector outputs are used to improve the steepness and shape of pulses at the cost of reduced drive capability and non-ECL load compatibility[7]. The improvement is due to the removal of the emitter follower collector-base capacitance and their transformed 50 Ω loads. Additional advantages of open collector outputs are that line driving is simplified and noise on power supply lines is reduced. For either output type, achieving the optimal output signal requires matching at the end of the driven transmission line to avoid reflections. On-chip terminating resistors integrated on the receiving chip usually provide the best matching.

Attenuation of the output signal, due to circuit and package limitations, can reduce a typical ECL output (595 mV minimum swing) to 50 - 200 mV at frequencies above 1 GHz. Increased switch current in the output circuit can provide a minimally attenuated signal at the circuit output for frequencies above 3 GHz. However, package effects may cause substantial attenuation. Although not normally practical, for clock signals the physical line length of the driven transmission line can be adjusted to allow reflections to increase the output amplitude.

The package lead and pin attenuation can be calculated for a given package using the following derivations. The reflection due to the pin capacitance at the package interface to the PC board is calculated from equation 2.6. The package attenuation due to the mismatch in the package lead impedance compared to the characteristic impedance of the transmission line will be derived (all equation variables are given after equation 2.12):

The maximum reflection occurs when:

$$T_1 = 2T_P \tag{2.7}$$

the delay of the package lead is:

$$T_P = 0.085\left(L_P\right)\sqrt{e_r} \tag{2.8}$$

For frequencies above 0.8 GHz, the frequency can be approximated by:

$$f = \frac{1}{2T_1} \tag{2.9}$$

substituting equation 2.8 and 2.9 into equation 2.7

$$\frac{1}{2f} = 2\,(0.085)\,L_P\sqrt{e_r}$$

Solving for f_{max} where maximum reflection occurs,

$$f_{max} = \frac{1}{(0.34)\, L_P \sqrt{e_r}} \text{ in GHz} \qquad (2.10)$$

Knowing the reflection coefficient at the package pin, P_A, the attenuation can be calculated,

for $f > f_{max}$

$$K_{att\_pkg_{max}} = 1 - |P_A| \qquad (2.11)$$

From 0.8 GHz to fmax, the maximum reflection decreases linearly,

$$K_{att\_pkg} = 1 - \frac{f}{f_{max}} \left| \frac{Z_L - Z_P}{Z_L + Z_P} \right| \qquad (2.12)$$

where:

e_r = relative dielectric constant

L_P = package lead length in inches

T_P = delay of package lead in ns

T_1 = rise time of the driving signal in ns (0 to 100%)

Z_P = characteristic impedance of the package lead

Z_L = characteristic impedance of the driven transmission line, terminated with its characteristic impedance

For instance, the 64 QFP has a package line length of about 0.24 inches and a dielectric constant of 4.

Therefore,

$$f_{max} = \frac{1}{(0.34)\ (0.24\text{in})\ (2)} = 6.127\text{GHz}$$

If a package was used that didn't have a controlled impedance such that Z_P = 100 ohms then K_{att_pkg} at 2.5 GHz would be:

$$K_{att\_pkg} = 1 - \frac{2.5}{6.127} \left| \frac{50 - 100}{50 + 100} \right| = 0.863$$

Note that the actual $Z_P = 50\ \Omega \pm 2\ \Omega$ for the 64 QFP.

The attenuation due to the pin capacitance can be calculated from equation 2.6. The pin capacitance for the lead (0.16 in.) is about 0.15 pF. For a frequency of 2.5 GHz

$$P_{pin} = \frac{1}{\sqrt{1 + \frac{1}{(\pi\,(2.5\text{GHz})\ (0.15\text{pf})\ (50\text{ohms}))^2}}} = 0.059$$

$$K_{att\_pkg} = 1 - P_{pin} = 0.941$$

$K_{att\_ckt} = 0.403$ for the HE70[1] macro at 2.5 GHz

$$K_{att\_total} = K_{att\_ckt} K_{att\_pkg} K_{att\_pin}$$

$$= (0.403)\ (0.863)\ (0.941) = 0.327$$

The typical output swing would be (850 mV) (0.327) = 278 mV.

A 10 mA internal current switch with differential ECL outputs (macro HE70) has been designed and characterized for the MCA3 ETL arrays. The circuit has emitter follower inputs to reduce the input capacitance. Figure 2-7 contains a plot of the measured output swing versus frequency for the HE70 macro at V_{CC} = -5.2 Volts and a junction temperature of 75°C. The chip was packaged in the 64 QFP package with the output pin soldered to a 50 Ω transmission line terminated with a 50 Ω resistor. It can be seen that at 2.6 GHz the amplitude was approximately 330 mV.

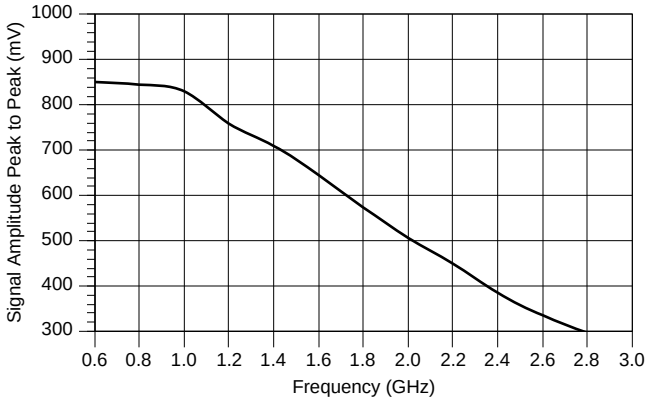


Figure 2-7 10 mA (HE70) ECL Output Amplitude (measured)

Both 12 mA and 25 mA open collector output macros have been designed for the MCA3 ETL arrays. The current value was selected to provide approximately 600 mV swings for 50 Ω and 25 Ω transmission line environments respectively (see Figure 2-8).

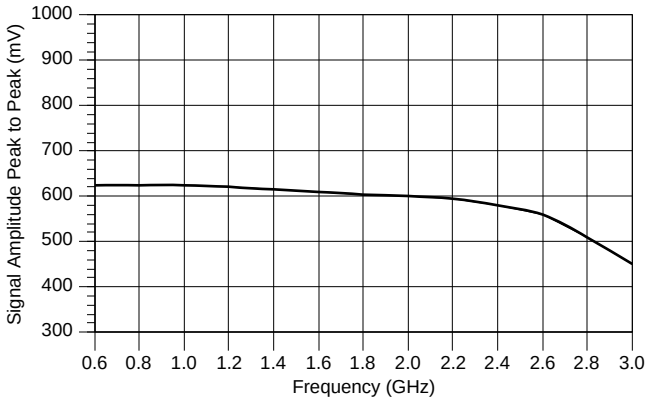


Figure 2-8 25 mA (HE72) Open Collector Output Amplitude with 25 Ohm Load (simulated typical)

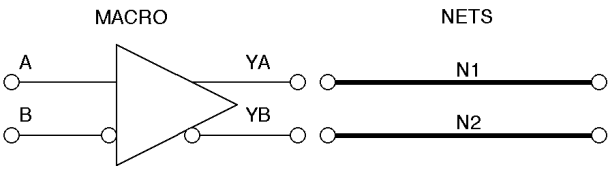
3. INTERNAL MACRO OPERATION

High speed operation of internal circuitry in an ECL gate array requires careful logic design with the selection of macro functions, fixed placement, and sometimes manual routing intervention. The widths of all signal pulses (40% to 60% duty cycle) should satisfy the criterion for that macro and fanout delay as discussed in section 4.4. Differential macros are recommended for high speed signals wherever possible. For connections with low fanout and metal lengths, open collector, or current mode logic (CML) could be employed for ob-

taining shorter delay paths.

3.1 DIFFERENTIAL SIGNAL PATHS

The differential macro and net delays are calculated as shown in Figure 3-1.



Single-ended Macro Delays (ps)			
IN	OUT	(+)	(-)
A,B	YA	100	125
A,B	YB	100	150

Single-ended Net Delays (ps)		
NET	(+)	(-)
N1	75	125
N2	25	25

Differential macro and net delay equations:

$$T_{pd+(YA/YB)} = \frac{2\,[\,T_{pd+(YA)}]\,[\,T_{pd-(YB)}]}{[\,T_{pd+(YA)}] + [\,T_{pd-(YB)}]}$$

$$T_{pd-(YA/YB)} = \frac{2\,[\,T_{pd-(YA)}]\,[\,T_{pd+(YB)}]}{[\,T_{pd-(YA)}] + [\,T_{pd+(YB)}]}$$

Macro delay calculation:

$$T_{pd+(YA/YB)} = \frac{2\,[\,100]\,[\,150]}{[\,100] + [\,150]} = 120\ ps$$

$$T_{pd-(YA/YB)} = \frac{2\,[\,125]\,[\,100]}{[\,125] + [\,100]} = 111\ ps$$

Net delay calculation:

$$T_{pd+(YA/YB)} = \frac{2\,[\,75]\,[\,25]}{[\,75] + [\,25]} = 38\ ps$$

$$T_{pd-(YA/YB)} = \frac{2\,[\,25]\,[\,125]}{[\,25] + [\,125]} = 42\ ps$$

Figure 3-1 Differential Macro And Net Delay Calculation Example

As can be seen, the delay is reduced when using differential macros and nets. Another advantage of differential connections is that the pulse width shrinkage is minimized when using differential signal pairs compared with single-ended signals. Refer to section 4.3 Pulse Width Shrinkage.

Lastly, on-chip propagation delay skew for differential connections is approximately 12% less than for single-ended connections. The on-chip propagation delay skew is defined as the largest delay difference that exists between similar signal path elements (i.e, macros or metal) located in different places on the die. Refer to section 4.1. for a discussion regarding worst case on-chip skew considerations.

3.2 MACRO SELECTION

Most ECL gate arrays provide power programmability of internal macros. This provides a means for adjusting the switch current and output emitter follower of a macro to achieve the delay or frequency desired. One can spend many hours “hand tweaking” a design to set all the current levels to achieve the lowest power while still meeting the performance goal. This is where a logic synthesis tool could be of great assistance. The selection of the switch and output follower current could be made by the tool during both pre- and post-layout. For most ECL gate arrays, the adjusting of currents is not made through using routed metal and therefore changes made after routing would not effect the design.

3.2.1 Macro Switch Currents

To provide an example of macro current level selection, the MCA3 ETL array macro current levels are now discussed. Two current levels are available on most MCA3 ETL array macros. A third “HIGH DRIVE” current level is available on select macros to provide the highest operating frequencies. Table 3-1 shows the recommended maximum frequency, propagation delay, switch current, and output follower current for the three power levels of the MCA3 ETL macros.

Table 3-1 MCA3 ETL Array Macro Speed Power Programmability

Low Power (L) Macro	High Power (H) Macro	HIGH DRIVE (L) Macro
0.27 mA switch current	0.53 mA switch current	1.1 mA switch current
0.48 or 0.96 mA emitter follower current	0.48 or 0.96 mA emitter follower current	0.96 or 1.92 mA emitter follower current
300 ps worst case delay	200 ps worst case delay	125 ps worst case delay
< 800 MHz	< 1660 MHz	< 2500 MHz

The frequency shown for each macro power level is not a fixed rule. It is based on the worst case operating frequency of typical differential flip-flops for that power level. Depending on the macro type and load being driven, the maximum frequency may be substantially less than the values given in Table 3-1. As stated in section 4.4, the macro and metal fanout minimum pulse widths should not be violated.

Worst case flip-flop delays and specifications are shown in Table 3-2 for all power levels. Several D type flip-flops are available at both the high power and high drive levels. Such functions as an EXNOR gated data input have been designed into a flip-flop to virtually eliminate the delay of using a separate EXNOR macro without compromising the flip-flop specifications for that power level (see Figure 3-4).

Table 3-2 Differential Hi Speed Flip-Flop Specification For L, H and HIGH DRIVE Macros

	Low Power (L) Macro	High Power (H) Macro	HIGH DRIVE (L) Macro
Max. Freq. (MHz)	<800	<1660	<2500
Power (mW)	9.3	16.0	32.0
Data setup (ps)	450	200	100
Clock delay (ps)	500	300	200

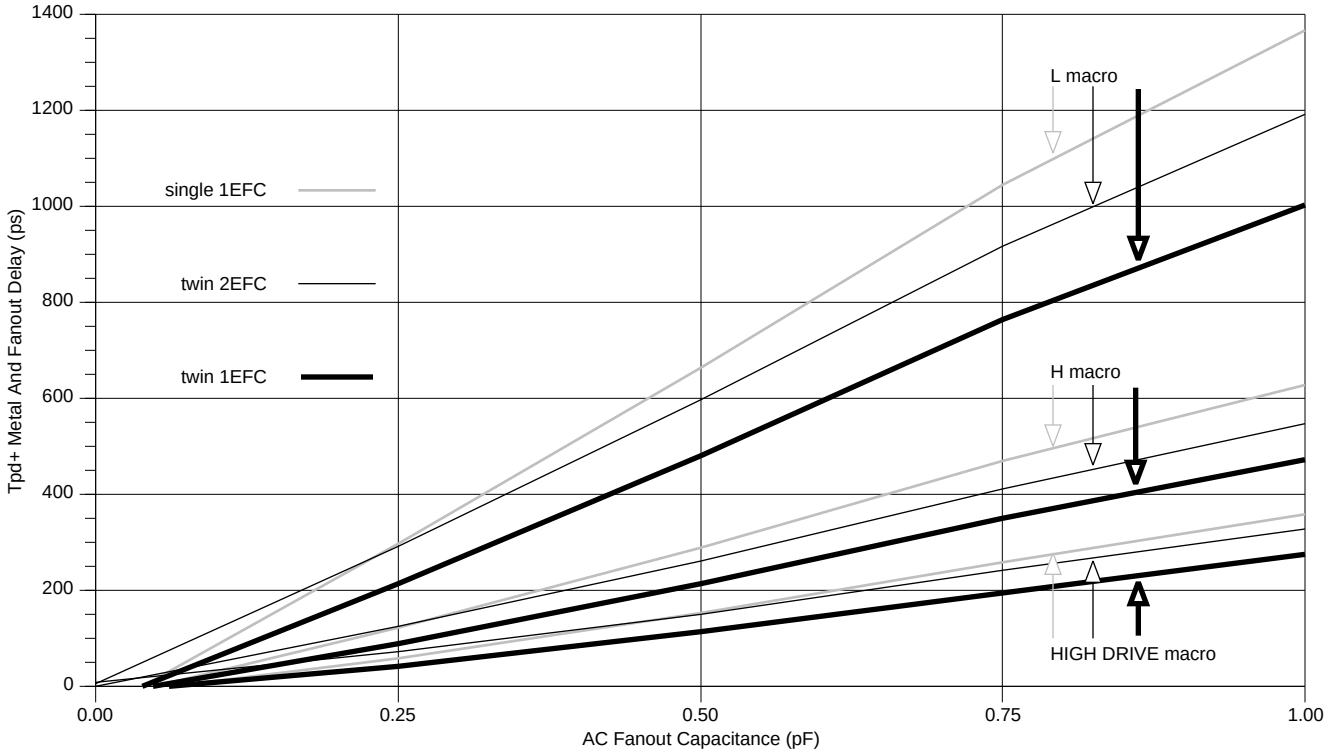


Figure 3-2 Internal Macro Worst Case Rising Edge Delay versus Metal and Fanout Capacitance (20 mils of metal are included for each 0.1 pF at 115°)

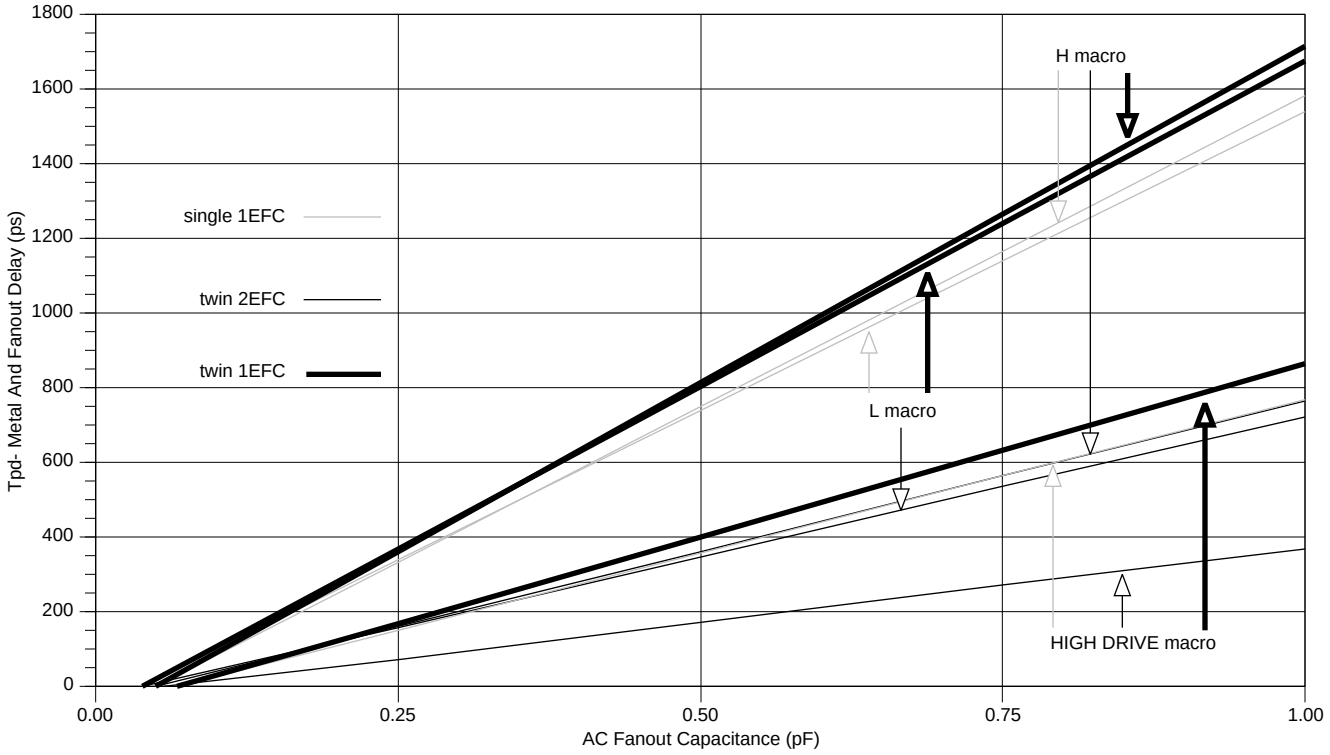


Figure 3-3 Internal Macro Worst Case Falling Edge Delay versus Metal and Fanout Capacitance (20 mils of metal are included for each 0.1 pF at 25°C)

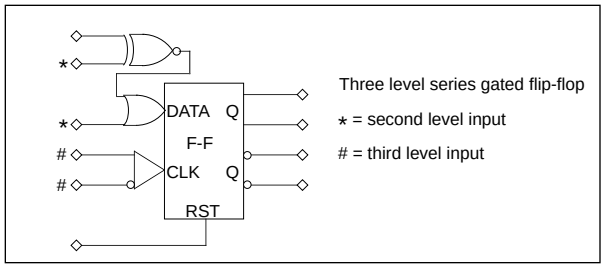


Figure 3-4 D Flip-Flop with EXNOR Gated Data Input (macro H712)

3.2.2 Emitter Follower Current Selection

Selection of emitter follower current (EFC) levels is not as straight forward as choosing the macro switch current level. As seen in Table 3-1, each macro power level has two levels of EFC. The higher value is obtained by tying together, or "twinning", the outputs of the double emitter output device and doubling the EFC of the device. "Twinning" outputs while maintaining one EFC is used for special cases where only the rising edge delay is a concern. To assist in making the correct EFC selection, the graphs in Figure 3-2 and Figure 3-3 show the metal (20 mils for each 0.1 pF) and fanout delay which must be added to the delay of a macro as a function of the AC fanout being driven by the macro output. Each graph contains nine curves, one for each macro switch current and EFC selection. The x-axis ranges from 0 to 1.0 pF of fanout capacitance. Table 3-3 contains the input capacitance for each macro type and input type for a particular macro. Upper level inputs are connections made to the base of the transistor in the top level differential pair of the ECL circuit. A lower level input is a connection to the base of an emitter follower input transistor connected to a second or third level differential pair of the ECL circuit. Twenty mils of metal can be assumed for each 0.1 pF of fanout capacitance. Since the metal length can vary for each net, this number provides an estimated length of metal per fanout capacitance of nets intended for higher frequency operation. A conservative metal length estimate is 30 mils per connection.

Table 3-3 Typical Macro Input Capacitance (pF)

Internal Macro type	Input Type	
	Lower	Upper
Low Power (L) Macro	0.05	0.07
High Power (H) Macro	0.05	0.09
HIGH DRIVE (L) Macro	0.05	0.12

The following list contains guidelines for the selection of twin outputs and EFC's. These are approximate output characteristics when compared to a single output with one EFC.

1. A decrease (20-25%) of the rising edge delay occurs on twin outputs with one EFC.
2. A small increase (8-12%) of the falling edge delay occurs on twin outputs with one EFC.
3. A small decrease (5-12%) of the rising edge delay occurs on twin outputs with two EFC's.
4. A decrease (50-55%) of the falling edge delay occurs on twin outputs with two EFC's.
5. For signals over 800 MHz, a minimum of 0.96 mA of EFC is recommended.
6. An EFC of 0.96 mA may be used for up to 2.5 GHz operation if the minimum pulse width rule insection 4.4 is satisfied.

4. GENERAL AC PERFORMANCE CONSIDERATIONS AND GUIDELINES

This section provides guidelines and application information to predict the internal AC performance for high frequency ECL gate array design. This information has been compiled through simulation, empirical evaluation, and experience with the usage of ECL gate arrays. These guidelines are not, however, specification limits.

4.1 DELAY SKEW CONSIDERATIONS

The on-chip delay skew is defined as the largest delay difference which can exist between similar signal paths located on the chip. This delay skew depends on the type and relative position of the elements (i.e. macro or metal) making up the delay path.

In order to guarantee that the worst-case skew conditions are analyzed, the skew must be calculated between the two paths in question for four cases:

1. Slow macros and slow metal (SS). All delays are running at the specified maximum.
2. Fast macros and fast metal (FF). All delays are running at the minimum values.
3. Fast macros and slow metal (FS). Macro delays are running at minimum delays and metal is running at maximum delays.
4. Slow macros and fast metal (SF). Macro delays are running at maximum delays and metal is running at minimum delays.

In order to calculate the skew, the manufacturer should provide a skew factor that when multiplied by the maximum delay the skewed delay is calculated.

For the MCA3 ETL array, skew factors are designated as K factors. Macro K factors vary depending on the macro type. These include whether or not the macro output is collector dotted, if the macro is a differential receiver driven differentially, and among other things, if the macro is an internal or I/O circuit. In general, the K factor is between 0.7 and 0.9. Metal and fan-out K factors also vary depending on characteristics such as if the net is driven differentially or if signals are switching in opposite directions. These K factors range from 0.6 to 0.8. Specific K factors for a given macro and or metal path can be found in the MCA3 ETL Series Design Manual section 5.3.3.

An example of a skew delay calculation follows:
Assume that two similar macros (M1 & M2) with delay skew K factors equal to 0.8 are placed on opposite sides of a gate array. Further more, assume that the propagation delay time of a rising edge from input A to output YA for macro M1 is at the specified maximum, 250 ps. The fastest that the same path (A to YA) can be on macro (M2), is 250(0.8) = 200 ps.

Similarly, the greatest delay difference which can exist between signals switching in the same direction traveling along two equivalent metal paths (equal in length and fanout) with a delay skew factor of 0.7 is $t_{d2} = t_{d1}(0.7)$ where t_{d1} is the larger of the two delays in question and t_{d2} is the smallest value that the other delay can have.

4.2 SETUP AND HOLD TIME CALCULATIONS

The minimum setup time is the amount of time the data must be present at the data input before the latching edge of the clock occurs at the clock input in order to insure that the data is latched properly. The minimum hold time is the amount of time the data must remain unchanged at the data input after the latching edge of the clock at the clock input in order to insure that the data is latched properly. A negative hold time means that the data may be changed before the clocking edge and still be latched properly. The hold time is zero unless otherwise specified.

Setup and hold times for flip-flops and latches are defined by the following equations:

Setup Time - General Equation

$$T_S = T_{MS} + T_{DMAX} - T_{CMIN} \quad (4.1)$$

Hold Time - General Equation

$$T_H = T_{MH} + T_{CMAX} - T_{DMIN} \quad (4.2)$$

where:

T_S = setup time at the input
T_H = hold time at the input
T_{CMAX} = maximum clock path time
T_{CMIN} = minimum clock path time
T_{DMAX} = maximum data path time
T_{DMIN} = minimum data path time
T_{MS} = specified macro setup time
T_{MH} = specified macro hold time

Setup and hold times for flip-flops and latches as seen from the input pins will vary from the times given for the specified macro setup and hold time due to differences in the delay paths leading to the macro. The method used by Motorola on ECL gate arrays determines the actual setup and hold times as seen from the input pins, these times are found by derating the times listed for the macro by the difference between the maximum and minimum delay in the clock and data paths leading to the macro. To calculate the effective setup and hold time at the input pins, the designer must look at the four possible combinations of slow and/or fast effects (see section 4.1).

The factors determining which combination to use depends on the following values and their relationships with each other.

T_{CMAC_MAX} = maximum delay due to the macros in the clock path
T_{DMAC_MAX} = maximum delay due to the macros in the data path
T_{CMFO_MAX} = maximum delay due to the metal and fanout in the clock path
T_{DMFO_MAX} = maximum delay due to the metal and fanout in the data path

In order to determine the minimum setup and hold times, taking into account the minimum propagation delay and the on-chip propagation delay skew, one should use the following set of equations to first determine the case that yields the correct equation for the minimum setup (T_{SMIN}) and minimum hold (T_{HMIN}) times.

Equations to Determine Minimum Setup Time

For the (SS) case, if the following conditions exist ⇒

$$T_{CMFO\_MAX} \le \left(\frac{1}{K_{METAL\_SKEW}}\right)\left(T_{DMFO\_MAX}\right) \text{ and}$$

$$T_{CMAC\_MAX} \le \left(\frac{1}{K_{MACRO\_SKEW}}\right)\left(T_{DMAC\_MAX}\right) \text{ then:}$$

$$T_{SMIN} = T_{MS} + T_{DMAX} - K_{METAL\_SKEW}\left(T_{CMFO\_MAX}\right) - K_{MACRO\_SKEW}\left(T_{CMAC\_MAX}\right) \quad (4.3)$$

For the (FF) case, if the following conditions exist ⇒

$$T_{CMFO\_MAX} > \left(\frac{1}{K_{METAL\_SKEW}}\right)\left(T_{DMFO\_MAX}\right) \text{ and}$$

$$T_{CMAC\_MAX} > \left(\frac{1}{K_{MACRO\_SKEW}}\right)\left(T_{DMAC\_MAX}\right) \text{ then:}$$

$$T_{SMIN} = T_{MS} + \left(\frac{K_{METAL\_MIN}}{K_{METAL\_SKEW}}\right)\left(T_{DMFO\_MAX}\right) + \left(\frac{K_{MACRO\_MIN}}{K_{MACRO\_SKEW}}\right)\left(T_{DMAC\_MAX}\right) - K_{METAL\_MIN}\left(T_{CMFO\_MAX}\right) - K_{MACRO\_MIN}\left(T_{CMAC\_MAX}\right) \quad (4.4)$$

For the (SF) case, if the following conditions exist ⇒

$$T_{CMFO\_MAX} > \left(\frac{1}{K_{METAL\_SKEW}}\right)\left(T_{DMFO\_MAX}\right) \text{ and}$$

$$T_{CMAC\_MAX} \le \left(\frac{1}{K_{MACRO\_SKEW}}\right)\left(T_{DMAC\_MAX}\right) \text{ then:}$$

$$T_{SMIN} = T_{MS} + \left(\frac{K_{METAL\_MIN}}{K_{METAL\_SKEW}}\right)\left(T_{DMFO\_MAX}\right) - K_{METAL\_MIN}\left(T_{CMFO\_MAX}\right) + T_{DMAC\_MAX} - K_{MACRO\_SKEW}\left(T_{CMAC\_MAX}\right) \quad (4.5)$$

For the (FS) case, if the following conditions exist ⇒

$$T_{CMFO\_MAX} \le \left(\frac{1}{K_{METAL\_SKEW}}\right)\left(T_{DMFO\_MAX}\right) \text{ and}$$

$$T_{CMAC\_MAX} > \left(\frac{1}{K_{MACRO\_SKEW}}\right)\left(T_{DMAC\_MAX}\right) \text{ then:}$$

$$T_{SMIN} = T_{MS} + T_{DMFO\_MAX} - K_{METAL\_SKEW}\left(T_{CMFO\_MAX}\right) + \left(\frac{K_{MACRO\_MIN}}{K_{MACRO\_SKEW}}\right)\left(T_{DMAC\_MAX}\right) - K_{MACRO\_MIN}\left(T_{CMAC\_MAX}\right) \quad (4.6)$$

Equations to Determine Minimum Hold Time

For the (SS) case, if the following conditions exist ⇒

$$T_{DMFO\_MAX} < \left(\frac{1}{K_{METAL\_SKEW}}\right)\left(T_{CMFO\_MAX}\right) \text{ and}$$

$$T_{DMAC\_MAX} < \left(\frac{1}{K_{MACRO\_SKEW}}\right)\left(T_{CMAC\_MAX}\right) \text{ then:}$$

$$T_{HMIN} = T_{MH} + T_{CMAX} - K_{METAL\_SKEW}\left(T_{DMFO\_MAX}\right) - K_{MACRO\_SKEW}\left(T_{DMAC\_MAX}\right) \quad (4.7)$$

For the (FF) case, if the following conditions exist ⇒

$$T_{DMFO\_MAX} \geq \left(\frac{1}{K_{METAL\_SKEW}}\right)\left(T_{CMFO\_MAX}\right) \text{ and}$$

$$T_{DMAC\_MAX} \geq \left(\frac{1}{K_{MACRO\_SKEW}}\right)\left(T_{CMAC\_MAX}\right) \text{ then:}$$

$$T_{HMIN} = T_{MH} + \left(\frac{K_{METAL\_MIN}}{K_{METAL\_SKEW}}\right)\left(T_{CMFO\_MAX}\right) + \left(\frac{K_{MACRO\_MIN}}{K_{MACRO\_SKEW}}\right)\left(T_{CMAC\_MAX}\right) - K_{METAL\_MIN}\left(T_{DMFO\_MAX}\right) - K_{MACRO\_MIN}\left(T_{DMAC\_MAX}\right) \quad (4.8)$$

For the (SF) case, if the following conditions exist ⇒

$$T_{DMFO\_MAX} \geq \left(\frac{1}{K_{METAL\_SKEW}}\right)\left(T_{CMFO\_MAX}\right) \text{ and}$$

$$T_{DMAC\_MAX} < \left(\frac{1}{K_{MACRO\_SKEW}}\right)\left(T_{CMAC\_MAX}\right) \text{ then:}$$

$$T_{HMIN} = T_{MH} + \left(\frac{K_{METAL\_MIN}}{K_{METAL\_SKEW}}\right)\left(T_{CMFO\_MAX}\right) - K_{METAL\_MIN}\left(T_{DMFO\_MAX}\right) + T_{CMAC\_MAX} - K_{MACRO\_SKEW}\left(T_{DMAC\_MAX}\right) \quad (4.9)$$

For the (FS) case, if the following conditions exist ⇒

$$T_{DMFO\_MAX} < \left(\frac{1}{K_{METAL\_SKEW}}\right)\left(T_{CMFO\_MAX}\right) \text{ and}$$

$$T_{DMAC\_MAX} \geq \left(\frac{1}{K_{MACRO\_SKEW}}\right)\left(T_{CMAC\_MAX}\right) \text{ then:}$$

$$T_{HMIN} = T_{MH} + T_{CMFO\_MAX} - K_{METAL\_SKEW}\left(T_{DMFO\_MAX}\right) + \left(\frac{K_{MACRO\_MIN}}{K_{MACRO\_SKEW}}\right)\left(T_{CMAC\_MAX}\right) - K_{MACRO\_SKEW}\left(T_{DMAC\_MAX}\right) \quad (4.10)$$

where:

K_{MACRO_MIN} = minimum macro delay K factor
K_{MACRO_SKEW} = macro delay skew K factor
K_{METAL_MIN} = minimum metal delay K factor
K_{METAL_SKEW} = metal delay skew K factor
T_{CMAX}, T_{DMAX}, T_{MS}, T_{MH} = previously defined

Worst-Case Setup and Hold Example

The following example shows the calculation of the worst-case hold time at the DATA and CLOCK inputs to a flip-flop or latch. For simplicity, all worst-case gate delays are assumed to be 1 ns. Metal delays are assumed to be 1 ns for the data path, and 4 ns in the clock path.

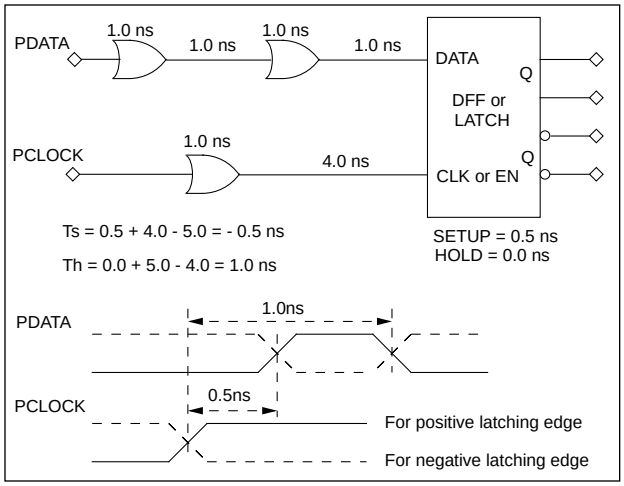


Figure 4-1 Setup and Hold Time Example -NO Skew

Figure 4-1 shows the setup and hold time calculation without taking into account the on chip skew for this example. The setup time at the DFF/LATCH inputs is specified at 0.5 ns. If maximum delays are used, the setup time at the PDATA and PCLK inputs is -0.5 ns. The hold time at the DFF/LATCH inputs is specified at 0.0 ns. If all maximum delays are used, the hold time at the PDATA and PCLK inputs is 1.0 ns.

Skewed Setup and Hold Example

The minimum setup and hold time will now be calculated using the skewed values for the macro and metal delays. First, the case (SS, FF, SF, FS) must be found for the setup and hold time.

For this example, the following values can be assumed:

T_{CMAC_MAX} = 1.0 ns
T_{DMAC_MAX} = 2.0 ns
T_{CMFO_MAX} = 4.0 ns
T_{DMFO_MAX} = 2.0 ns
K_{MACRO_MIN} = 0.4
K_{MACRO_SKEW} = 0.8
K_{METAL_MIN} = 0.4
K_{METAL_SKEW} = 0.6

Case Determination for Setup Time

Using the above equations to determine the case for the minimum setup time would result in case (SF), slow macros and fast metal since;

$$T_{CMFO\_MAX} > \left(\frac{1}{K_{METAL\_SKEW}}\right)\left(T_{DMFO\_MAX}\right)$$

$$4.0\text{ns} > (1.67)\ (2.0\text{ns}) = 3.34\text{ns}$$

and

$$T_{CMAC\_MAX} \leq \left(\frac{1}{K_{MACRO\_SKEW}}\right)\left(T_{DMAC\_MAX}\right)$$

$$1.0ns \leq (1.25)\,2.0ns = 2.5ns$$

Case Determination for Hold Time

Using the above equations to determine the case for minimum hold time would result in case (FS), fast macros and slow metal since;

$$T_{DMFO\_MAX} < \left(\frac{1}{K_{METAL\_SKEW}}\right)\left(T_{CMFO\_MAX}\right)$$

$$2.0ns < (1.67)\,(4.0ns) = 6.68ns$$

and

$$T_{DMAC\_MAX} \geq \left(\frac{1}{K_{MACRO\_SKEW}}\right)\left(T_{CMAC\_MAX}\right)$$

$$2.0ns \geq (1.25)\,(1.0ns) = 1.25ns$$

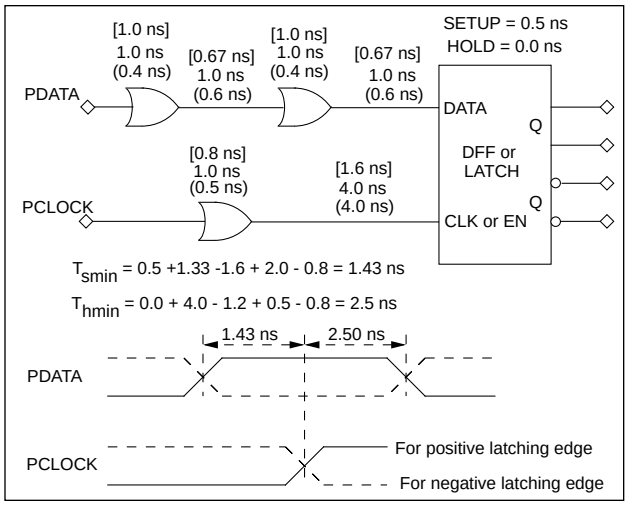


Figure 4-2 Setup and Hold Time Example - With Skew

Figure 4-2 contains the example circuit showing the setup and hold time calculations with skew. Values in square brackets [ ] are the values used in the setup time calculation, while values in parentheses ( ) are values used to determine the new hold time. The equations are listed below:

The minimum setup time (T_{SMIN}) is calculated by using equation 4.5 for the (SF) case.

$$T_{SMIN} = 0.5ns + \left(\frac{0.4}{0.6}\right)(2.0ns) - 0.4\,(4.0ns) + 2.0ns - 0.8\,(1.0ns)$$

$$T_{SMIN} = 1.43ns$$

The minimum hold time (T_{HMIN}) is calculated by using equation 4.10 for the (FS) case.

$$T_{HMIN} = 0.0ns + 4.0ns - 0.6\,(2.0ns) + \left(\frac{0.4}{0.8}\right)(1.0ns) - 0.4\,(2.0ns)$$

$$T_{HMIN} = 2.50ns$$

4.3 PULSE WIDTH SHRINKAGE (PWS)

4.3.1 PWS Due to Rise/Fall Delay Skew

Pulses propagating through an array will shrink due to the delay differences in the rising edge delay versus the falling edge delay, both for the macro delay and the metal and fanout delay. Even if the worst-case rising and falling edge delays are specified the same, pulse width shrinkage can still occur.

The following equations should be used to calculate the rising and falling pulse width shrinkage due to the driving macro and the metal and fanout for both negative and positive pulses:

$$PWS_{(-)} = T_{pd\_max(-)} - 0.8T_{pd\_max(+)} + T_{pd\_metal\_fo(-)} - 0.6T_{pd\_metal\_fo(+)} \quad (4.11)$$

$$PWS_{(+)} = T_{pd\_max(+)} - 0.8T_{pd\_max(-)} + T_{pd\_metal\_fo(+)} - 0.6T_{pd\_metal\_fo(-)} \quad (4.12)$$

where:

$T_{pd\_max(+)}$ = the maximum macro delay, rising
$T_{pd\_max(-)}$ = the maximum macro delay, falling
$T_{pd\_metal\_fo(+)}$ = metal and fanout delay, rising
$T_{pd\_metal\_fo(-)}$ = metal and fanout delay, falling

If an external clock driver is driving the clock input pin, the rise and fall times of the clock driver must be such that the minimum required pulse widths specified in equations 4.11 and 4.12 above are met. The minimum pulse width that the external clock driver can generate as a function of the rise/fall time and the input fanin is:

$$PW_{min}(DRIVER) = 1.7t_r + 0.1\,(FI - 1) \quad (4.13)$$

where:

t_r = the 20 to 80% rise or fall time at the input
FI = the input fanin

Pulse width shrinkage (and stretching) due to skew can be minimized by using pairs of physically adjacent inverting gates with approximately the same fanout and metal lengths.

4.3.2 PWS Due to Narrow Pulses

A short pulse with a small duty cycle (<20%) will tend to shrink as it propagates through an ECL gate because the response time of the circuit may keep the signal from fully reaching the opposite logic state voltage (V_{OH} or V_{OL}). This shrinkage will occur at each gate through which the narrow pulse passes. The designer should note that using a series of inverting gates will not alleviate this type of shrinkage.

The following equation can be used as a guideline to estimate additional pulse width shrinkage due to narrow pulse effects:

for $\frac{W_p}{T_{pd\_max}} < 10$

$$PWS_n = T_{pd\_max}\left(1 - \left(0.028\left(\frac{W_p}{T_{pd\_max}}\right) + 0.694\right)\right) \quad (4.14)$$

where:

T_{pd_max} = the maximum delay, either rising or falling edge, of the gate through which the pulse is propagating.

W_p = width of the pulse

This calculation does not include the metal and fanout delay since it is already accounted.

4.4 MINIMUM PULSE WIDTH SPECIFICATIONS

The widths of all internal pulses should satisfy the following criterion after pulse width shrinkage has been taken into account:

For single-ended signals:

$$PW_{MIN} > 2\,(t_{pd\_max}) \quad (4.15)$$

For differential signals:

$$PW_{MIN} > (t_{pd\_max}) \quad (4.16)$$

where:

t_{pd_max} = the delay of the macro plus the metal/fanout delay of the macro output. For duty cycles less than 40% or greater than 60%(data signals), multiply t_{pd_max} times a factor of 1.6 (See section 4.5).

If the pulse is going to an output pin from an output macro, the pulse at the pin(s), after the pulse width shrinkage is calculated, should be at least 1.6 times the worst-case rise time of the output for single-ended outputs. For differential outputs driving differential receivers, the output pulse width should be greater than 0.8 times the output rise time.

4.5 BIT RATE VERSUS FREQUENCY

A relation between frequencies (~50% duty cycle) and bit rates can be made by multiplying the frequency by a factor of 1.6. Therefore, if a frequency specification is 1.6 GHz, this can be translated to 2.56 Gb/s (1.6 X 1.6 GHz). The reason a direct 2 to 1 translation between frequency and bit rate can not be made is that the frequency specifications are for a 45 to 55% duty cycle. Bit rates will not exhibit this duty cycle and can produce minimum V_{OL} or V_{OH} levels on internal and I/O macros. At high frequencies, a 45 to 55% duty cycle signal may never reach minimum V_{OL} or maximum V_{OH}; therefore, a smaller swing is required to reach the switch point. In general, the 1.6 multiplication factor to determine the bit rate will ensure macro switching for levels at maximum V_{OL} or minimum V_{OH}.

5. CLOCK DISTRIBUTION

In order to achieve the highest performance with ECL gate arrays operating above 1 GHz, good storage elements, special circuit design techniques, and clock distribution schemes are required. Through a carefully designed clock distribution network with manual placement and routing, the designer can keep the sum of the storage-element delay, setup time, and clock skew to a minimum. Clocking schemes are typically limited to a single-phase latch or flip-flop design. This approach usually achieves the highest performance since the least number of elements and minimal clock wiring is required. However, considerable control of minimum and maximum delays is necessary to prevent race conditions.

5.1 SINGLE-PHASE CLOCKING WITH FLIP-FLOPS

Single-phase edge-triggered flip-flop designs are preferred over a latch based design since less severe race conditions exist. The cycle time in such a flip-flop based design is given by:

$$T_{cycle\_min} = T_{dmax} + T_{ms} + T_{skew\_max} \quad (5.1)$$

where:

T_{dmax} = the maximum flip-flop, logic, and metal delay between two flip-flops

T_{ms} = flip-flop setup time

T_{skew_max} = maximum skew between clocks

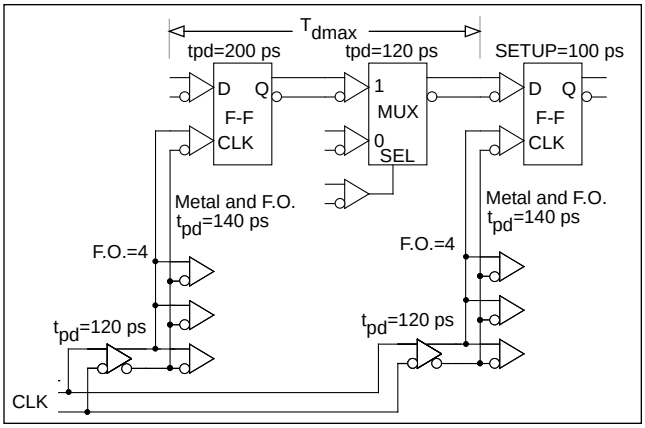


Figure 5-1 Example Circuit for Maximum Cycle Time Calculation

Using equation 5.1 and the example MCA3 ETL array circuit in Figure 5-1 a calculation of the minimum cycle time will now be performed. High speed flip-flops with clock to output delays of 200 ps and setup times of 100 ps are driven from a simple clock network. A differential logic gate, such as a 2:1 multiplexer, is between the two flip-flops comprising a T_{dmax} macro delay of 120 ps. Assuming the metal path between the flip-flops and logic gate is relatively short, the metal and fanout delay would be about 20 ps or a total of 40 ps for the T_{dmax} metal and fanout delay portion. The skew for a differential single stage clock tree with matched nets and fanout of 4 on each buffer would result in a clock skew of 40 ps. This is derived by using the delay skew factors for MCA3 ETL arrays.

$$T_{skew\_max} = 10\%\,of\,differential\,macro\,delay + 20\%\,of\,differential\,metal\,and\,fanout\,delay$$

$$T_{skew\_max} = 0.1\,(120ps) + 0.2\,(140ps) = 40ps$$

Using equation 5.1 would result in the following cycle time:

$$T_{cycle\_min} = (200 + 120 + 40) + 100 + 40 = 500ps$$

or 2.0 GHz

In a simple divider circuit, there is no need for a logic gate in between the two flip-flops. A calculation of the cycle time would yield:

$$T_{cycle\_min} = (200 + 20) + 100 + 40 = 360ps$$ or 2.8 GHz

It should be noted that the maximum operating frequency of the flip-flop is 2.5 GHz and therefore the minimum cycle time would be determined by the flip-flop operating limit.

5.2 CIRCUIT DESIGN TECHNIQUES FOR EASING CLOCK DISTRIBUTION

From the above calculations, it can be seen that delays and skews must be held to a minimum in order to achieve over 2.0 GHz operation. One method for improving the operating frequency can be achieved by reducing any logic delay between two flip-flops. This can be done by integrating certain logic functions into the master section of a flip-flop. Three commonly used functions include an OR/NOR gate, 2:1 mux, and an EXNOR gate. Flip-flop circuits with these logic functions were fabricated for the MCA3 ETL array library and were simulated and measured in the lab. Nearly identical setup, hold, and delay characteristics as those specified for a simple data input flip-flop were found.

In general, a minimal stage clock distribution network is desired to minimize the delay and keep the layout simple. However, the number of macro fanouts will be higher than for a multi-stage clock network. This will result in large delays on the net especially when driving high speed macros. This is due to the fact that when driving upper level inputs of the high speed macros, large input capacitance occurs due to the higher currents through the input transistor. To reduce the loading, and thus the delay, an input follower may be integrated into the ECL upper level input with very little impact on the performance of the macro. A speed/power trade-off of the current through the emitter follower must be chosen such that the additional delay is small while maintaining an acceptable power increase. Also, as the current increases through the emitter follower, the input capacitance will increase. As an example, the macro L474 and L700 in the MCA3 ETL library are 1.1 mA switch current buffers with standard upper level inputs and buffered (emitter follower) inputs respectively. The differential delays are specified within less than 10 ps with the L700 slightly larger. The input capacitance for the L474 is 0.12 pF for a DC fanin of 4. The L700 has an input capacitance of 0.09 pF with a DC fanin of 2. The power for the L474 is 5.7 mW while the L700 is 10.6 mW. As can be seen, an 86% increase in power occurred for a 25% reduction in input capacitance and a 50% decrease in DC fanin. The percentage increase in power is largest for a differential buffer since two emitter follower inputs are used and the power of the switch current is small.

5.3 PLACE AND ROUTE TECHNIQUES FOR EASING CLOCK DISTRIBUTION

Unless specialized software is available, it is best to perform a manual placement of the clock drivers and clocked elements for very high speed circuits on an ECL gate array. The designer should have the macro layout drawings with the port locations clearly identified. This will allow the ability to obtain minimum metal lengths, as well as matched line lengths, for all critical elements. Macro orientation within a cell location is critical for achieving perfectly matched clock networks. Orientation should provide the macro layout to be flipped about both a vertical and horizontal axis. This allows the designer to generate mirrored images of clocked elements such that identical minimum length clock nets on all layers of metal is achieved. Depending on the process technology, the available metal layers used for routing may have significant differences in resistance and capacitance thus resulting in time of flight and propagation delays being different for equal metal lengths.

6. EXAMPLES OF HIGH FREQUENCY DESIGN TECHNIQUES

Figure 6-1 contains two clock driver circuits. The circuit in a) has a differential clock input, a clock disable input, and a single-ended clock output. The circuit in b) has the same inputs as a) however, it produces a single or differential clock output. This circuit uses a differential multiplexer to produce a differential OR function. A benefit for both techniques is that no decoding glitches occur therefore making it useful in clock driver and decode applications. With a simple modification, the circuit in b) generates a negative clock pulse every two clock periods with minimal clock pulse shrinkage. To achieve this, the flip-flop input and output are connected together to produce a divide by two function.

For clock distribution, attempts to limit the high speed clock to a minimum is often preferred. Techniques such as clocking data on both the rising and falling edges of a clock and using parallel data blocks can reduce the clock rate in half. For example, consider a 2.5 Gb/s incoming data stream. To capture this, one would require a 2.5 GHz clocked flip-flop. A designer may find it possible that the incoming data could be connected to two flip-flops operating at 1.25 GHz. One flip-flop captures the data on the rising edge, while the other on the falling edge of the clock. Therefore, the clock network and flip-flops always operate at a maximum of 1.25 GHz. This is an advantage in the MCA3 ETL array technology since flip-flops capable of 1.66 GHz operation are half the size and power as those that operate at 2.5 GHz.

In certain designs, it may be desirable to clock data at the clock rate even it if means using higher power and larger devices. Ideally, one would limit their use to the input or output stage of the circuit. The following are two examples of a demultiplexer and multiplexer using this technique.

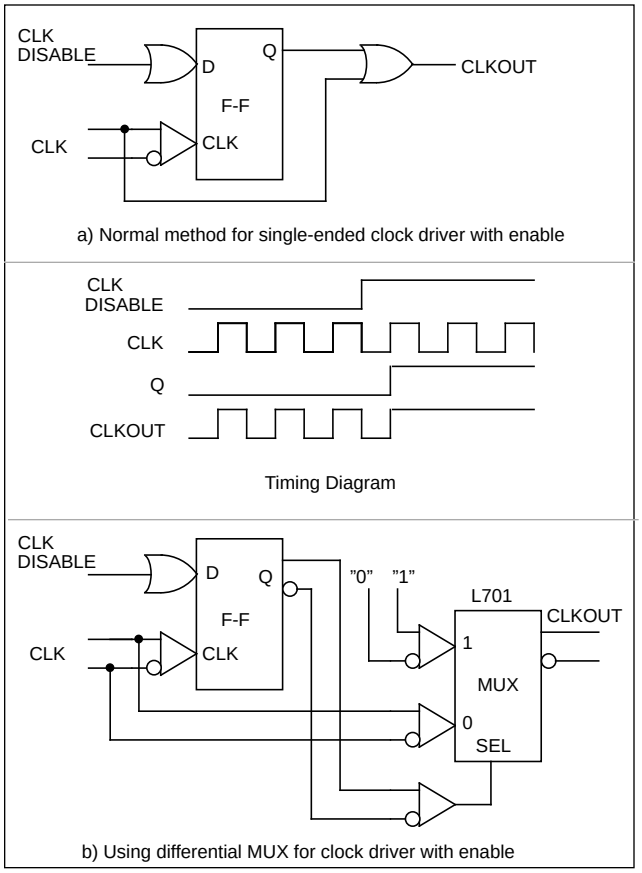


Figure 6-1 Clock Driver Circuits with Enable

The first example, found in the final stage of a high speed multiplexer, depicts a circuit used on an MCA3 ETL array to achieve a 2.5 Gb/s output data signal (see Figure 6-2). The data signal is retimed at the clock rate resulting in a clean, low jitter output signal. To provide the correct timing of the clock at flip-flop Q2, it was necessary to delay the input clock by the clock to output delay of a flip-flop. A delay macro, D1, that emulated the exact delay of a flip-flop itself, provided the necessary delay. The delay macro also proved useful in reducing the skew between the output data and clock signals at the output of the multiplexer. In this example, macro D2 delayed the clock such that the off-chip skew between the clock and data signal did not exceed 75ps.

The second example is an initial stage of a high speed demultiplexer (see Figure 6-3). The input flip-flops operate at the full clock cycle (2.5 GHz) while the following flip-flops are clocked at one half the input clock rate. As seen from the demultiplexer timing diagram, the data change occurs on the negative edge of the clock and synchronized by flip-flop Q1. Q2 is connected in a divide by two configuration that is clocked on the negative edge of the clock to provide timing to Q3 and Q4. These flip-flops split the data stream into two paths, each at one half the original rate.

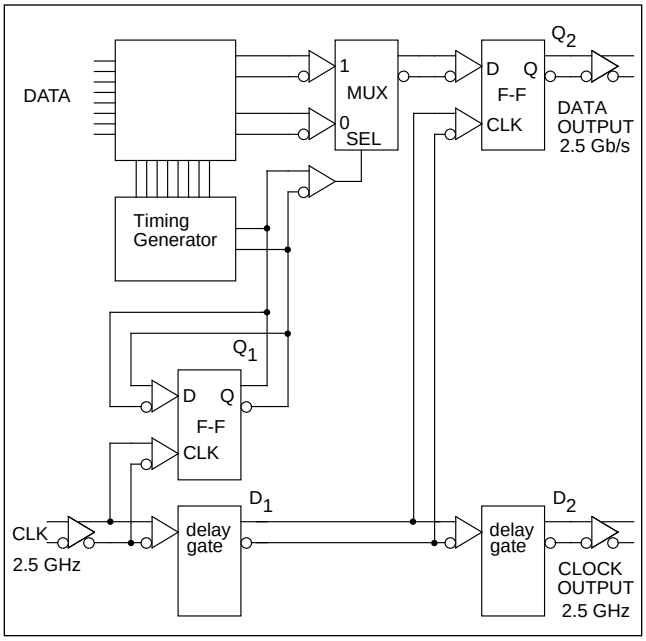


Figure 6-2 High Speed Multiplexer

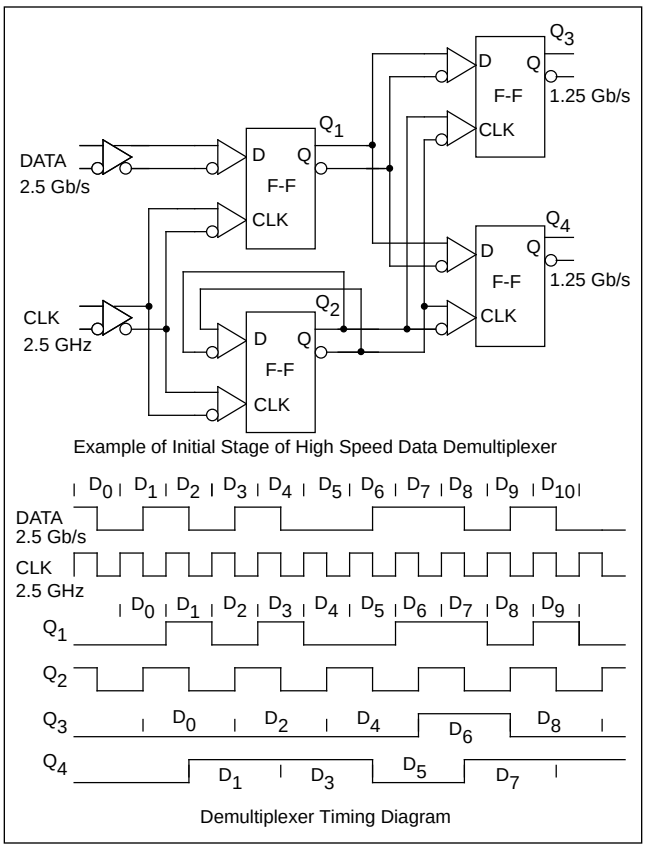


Figure 6-3 High Speed Demultiplexer

7. SUMMARY

This application note has discussed numerous considerations, guidelines, and applications concerning high frequency operation for bipolar gate arrays. Through examination of Motorola's MCA3 ETL array series, descriptive examples, actual and simulated data, as well as, state of the art information is given. Depending on the design application, it may be possible to fabricate a high speed circuit in a relatively low cost bipolar gate array. As discussed in section 2. and section 3., limitations in packaging, I/O termination, and voltage levels can be surmounted to allow on and off-chip signal interfacing up to 2.5 GHz. With an established, well characterized process, including on-chip delay skew factors, pulse width shrinkage and minimum pulse width specifications, high speed circuits can be designed to worst case with a high probability of first pass operation. In fact, Motorola guarantees operation up to 2.5 GHz on MCA3 ETL arrays when all AC and DC guidelines are observed. To assist in implementing these guidelines, several clock distribution and circuit design techniques were given that can optimize the internal operating frequency and/or enhance circuit integrity.

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