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APPLICATION NOTE

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H4CPlus™ and H4EPlus™ Series 3.3V/5V Design Considerations

Prepared by: David Crohn
and Peter Economopoulos
Motorola, Chandler AZ

INTRODUCTION

The H4CPlus and H4EPlus Series technologies offers the ability to implement designs with one of two possible core voltages, in combination with all 3V, all 5V, or mixed 3V/ 5V I/O designs. To achieve this end, it is helpful to understand how this technology is implemented, and how to incorporate these details into the design via Motorola's Open Architecture CAD System (OACS™) interface.

Throughout this application note, 3.3-volt I/Os will be loosely referred to as 3-volt I/Os, since the operating range is selectable from 3.0 ±.3 volts, to 3.3 ±.3 volts, and is not required to be 3.3 volts.

This application note is best understood if the reader has a working knowledge of the Motorola OACS[1] design tools.

OBJECTIVE

This application note provides the knowledge necessary to implement designs that are all 3V, all 5V, or mix both 3- and 5- volt I/Os and a single core voltage of either 3 or 5 volts in both the H4CPlus and H4EPlus Series CMOS array families.

1. DESIGN DETAILS

1.1 Power Rail Configuration

An H4CPlus and H4EPlus array has five distinct power and ground rails, which are shown in Figure 1. An H4CPlus and H4EPlus Series array contains an output power rail for powering 5-volt outputs named the OVDD5 rail, an output power rail for powering 3-volt outputs named the OVDD3 rail, an output ground bus named OVSS, and the core power and ground rails named VDD and VSS, respectively.

1.2 Technology Selection

There are two distinct technology libraries to choose from when implementing either a H4CPlus or a H4EPlus design. They are the H4CP3 library, which contains all of the 3-volt core macros along with the 3-to-3 and 3-to-5 volt I/Os, and the H4CP5 library, which consists of all the 5-volt core macros with the corresponding 5-to-5 and 5-to-3 volt I/Os available for that technology. The selection process is the same as selecting between array families (e.g., HDC and H4C Series) in the OACS DESIGN_INFO tool today. Once a given technology has been selected, accessing macros in the other technology is neither possible, nor desirable.

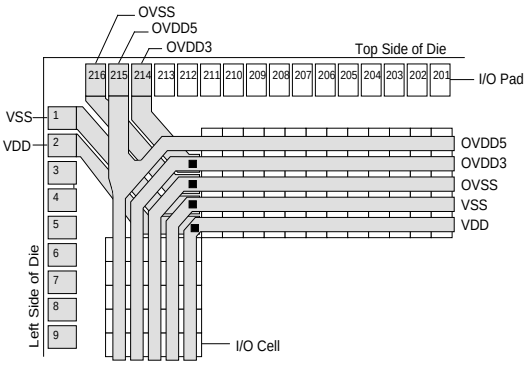

Figure 1 H4CPlus and H4EPlus Power and Ground Busses

1.3 Macro Naming Conventions

The H4CPlus and H4EPlus macro naming conventions have been selected to simplify the design process. There are two distinct conventions to describe: those for the core macrocells, and those used in the I/O portion of a design.

1.3.1 Core Macrocells

Core macros have the same name regardless of technology selected. The only difference between the technologies for core macros is the timing data, since H4CP3 has been characterized at 3.3 volts, and H4CP5 at 5.0 volts. Section 1.2 describes the H4CP3 or H4CP5 timing data selection process.

1.3.2 I/O Macrocells

A consistent naming convention has been put in place so that I/O selection can be done easily. The two key characters

used are “L” and “X”. Remembering the following two rules — that always apply— will simplify macro selection. An “L” in the I/O macro name always indicates that the macro has been designed for a 3-volt external interface. An “X” always indicates that there is a translation of voltage between the core and the external interface voltage.

Consequently, the H4CP3 technology will contain only I/O macros with either an “L” or an “X” in their names, but not both. The names of H4CP5 I/O macros will either contain both letters (L and X) together or neither letter- e.g. ONLX8 or ON8.

For example, an ONL8 is an 8mA output with a 3-volt core and a 3-volt interface. An ONX8, is a macro with a 3-volt core and a 5-volt interface. Both of these macros would be found only in the H4CP3 library. An ON8 is a 5-volt core, 5-volt interface macro. An ONLX8 is a 5-volt core, 3-volt interface macro. Both of these macros would be found only in the H4CP5 library.

1.3.3 Special 3-Volt I/O Considerations

The usage of 3-volt receivers in a technology that allows 3 and/or 5-volt supplies has three points that require explanation.

The first is with respect to the input threshold. Due to the small difference between 3-volt CMOS and TTL thresholds, no distinction is made. Consequently, an ILTN macro will not be found in the H4CP3 library. Instead an ILCN with a VDD/2 threshold is used, since the small difference in threshold was not considered justification enough to create a separate 3-volt TTL receiver at this time.

The next design impact to consider is steady state current draw consumed by 3-volt inputs with a 5-volt core voltage, such as an ILTXN. Receivers are powered by the core voltage, which in this case would be 5 volts. A high on the 3-volt input would result in the receiver never completely cutting off the P-channel transistor. For a 3.3-volt signal, and a 5-volt core with typical conditions this current would be 225µA, and with a TTL input high of 2.0 volts this current would be 850µA.

The steady state current is only a power issue and will cause no degradation in the performance or functionality of the receiver over time, but the designer needs to be aware that this condition exists. This current is included by ERC during its DC power consumption analysis.

The final point is in regards to the type of receiver a 3-volt output is driving. three-volt outputs should not drive CMOS inputs, since VOH requirements can not be guaranteed. ERC will flag any invalid bi-directional combinations in a design, such as a BICN used with a BONLX8T. This check cannot be done for external loads, since ERC does not know what type of receiver is being driven by the 3-volt output. Refer to the “H4CPlus Series Design Reference Guide” [2] DC Electrical Characteristics chapter for the 3- and 5- volt specifications when implementing the I/O portion of the design.

1.4 Power Bus Tying

Many legitimate power bus tying combinations are possible with H4CPlus or H4EPlus. Both output rails (OVDD5 and OVDD3) can be tied, or the core power rail can be tied to either output power rail, or all three power rails can be tied together as well.

The mechanism for choosing which buses to tie is the OACS DESIGN_INFO tool. The first selection to make is whether to use the 3-volt or 5-volt technology. The next selection is whether the I/O is all 3-volt, all 5-volt, or a mix of the two. An important point to understand is that this question pertains to the interface voltage, and not necessarily the voltage at which the I/O operates.

Making this selection isn’t always as easy as it would appear to be. At first glance, a design with a 3-volt core and all 3-volt outputs with a 5-volt input, such as an ICXN, may appear to only require 3-volt power since inputs are powered from the core. Even though this macro is powered from the core, it still requires the OVDD5 power to be provided with 5 volts to prevent forward-biasing the protection diode when 5 volt signals are received at the input. So even though the input macro and all of the outputs are powered by 3 volts, it is incorrect to select all 3-volt I/O, since 5 volts is required as well.

The basic rule of thumb is this: The only time “I/O Type 3.3v” can be selected in DESIGN_INFO is if all I/O macros used contain an “L” in their name. The only time “I/O Type 5.0v” can be selected in DESIGN_INFO is if all I/O macros do not contain an “L” in their name. Any other scenario would require that “I/O Type mixed” be selected in DESIGN_INFO.

The final selection to make is whether or not to tie the core power rail to either of the output rails, if outputs exist in the design that operate at the same voltage as the core.

For example, if H4CP5 is the technology selected, and all 3.3-volt I/O is indicated, then the question to answer regarding the tying of the core to the output rail would disappear, since all the I/O are at a different potential than the core.

There is one exception to designer-controlled bus tying selection. If all 3.3-volt or 5-volt I/O is selected, then by default the two output power buses OVDD3 and OVDD5 will be tied. There are several reasons for this. First, dedicated power pins to the unused power rail can now be used to provide power to the utilized power rail. Second, this prevents a floating metal ring around the array from building up excess charge. Finally, the added bus capacitance and reduced pin inductance are advantageous for improving the SSO environment.

Valid DESIGN_INFO selections are verified by ERC. Running ERC early on, and frequently as the I/O portion of the

design is implemented, prevents time consuming corrections that may not otherwise be found until the final stages of ASIC development.

1.4.1 Power Bus Macro Selection

A full set of design selectable power macros exist that enable designers to place powers and grounds where necessary, and either tie or provide the individual rails as needed by the design. Table 1 gives the macro name and the associated power or ground bus supplied by that macro. Table 2 shows which programmable power macros to use based on the design outlined by entries in DESIGN_INFO. Figures 2-11 illustrate the core, I/O, and bus tie connections for the various scenarios listed in Table 2.

Table 1. Macro Definition

MACRO NAME	BUS SUPPLIED
ALLVDD	VDD,OVDD3,OVDD5
BOTHOVDD	OVDD3, OVDD5
BOTHVDD3	VDD, OVDD3
BOTHVDD5	VDD, OVDD5
OVDD5	OVDD5
OVDD3	OVDD3
VDD	VDD
OVSS	OVSS
VSS	VSS

Table 2. Macro Selection

Customer Options in DESIGN_INFO			MACRO NAME							
Technology Selection	I/O Type	Tie Core Rail to I/O Rail	VDD	OVDD3	OVDD5	ALLVDD	BOTHOVDD	BOTHVDD3	BOTHVDD5	Figure
H4CP3	All 3 Volt	No	X				X			2
H4CP3	All 3 Volt	Yes				X				3
H4CP3	Mixed	No	X	X	X					4
H4CP3	Mixed	Yes			X			X		5
H4CP3	All 5 Volt	N/A	X				X			6
H4CP5	All 5 Volt	No	X				X			7
H4CP5	All 5 Volt	Yes				X				8
H4CP5	Mixed	No	X	X	X					9
H4CP5	Mixed	Yes		X					X	10
H4CP5	All 3 Volt	N/A	X				X			11

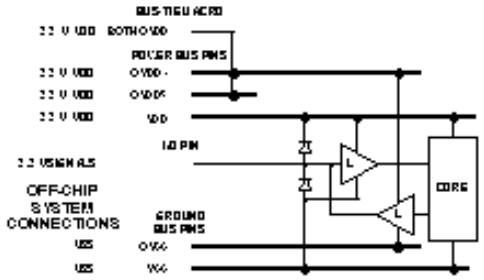

Figure 2 Example of a 3.3 V Core with 3.3 V I/O and OVDD3 & OVDD5 Tied

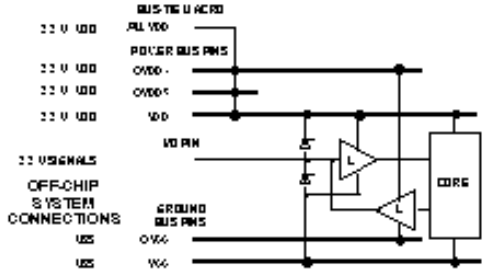

Figure 3 Example of a 3.3 V Core with 3.3 V I/O and All VDD Tied

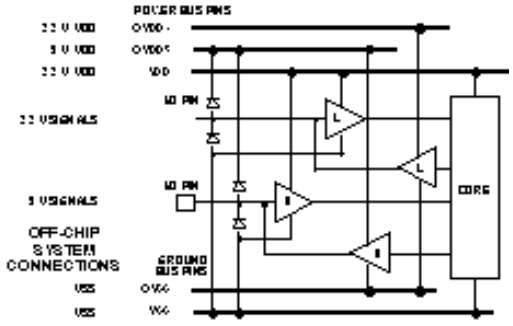

Figure 4 Example of a 3.3 V Core with Mixed 3.3V/5V I/O and No VDD Ties

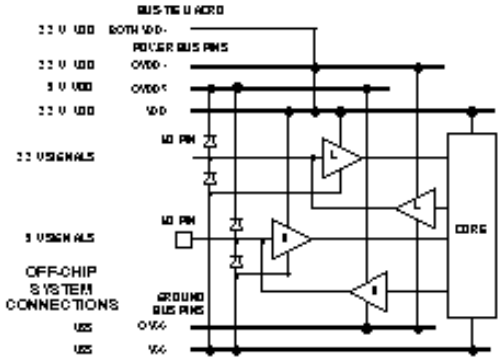

Figure 5 Example of a 3.3 V Core with Mixed 3.3V/5V I/O and OVDD3 & VDD Tied

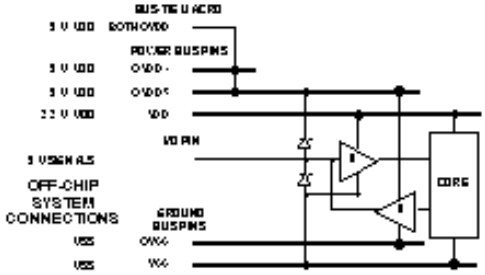

Figure 6 Example of a 3.3 V Core with 5 V I/O and OVDD3 & OVDD5 Tied

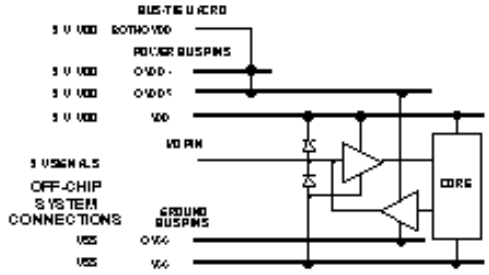

Figure 7 Example of a 5 V Core with 5V I/O and OVDD3 & OVDD5 Tied

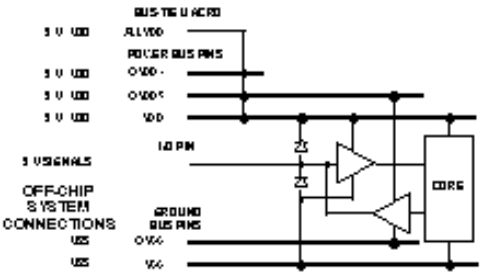

Figure 8 Example of a 5 V Core with 5V I/O and All VDD Tied

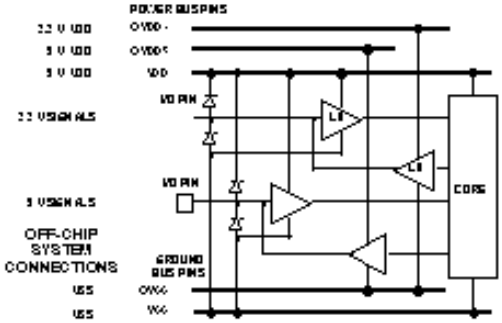

Figure 9 Example of a 5 V Core with Mixed 3.3V/5V I/O and No VDD Tied

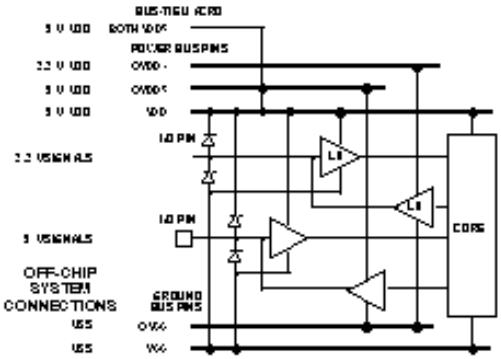

Figure 10 Example of a 5 V Core with Mixed 3.3V/5V I/O and OVDD5 & VDD Tied

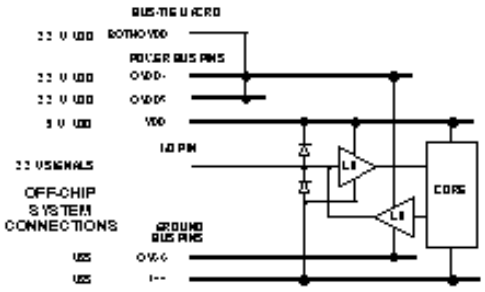

Figure 11 Example of a 5 V Core with 3.3 V I/O and OVDD3 & OVDD5 Tied

1.5 Propagation Delay Adjustments

When simulating with timing, propagation delay adjustments can be applied to macros powered by 3 volts independently of macros powered by 5 volts. The DESIGN_INFO tool has entries for a designer to select best-, typical-, and worst-case voltages for the 5-volt rail and for the 3-volt rail independently. The associated delay adjustments would then be applied to macros powered by the given rail.

For example, a design with a 5-volt core may have all 3-volt I/Os, but it is desired to run the I/Os at 3.0 rather than at 3.3 volts. Simply modify the values in DESIGN_INFO to be 3.0±.3 volts, and leave the 5-volt rail at 5 volts. The appropriate delay adjustments will then be applied to the 3-volt I/Os, independently from the adjustments made to the macros powered by the 5-volt supply.

There are limits to the range of voltage adjustments possible. If the H4CP3 technology is selected, and the designer requests the design's core power supply to be 4.5 volts, then an error will occur, since if this is the true operating voltage, then a switch to the H4CP5 technology should be considered. H4CP5 has been characterized at 5.0 volts, and provides more accurate timing being scaled to 4.5 volts, rather than scaling 3.3-volt data to 4.5 volts, which exceeds the range of the scaling equations.

Although ranges typically selected for the 3-volt supply will be from 2.7 volts (worst-case) to 3.6 volts (best-case), DESIGN_INFO will allow selections up to 4.0 volts to be made. Similarly for the 5-volt supply, typical selections will be from 4.5 volts (worst-case) to 5.5 volts (best-case), but selections down to 4.0 volts are allowed. Selections outside these ranges will cause fatal errors when DECAL [1] attempts to apply voltage adjustments that don't exist.

The designation for the two supplies in DESIGN_INFO is VDD for the core and output power rail(s), if supplied by the same voltage, and VDD2 for the alternate output power rail. So, if "Technology H4CP3" is selected, then the default range for VDD will be from 3.0 to 3.6 volts, and from 4.5 to 5.5 volts for VDD2. If "Technology H4CP5" is selected, then the default range for VDD will be from 4.5 to 5.5 volts, and from 3.0 to 3.6 volts for VDD2. If the "I/O Type" and "Technology" selections are for the same voltage, the VDD2 will be removed, and only the VDD entry will remain, since at that point it is known that the core and both output power rails will be operating at the same potential.

1.6 Pull-ups and Pull-downs

Pull-downs always tie to the output ground rail OVSS. The pull-ups, however, always tie to the core VDD rail. There are two scenarios which present potential design concerns.

The first scenario is for designs which have a 3-volt core and 5-volt inputs. The consequence is having the 5-volt input to 3-volt core potential difference across the pull-up resistor. This is not a serious problem, since the current through the pull-up will be small, with the difference of the 5-volt signal to the 3-volt core across a large resistance.

The second scenario is where bidirectional buses are employed that have 5-volt swings and have pull-ups to the 3-volt core. When the bus is tri-stated, the steady state would be 3 volts, and not 5 volts unless pulled to 5 volts through some external termination.

The suggested approach for these two scenarios is to use pull-downs if some type of pull resistor is absolutely necessary. Pull-ups can be used if the consequences mentioned above are understood, and can be tolerated by a given design. Simulation does not differentiate between pull-ups to 3 and 5 volts, and ERC will not flag these as errors or warnings, since neither scenario is destructive.

1.7 SSO and Power Requirement Rules

This section addresses the electrical restrictions to consider when implementing the I/O portion of a design. These considerations can be broken down into two distinct areas: AC analysis or Simultaneously Switching Outputs (SSO), and DC power requirements.

1.7.1 SSO Analysis

Every output, whether it be 3- or 5-volt, has a drive parameter for it. ERC uses the parameter in conjunction with the package chosen, to do a detailed SSO analysis of a design, and flag problem areas as errors. A more comprehensive explanation of this analysis is covered in Chapter 3 of the "H4CPlus [2] or the H4EPlus [3]Series Design Reference Guide".

It is this analysis by ERC that offers designers tremendous flexibility when implementing mixed I/O designs. Although one needs to be cognizant of I/O partitioning and placement of power and ground based on the discussion of SSOs in the "H4CPlus [2] or the H4EPlus [2] Series Design Reference Guide" , there are no special restrictions regarding isolation of 3- and 5-volt I/Os, and no ground pad separation require-

ments. In the event an oversight is made, ERC will inform the designer where the violation has occurred so corrections can be made early on in the design cycle.

There is one consideration to keep in mind when implementing the I/O portion of a design. ERC will do either a CMOS or TTL SSO analysis for each of the SSO segments based on the macros found in the SSO segment. An SSO segment is defined as the group of I/Os found between two output power or ground macros. This means there are two distinct SSO segments for ERC to analyze for each output macro. One for the output power rail (OVDD5 or OVDD3) it uses, and one for the output ground rail OVSS. The individual analysis is necessary since the SSO noise sensitivity to the different technologies (e.g., CMOS and TTL for 3 and 5 volts) is different.

The first step in doing SSO analysis is determining whether a SSO segment is TTL or CMOS. If for a given SSO segment an `OUTPUT_THRESHOLD` of TTL is found on an output, any 3-volt outputs are found, or a TTL or 3-volt input are found within the segment, then TTL analysis will be done. Otherwise, CMOS analysis will be applied.

For example, say a design has an SSO segment with an OVDD5 and an OVSS pad on each end. If seven of them drive CMOS loads, and one drives a TTL load (determined by the value of the `OUTPUT_THRESHOLD` property), then TTL SSO analysis will be applied to that segment, even though seven of the loads drive CMOS levels. In this case the SSO noise seen at the TTL output would be the first to fail, and would be the weakest link in that SSO segment. The same argument can be applied if one of the macros in this predominantly CMOS segment were a 3-volt or TTL input.

The point of this discussion is to communicate the flexibility available for creating mixed-voltage I/O designs in the H4CPlus or the H4EPlus technology, but at the same time pointing out the consequences of design choices, so intended design objectives can be achieved.

1.7.2 DC Power Requirements

There are two basic DC power requirements to meet: IR loss and current density. The rule used for IR loss is the 25 I/O site rule, which states that a macro cannot be more than 25 I/O sites from the power site it is drawing its power from. This applies only to the output power rails, since the core-powered inputs always power CMOS loads, which don't require a steady state current source like an output may potentially need. The same rule is used for both 3- and 5-volt outputs, since the IR loss for the 25 I/O sites has enough margin to satisfy both and is not believed to be overly restrictive in either case.

The current density rule is 64mA per power/ground pin. ERC simply performs a current requirement calculation, divides out the number of powers and grounds available, and determines if there is enough or not. Once again, 3- and 5-volt outputs are given the same treatment. Whether an 8mA output is 3 or 5 volts, it is still designed to drive 8mA, therefore 8mA would be used by ERC during its analysis.

1.8 Testing

Option testing will be done at both 3.3 and 5.0 volts for designs which use both voltages. With two power rails, testing at the simulated voltages is necessary to make sure that the part functions properly at the voltages for which it was intended. Two other points to mention are power cycling of mixed-voltage designs and IDD testing.

1.8.1 Power Cycling

During test and in its application, the 5-volt power should be applied to the option before the 3-volt power, and similarly the 3-volt power should be removed before the 5-volt power. This will prevent parasitic devices from experiencing transients greater than their supply voltage.

1.8.2 Enable IDD (ENID) Pin

H4CPlus and H4EPlus offer the ability to do IDD testing without having to put special test vector requirements on designers via the addition of the ENID pin. All H4CPlus and H4EPlus designs are required to designate one pin for ENID by instantiating the symbol and defining the `IO_PIN1` property to the desired pin. When ENID is high all pull-up and pull-down resistors, and current sources in differential receivers are disabled, which enables accurate IDD testing independent of the state of the test vector. ENID has an internal pull-down to allow a design to function without tying it to ground. However tying ENID to ground in the system is still advised.

2. SUMMARY

This application note should give a designer having previous OACS experience the information necessary to expeditiously create 3- and/or 5-volt designs using the H4CPlus or the H4EPlus technology.

REFERENCES

(1) M. Vening, OACS User Guide, Order # 0384-OACS-U.0 from the Motorola ASIC Hotline (1-800-MDS-ASIC in the USA), October 1993.

(2) C. Nakata, J. Brock, H4CPlus Series Design Reference Guide, Order # H4CPDM/D from the Motorola Literature Distribution Center.

(3) Prliminary H4EPlus Series Design Reference Guide.

NOTES:

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