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High-Performance CMOS Interfaces for the H4CPlus™ and H4EPlus™ Series Gate Arrays

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INTRODUCTION

High speed bus and point-to-point interfaces between CMOS ASICs are no longer limited to conventional CMOS-level signals. Data rates over 500 Mb/s have been reported with low-voltage interfaces operating in a differential point-to-point terminated transmission line environment. Gunning Transceiver Logic (GTL), Current Mode Transceiver Logic (CMTL), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signaling (LVDS) are some of the latest emerging standards available to CMOS ASIC designers. Each has advantages and disadvantages thus making it more difficult to select the appropriate circuitry for an application.

Motorola's H4CPlus and H4EPlus Series CMOS gate arrays accommodate off-chip differential and single-ended signaling in a transmission line environment for a variety of interfaces at supply voltages of 5.0 and 3.3 volts. PECL, CMTL, and GTL transceivers are available.

This application note presents CMTL, GTL, PECL, and LVDS I/O interfaces as implemented in the H4CPlus and H4EPlus Series Gate Arrays. Transmission line concepts, termination techniques, voltage levels and circuit requirements of how to utilize these I/O are presented. Finally, measurements, simulations, and operating recommendations are given.

1. High-Speed Interface Macros

Motorola's H4CPlus and H4EPlus Series arrays feature 3.3 V, 5.0 V and mixed-voltage capability, high-speed interfaces, and a host of additional features and capabilities. A 0.65 µm Leff gate length provides superior 5 V performance and competitive speed at 3.3 V. Refer to the H4CPlus and H4EPlus Series Design Reference Guides for complete specifications of this product.

Table 1-1 contains a complete list of available high-speed interface macros for the H4CPlus and H4EPlus arrays.The following is a description of each high-speed interface discussed in this report.

2. CMTL Characteristics and Operation

CMTL has been designed by Motorola to provide a practical high speed transmission line interface with the following characteristics.

- Reduced voltage swings
- Low standby power
- High noise margins
- No external components for point to point
- Matched resistor termination for multi-tap
- Single or differential drive
- Differential bidirectional bus driving (25 Ω load)
- Optional internal active termination

The CMTL driver output stage is a complementary push-pull CMOS output stage with a reduced output voltage swing centered approximately at the mid-point of the V_{DD} power supply ($V_{DD}/2$). The output swing is reduced compared to CMOS outputs by using an N channel device connected to V_{DD} and a P channel device connected to V_{SS}. The output stage eliminates the Miller capacitance and uses smaller devices in order to provide a higher bandwidth. The basic theory of operation is described in (1). In addition to standard external termination schemes (2), H4CPlus and H4EPlus

Table 2-1 H4CPlus and H4EPlus Series System Interface Macros

Input Macro	System Logic		Core Logic		Inverting	Non-Inverting	Differential	JTAG
	3.3V	5.0V	3.3V	5.0V				
CMTL Input Logic								
BICMD		•		•			•	
ICMD		•		•			•	•
ILCMD	•		•				•	
GTL Input Logic								
BIGN		•		•		•		•
IGI		•		•	•			
IGN		•		•		•		•
BILGN	•		•			•		•
ILGI	•		•		•			
ILGN	•		•			•		•
IGD		•		•			•	
ILGD	•		•				•	
PCI Input Logic								
IPCH		•		•		•		•
IPCXN		•	•			•		•
IPCXNH		•	•			•		•
BIPCXN		•	•			•		•
ILPC	•		•			•		•
ILPCH	•		•			•		•
BILPC	•		•			•		•
PECL Input Logic								
IPD		•		•			•	•
IPN		•		•		•		
ILPD	•		•				•	
ILPN	•		•			•		
IPXD		•	•				•	
IPXN		•	•			•		

Output Macro	System Logic		Core Logic		Differential	JTAG
	3.3V	5.0V	3.3V	5.0V		
CMTL Output Logic						
BOD32TCMT		•		•	•	
O32CM		•		•		
OD32CMT		•		•	•	•
OD32TCMT		•		•	•	•
ODX32CM		•	•		•	
ODLX32CMT	•			•	•	
ODL32CMT	•		•		•	•
GTL Output Logic						
BON40G		•		•		•
ON20G		•		•		•
ODL20G	•		•		•	
OD20G		•		•	•	
BONL40G	•		•			•
ONL20G	•		•			•
PCI Output Logic						
BONTPC		•		•		•
BONXTPC		•	•			•
BONLXTPC	•			•		•
ONPCS2		•		•		•
ONPC		•		•		•
ONTPC		•		•		•
BONLTPC	•		•			•
BONTPCS2		•		•		•
ONLPC	•		•			•
ONLTPC	•		•			•
ONXPC		•	•			•
ONXTPC		•	•			•
ONLXPC	•			•		•
ONLXTPC	•			•		•
ONTPCS2		•		•		•

CMTL offers on chip active termination. Figure 2-1 shows an example of the OD32TCMT macro, a 32 mA CMTL differential output driver with an active termination across the outputs (denoted with the symbol “T”). The active termination is a pair of FETs connected like back to back diodes in order to further limit the swing at the output. The active termination sets the quiescent current of the driver at about 3.7 mA for V_{DD} = 5.0 V while the quiescent current is only 0.1 mA for V_{DD} = 3.3 V.

The OD32TCMT/OD32CMT is used to drive twisted pair line (Z_O = 100 to 150Ω) or two controlled impedance pc board (PCB) lines (Z_O = 50 to 100Ω). The latter may have a CMTL receiver connected at the end of the lines without using termination resistors. In addition, each output of the CMTL driver will drive a load of 25Ω with resistor termination (as low as 50Ω) at both ends of the transmission line. The resistors are not needed for point to point connections due to the effective output impedance of the driver (32Ω for V_{DD} = 5.0 V and 50Ω for V_{DD} = 3.3 V) which provides a series termination for twisted pair lines having a Z_O of 100Ω or controlled impedance PCB lines having a Z_O of 50Ω. For multi-taps on the lines, a resistor can be placed across the twisted pair at the end of the line with a value equal to the characteristic impedance of the pair of lines. Figure 2-2 shows an example of the ICMD macro which is a CMTL differential receiver. For V_{DD} = 5.0 V, the receiver has a maximum input sensitivity of ±200 mV differential, for frequencies less than 200 MHz.

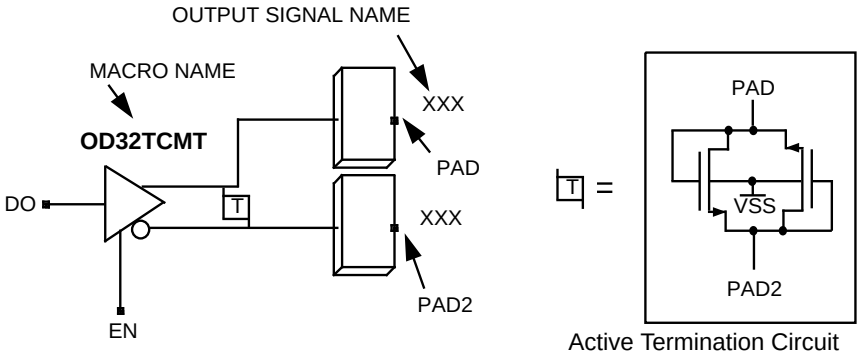


Figure 2-1 Example CMTL Driver Symbol

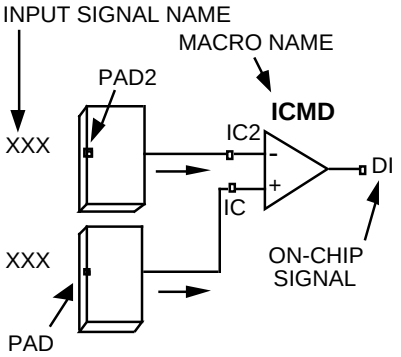


Figure 2-2 Example CMTL Receiver Symbol

2.1 CMTL Signaling

CMTL provides the user with a variety of connection techniques which effect the performance, power, number of pins, and termination scheme. The particular transmission line scheme selected should be chosen with careful consideration of the board design and signaling requirements for a given application.

The following contains examples and information for many of the connection techniques for the CMTL I/O. Note that the figures do not differentiate between normal and bidirectional macros for the sake of brevity. Additionally, the tri-state input is not shown on outputs and should be held low for standard macro operation.

2.1.1 Differential with Active Termination

The basic differential with active termination scheme is shown below in Figure 2-3. This scheme maps to the macros listed in Table 2-1. The advantage of this scheme is that external components are not required and the standby current is low.

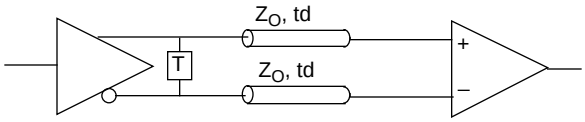


Figure 2-3 Differential CMTL with Active Termination

Table 2-2 CMTL Macros for Figure 2-3

Output Macro	Appropriate Input Macro	System/Core voltages
OD32TCMT	ICMD	5/5 volts
BOD32TCMT	BICMD	5/5 volts Bidi

2.1.2 Differential with Passive Termination

CMTL differential signaling schemes with passive termination are shown in Figures 2-4 and 2-5. These schemes map to the macros listed in Table 2-2.

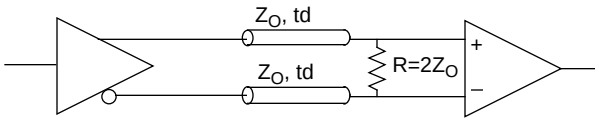


Figure 2-4 Differential CMTL with Passive Termination

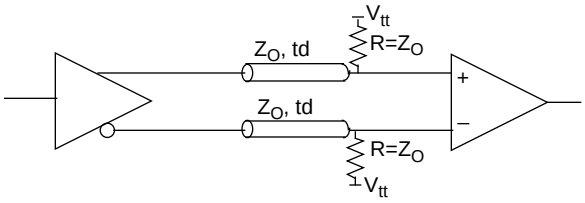


Figure 2-5 Differential CMTL with Passive Termination to V_{tt}

Table 2-3 CMTL Macros for Figures 2-4 and 2-5

Output Macro	Appropriate Input Macro	System/Core voltages
OD32CMT	ICMD	5/5 volts
ODL32CMT	ILCMD	3.3/3.3 volts
ODLX32CMT	ICMD	3.3/5 volts

The resistance R in Figure 2-4 is equal to 2*Z_O for differentially routed lines or Z_O for twisted pair. The passive termination voltage V_{tt} in Figure 2-5 is typically set to $V_{DD}/2 + 0.15V$. However, a capacitor to ground can be connected to V_{tt} instead of using a power supply. The voltage at V_{tt} will automatically charge to the common mode voltage. In both topologies, the termination resistors can be placed at both ends of the lines for multi-point signaling.

3. GTL Characteristics and Operation

Gunning Transceiver Logic (GTL) is a low voltage interface developed to provide the following characteristics:

- Up to 275 MHz clock rates (Worst case, differential point to point)
- 950 mV signal amplitude (Typical)
- Low power and EMI
- Ideal for driving doubly-terminated 50Ω transmission line

GTL was designed for driving a single-ended transmission line system with receivers, drivers and bidirectional macros (see Table 1-1). Differential GTL is offered to provide higher frequencies for applications such as clock line drivers.

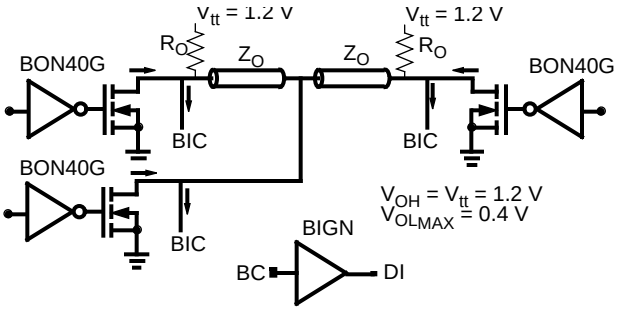
GTL drivers are open drain N-channel devices and the receivers are high gain differential comparators. The inverting

input of single-ended GTL receivers must be connected to a reference voltage pin, INPVR08 (see H4CPlus and H4EPlus Series Design Reference Guides). This pin is required if a GTL input macro is used in the design and should be connected to 0.8 V to maximize the noise margin. The GTL receivers have a DC uncertainty band of ± 50 mV around its reference voltage.

For V_{DD} = 5 V, the GTL driver output sink current at V_{OL} = 0.4 V max for the ON20G is 24 mA while the BON40G is 48 mA. The ON20G macro is used to drive 50Ω single-ended transmission lines with a 50Ω resistor connected at the end of the line between the V_{tt} supply (V_{tt} = 1.2 V) and the signal line. The BON40G is used to drive a bidirectional 50Ω transmission line with a 50Ω resistor connected at each end of the transmission line between the V_{tt} supply and the signal line. BON40G is a single pad, dual site macro. OVSSP is single pad, dual site macro which co-exists on the same sites as the BON40G. OVSSP is a special macro that provides the hi-drive current capability (currents above 24 mA) to the adjacent macro. It must be placed in the numerically lower I/O cell site adjacent to the BON40G macro. By driving terminated transmission lines, high performance buses can be designed by minimizing signal reflections that cause overshoot and undershoot.

3.1 GTL Signaling

Figure 3-1 displays the use of a BON40G bidirectional GTL macro.



GTL Bidirectional receiver macro BIGN is connected to the BIC nodes.

Figure 3-1 GTL Bidirectional Transmission Bus

For $R_O = Z_O$ = 50Ω, the load seen by each driver is about 25Ω with matched termination at both ends of the line minimizing reflections. The voltages are: V_{OLMAX} = 0.4 V; V_{OHMIN} = V_{tt} = 1.2 V; and V_{ref} = 0.8 V. The signal amplitude is close to that of ECL. The function of V_{ref} corresponds to that of V_{BB} in ECL.

3.2 Differential GTL

Differential GTL inputs and outputs are available for both 3 and 5 V operation. The outputs are identical to ON20G GTL macro with 24 mA drive capability. As frequencies exceed 100 MHz, differential GTL can provide reliable operation with excellent noise margin. Several standard products such as Motorola's Fast BiCMOS SRAMs (XCM69G536 and G618) have differential GTL compatible clock inputs for improved bus control. Differential GTL can also be used for driving high speed clock lines with worst case frequencies of up to 250 MHz. A circuit similar to Figure 2-5 can be used for differential drive with V_{TT} = 1.2 V. The output drive is similar to the ON20G of 0.4 V at 24 mA. The lower drive (compared to the ON40G) provides about 2 pF less output capacitance which improves the rising edge delay.

4. PECL Characteristics and Operation

Pseudo ECL (PECL), is ECL operating at V_{CC} = 5.0 V and V_{EE} = 0.0 V. PECL can be used to gain the advantages of higher performance, high common mode noise immunity and signal ground noise immunity to minimize thermal voltage level problems. Transmission lines normally used with PECL are twisted pair, coaxial cables, and controlled impedance printed circuit board interconnects that are terminated with a resistor matching the characteristic impedance of the transmission line. For simplicity, Figures 4-1, 4-3, and 4-4 depict a coaxial cable. Twisted pair with a Z_O equal to twice that of the coax may also be used. An external supply that is normally available in PECL interfaces, $V_t = V_{CC}$ - 2 V, is typically required to connect to the termination resistor. PECL is also capable of driving low impedance (25Ω) lines.

The following are recommendations for PECL and CMTL interconnections:

1 The CMTL (V_{DD}) and PECL (V_{CC}) power supply should be tied to the same supply. Variation between V_{DD} and V_{CC} should be less than ± 0.1V.

2 Terminate the receiver end of the line to the characteristic impedance (Z_O) of the line.

3 Although the pair will function with ±10% supply variation, it is recommended to use ± 5% supplies or better for maximum system performance.

PECL can be used to achieve high bit rates through transmission line impedance matching. In this way, reflections are controlled and signal integrity is maintained. It is expected that most PECL interconnections will use resistor terminated lines to improve interconnection distances and signal purity.

4.1 Standard PECL to H4CPlus and H4EPlus PECL

The basic differential parallel terminated connection scheme is shown in Figure 4-1. This scheme maps to the macros listed in Table 4-1. The resistor R_1 is equal to Z_O. The termination voltage is V_{CC} - 2.0 V.

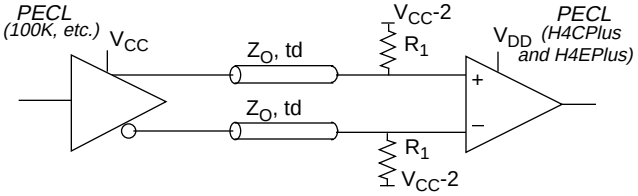


Figure 4-1 Differential PECL with Parallel Termination

Table 4-1 PECL Macros for Figure 4-1

Output Macro	Appropriate Input Macro	System/Core voltages
10KH/100K/ ECLinPS	IPD	5/5 volts
10KH/100K/ ECLinPS	IPXD	5/3.3 volts
10KH/100K/ ECLinPS	ILPD	3.3/3.3 volts

Figure 4-2 shows a basic single-ended termination scheme which is similar to Figure 4-1. A reference voltage can be provided to all single-ended PECL macros through the use of the reference voltage macro INPVR38. A value of V_{DD} - 1.3 V is recommended for PECL signals. This scheme maps to the macros listed in Table 4-2.

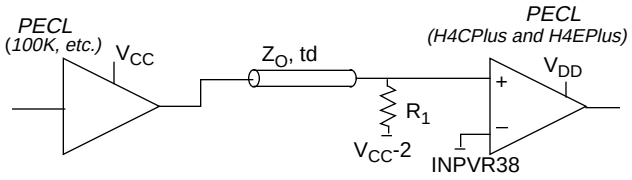


Figure 4-2 Single-Ended PECL Driving H4CPlus and H4EPlus PECL

Table 4-2 PECL Macros for Figure 4-2

Output Macro	Appropriate Input Macro	System/Core voltages
10KH/100K/ ECLinPS	IPN	5/5 volts
10KH/100K/ ECLinPS	IPXN	5/3.3 volts
10KH/100K/ ECLinPS	ILPN	3.3/3.3 volts

4.2 Differential CMTL Driving Standard PECL

Table 4-3 contains characteristics for some of the configurations discussed below. It is available to adapt the differential topologies of Figures 2-3 to 2-5 for CMTL or GTL driving PECL and LVDS applications. CMTL outputs configured as differential active termination, Figure 2-3, and differential passive termination, Figure 2-4, may be used to drive 10H/10K/100K family ECL inputs only (such as 10H116). The ECL inputs should have a common mode range like the 10H116 (no input followers), and power supply differences between chips should be 5% or less. Section 8.3 describes a test circuit and results for a CMTL output driving an ECL input with active termination.

Passive termination to V_{CC} - 2.0 V (Figure 4-3) may be used to drive the 10H/10K/100K family as well as differential input ECLinPS Lite devices (such as 100EL16). ECLinPS 10E/100E series devices can be driven but may exhibit CMR problems over worst case levels.

The reason for the various methods of driving PECL is that the input common mode range for the various ECL families are different due to circuit designs. Note that the common mode range is defined as the voltage range of the crossing voltage of the differential signals. Additionally, the ECL specifications have a CMR that is 100 mV higher than the crossing point. The ECL specifications define the common mode range referenced to the most positive side of the differential signal. The 10H116 has no input clamping circuitry so that the worst case common mode voltage must be greater than 2.1 volts above ground (V_{EE}). The10E116/100E116 in the ECLinPS family has a clamp circuitry referenced to V_{CC} that enables the inputs to be left floating. This reduces the common mode voltage requirement to greater than 2.65 V at V_{CC} = 4.75 V and 3.15 V at V_{CC} = 5.25 V. The 10EL16/100EL16 in the ECLinPS Lite family has a clamp circuitry that is referenced to V_{EE} that increases the worst case common mode voltage requirement to greater than 2.4 V above ground (V_{EE}) that also enables the inputs to be left floating.

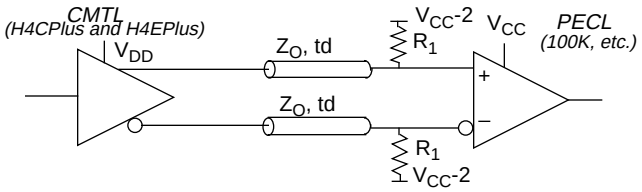


Figure 4-3 Differential CMTL Driving PECL with Parallel Termination to V_{CC}-2

In order to drive 10E/100E series devices (such as 100E116), the scheme in Figure 4-4 should be employed. For 50Ω Coax (or 100Ω twisted pair), R_1 = 109Ω and R_2 = 185Ω. An advantage of this method is that an extra power supply is not required.

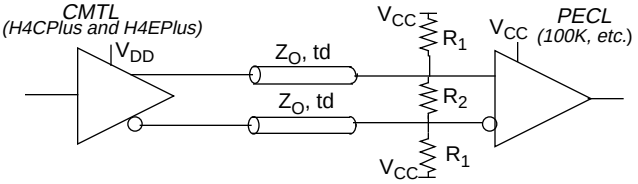


Figure 4-4 Differential CMTL Driving PECL with Parallel Termination to V_{CC}

4.3 Single-Ended CMTL to Standard PECL

A single-ended CMTL (O32CM) to PECL input can be realized (for V_{DD} = 5 V) as in Figure 4-5. The resistor values should have a parallel value equal to Z_O. For 50Ω lines, R_1 = 61Ω and R_2 = 278Ω. For 100Ω lines, R_1 = 122Ω and R_2 = 556Ω.

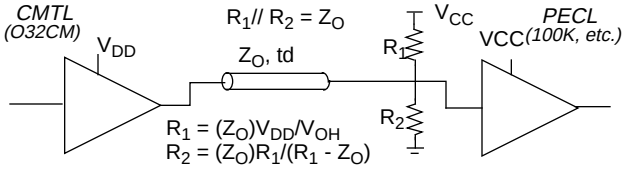


Figure 4-5 Single-Ended CMTL Driving PECL

For point to point applications, the resistor can use the values for 100Ω termination to reduce power even if Z_O is 50Ω. The reason is that the CMTL output absorbs most of the reflection due to any mismatch with the output acting like a series terminated line.

Table 4-3 CMTL and GTL Driving PECL and LVDS (50Ω Termination)

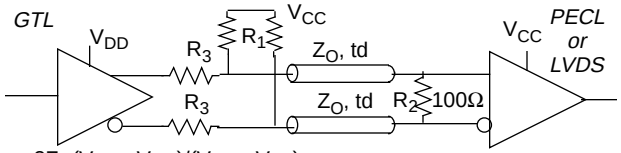
Output Configuration	V_{DD}	V_{OH}	V_{OL}	V_{CM}[1]	I_{OUT_1}[2]	I_{OUT_0}[3]	$P_{RL\ DC}$[4]	$P_{ext\ RL\_1}$[5]	$P_{ext\ RL\_0}$[6]
	V	V	V	V	mA	mA	mW	mW	mW
Figure 4-3 CMTL to PECL Differential	4.75	3.20	2.03	2.62	9.1	14.4	43.2	14.4	14.4
	5.0	3.47	2.11	2.79	9.4	17.6	51.8	20.0	20.0
	5.25	3.69	2.25	2.97	8.9	20.0	58.9	24.0	24.0
Figure 4-4 CMTL to PECL Differential	4.75	3.93	2.54	3.23	~0	27.8	70.6	61.6	61.6
	5.0	4.10	2.57	3.33	~0	30.6	78.5	74.3	74.3
	5.25	4.29	2.67	3.48	~0	32.4	86.6	83.7	83.7
Figure 4-5 CMTL to PECL Single-Ended	4.75	3.90	2.52	3.21	~0	27.5	69.2	66.6	104.3
	5.0	4.10	2.53	3.32	~0	31.4	79.4	73.7	123.1
	5.25	4.3	2.67	3.49	~0	32.6	87.2	81.3	134.4
Figure 5-1 GTL to PECL Differential	4.75	3.77	3.09	3.43	0	18.4	3.3	84.3	84.3
	5.0	3.97	3.25	3.61	0	19.4	3.6	93.4	93.4
	5.25	4.17	3.41	3.79	0	20.4	3.9	103.1	103.4
Figure 5-1 GTL to PECL Differential	3.14	2.04	1.61	1.82	0	10.3	1.2	31.3	31.3
	3.3	2.14	1.69	1.92	0	10.8	1.3	34.5	34.5
	3.46	2.25	1.77	2.01	0	11.4	1.5	37.8	37.8
Figure 5-1 GTL to LVDS Differential	4.75	1.29	0.96	1.13	0	6.8	0.45	32.0	32.0
	5.0	1.36	1.01	1.18	0	7.2	0.50	35.5	35.5
	5.25	1.42	1.06	1.24	0	7.6	0.54	39.2	39.2
Figure 5-1 GTL to LVDS Differential	3.14	1.29	0.96	1.13	0	7.2	0.58	22.0	22.0
	3.3	1.35	1.00	1.18	0	7.6	0.63	24.3	24.3
	3.46	1.42	1.05	1.24	0	7.9	0.68	26.7	26.7
Figure 5-2 GTL to PECL Single-Ended	4.75	3.97	3.12	3.54	0	16.9	2.8	61.8	126.1
	5.0	4.18	3.29	3.74	0	17.8	3.0	68.5	139.8
	5.25	4.39	3.45	3.92	0	18.7	3.4	75.5	154.0
Figure 5-2 GTL to PECL Single-Ended	3.14	2.27	1.41	1.84	0	17.2	3.3	39.8	75.3
	3.3	2.38	1.48	1.93	0	18.1	3.6	43.9	83.4
	3.46	2.50	1.55	2.02	0	19.0	3.9	48.3	91.8

1. Common mode voltage of output; 2. Total driver current for output high; 3. Total driver current for output low; 4. Driver power when output is low; 5. External resistor load power for output high; 6. External resistor load power for output low.

5. GTL Driving PECL and Interface to LVDS

5.1 Differential GTL Interface to PECL and LVDS

Figure 5-1 shows the design using GTL to interface to either PECL or Low Voltage Differential Signals (LVDS). Table 5-1 contains resistor values for a $Z_o = 50\Omega$.



$R_1 = 2Z_O(V_{CC} - V_{OH})/(V_{OH} - V_{OL})$
$R_2 = 2Z_O$
$R_3 = - R_O + R_1V_{OL}/(2V_{CC} - V_{OH} - V_{OL})$

Note: For twisted pair interconnect, Z_o is 1/2 the characteristic Impedance

Figure 5-1 Differential GTL Driving PECL or LVDS with Parallel Termination

The specifications for LVDS are defined in the IEEE standard 1596.3. LVDS is designed for high speed, low power, point to point applications. It has a smaller voltage swing of 250 to 400 mV when compared to PECL (800 mV). Also, LVDS outputs switch at a crossing voltage of 1.2 V referenced to V_{SS} compared to PECL where the crossing voltage is -1.3 V referenced to V_{DD}.

Table 5-1 Resistor Values for Figure 5-1

Type	V_{CC}	R_1	R_2	R_3
PECL	5	143	100	158
	3.3	255	100	145
LVDS	5	1060	100	131
	3.3	562	100	122

Table 4-3 shows the typical voltage levels, current, and power for differential GTL driving PECL and LVDS over a +/- 5% power supply tolerance. One advantage of this approach is that the worst case values are process independent and are practically the same as the typical values. The V_{OH} and V_{OL} levels are basically dependent on the values of the resistors. The output impedance (R_0) of the differential GTL is typically 9.6 Ω (16.6 Ω worst case) at V_{DD} = 5 V and 11.0 Ω (20.0 Ω worst case) at V_{DD} = 3.3 V. Since the voltage levels at the receiver are mainly dependent on the sum of R_0 plus R_3, R_0 has a very small effect since it is much smaller than R_3. For example, the typical V_{OH} and V_{OL} is 2.14 V and 1.69 V respectively

at V_{DD} = 3.3 V having a voltage swing of 450 mV. Using the worst case R_0, the V_{OH} and V_{OL} levels rise slightly to 2.18 V and 1.74 V resulting in a voltage swing of 440 mV. The typical value of R_0 was used for values in the table since the current and power are larger than the worst case value.

Another advantage of the design is that the power dissipation of the GTL macros on the H4CP or H4EP array is very small, only 1.2 to 3.9 mW when driving PECL and 0.45 to 0.68 mW when driving LVDS. The power dissipation of the resistors is much larger, but at least this can be managed on the system level. The lower power on the chip is important for maintaining a low cost packaging and power management solution.

The voltage swing for driving PECL at V_{DD} = 5 V is 720 mV compared to 450 mV at V_{DD} = 3.3 V. The reason for the larger swing at 5 V (which also increases the power) was to reduce the value of R_3 which improves the rise time as well as the operating frequency. The value of R_3 dropped from a value of 310 Ω to 158 Ω for increasing the swing to 720 mV. The rise time of the output is affected by the RC time constant consisting of the output capacitance at the GTL output (~6 pf) and the resistance of R_3 plus the parallel resistance combination of R_1 and one-half of R_2. The resulting rise time (20 to 80%) is about 1.8 ns versus 0.6 ns fall time for both V_{DD} = 5 V and 3.3 V. This should be acceptable for driving clock lines at 225 MHz worst case (see section 8.). If clock frequencies are less than 125 MHz, the voltage swing can be reduced to 450 mV for V_{DD} = 5 V.

Note that the resistors, R_1, are placed at the driver side for GTL driving PECL while they are placed at the receiver side for CMTL driving PECL. This appears to optimize the two circuits for performance versus speed. For instance, if the R_1 resistors were placed at the receiver for the GTL to PECL driver, then the voltage swing would have to be 970 mV instead of 720 mV for V_{DD} = 5 V to achieve the same power dissipation and speed.

The standard logic differential PECL receiver (ECLinPS) is specified with a minimum input AC voltage swing of 150 mVpp so that a 450 mV output signal produces a 300 mV DC noise margin and about 150 mV AC noise margin at the worst case frequency (see Table 8-3).

The LVDS voltage swing is designed for a 350 mVpp using resistor values shown for the differential GTL driver circuit in Figure 5-1. The V_{OH} and V_{OL} levels meet the LVDS specification of 1475 mV max and 1025 mV min. The output offset voltage ranges from 1120 mV min to 1285 mV max for a +/- 5% V_{DD} tolerance which is slightly larger than the specification by 5 to 10 mV. A +/- 4.5% V_{DD} tolerance should meet the V_{os} specification although it should not be that importance to the system designer since the receiver has an input voltage range of 0 to 2 V. The LVDS receiver is specified with a minimum input voltage of 100 mVpp so that the DC noise margin is 150 mV and the AC noise margin is about 100 mV.

The GTL differential receiver can also be used to receive LVDS signals. The input voltage and common mode voltage range for the GTL receiver is shown in section 6.3. The main advantage of using GTL to drive or receive LVDS signals is that LVDS is an IEEE standard which provides the capability to communicate with LVDS from other arrays. Presently, LVDS macros are difficult to implement directly in H4CP and H4EP using the components in the present I/O cell. The M5C arrays do offer LVDS macros.

5.2 Single-Ended GTL to Standard PECL

By using GTL to interface to PECL, as shown in Figure 5-2, lower power on the H4CP or H4EP array can be achieved compared to using CMTL (Figure 4-5). Also, only one output cell is required using the ON20G.

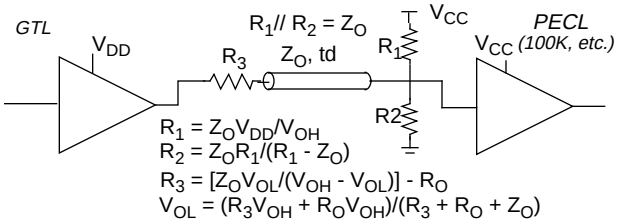


Figure 5-2 Single-Ended GTL Driving PECL

Resistors R_1 and R_2 are used to terminate the transmission line with the thevenin equivalent combination equal to Z_0 at a voltage equal to the PECL V_{OH}. An extra resistor, R_3, is required to set the V_{OL} level. The resistor values are R_1 = 60Ω, R_2 = 305Ω, and R_3 = 175Ω for Z_0 = 50Ω and V_{DD} = 5 V. For V_{DD} = 3.3 V, R_1 = 69Ω, R_2 = 179Ω, and R_3 = 71Ω.

Table 4-3 shows the typical voltage levels, current, and power for the single-ended GTL driving PECL over a +/- 5% power supply tolerance. Similar to differential GTL driving PECL, this design also has V_{OH} and V_{OL} levels that are process independent due to the low GTL output impedance compared to R_3. The typical value of R_0 was used for values in the table since the current and power are larger when compared to using the maximum value of R_0.

When interfacing to 3.3 V PECL, the voltage levels show that V_{OH} falls within the 100E specification while V_{OL} is about 100 mV lower at 1.91 V below V_{DD} at V_{DD} = 3.46 V. This should not present a problem since it provides a slightly larger noise margin. When interfacing to 5 V PECL, the voltage levels show that the voltage swing has been raised by about 100 mV so that V_{OL} falls within the 100E specification while V_{OH} is about 100 mV higher at V_{DD} = 4.75 V. Again, this will not present a problem since it causes a slightly higher noise margin. The reason for the tight control of the voltage levels for the 100E family is to provide tight distribution using voltage compensation which helps to achieve a more controlled test environment. The reason for designing the voltage levels 100 mV higher at V_{DD} = 5 V is to reduce the amount of time it takes to reach the V_{bb} threshold due the slower rise time 2.5 ns (20 to 80%) compared to the fall time (0.7 ns). Raising the voltage improves the rising edge delay and provides better performance. For V_{DD} = 3.3 V, the rise time was 0.9 ns and the fall time was 1 ns. See section 8. on the worst case frequency of operation.

A V_{DD} - 2 V supply is available in many PECL systems in order to lower the system power dissipation. For these systems, a faster rise time can be achieved for a V_{DD} = 5 V, by slightly changing the circuit shown in Figure 5-2. First, the

ground connection going to resistor R_2 is instead connected to the V_{DD} - 2 V supply and resistor R_1 is moved to the driving end of the transmission line. The resistor values are R_1 = 43Ω, R_2 = 50Ω, and R_3 = 73Ω. Due to the higher driver sink current of 36 mA, the driver needs to be an ON40G (2 output cells) instead of the ON20G. The output capacitance of the ON40G (~8 pf) is about 2 pf larger than the ON20G. However, the rise time is still reduced to about 1.6 ns from 2.5 ns. Another advantage of this circuit is that the impedance looking into the driver side from the transmission line is almost matched which reduces any noise from crosstalk or reflections.

6. GTL Measurements and Specifications

6.1 GTL Output Voltage and Current Sinking

The GTL drivers were tested for output load characteristics. The results showed that the output impedance was very linear over a wide range of current loading. The BON40G operating at V_{DD} = 5 V was capable of sinking 38.4 mA at a V_{OL} = 0.2V which is an output impedance of 5.2Ω. When the output of the BON40G was forced to a V_{OL} = 0.5V, the current sinking was 93.7 mA for an average output impedance of 5.3Ω. There was very little change with a +/-10% V_{DD} variation.

The output impedance of the BONL40G at V_{DD} = 3.3 V was also very linear over a wide range of current loading. The BONL40G was capable of sinking 33.83 mA at a V_{OL} = 0.2V which is an output impedance of 5.9Ω. When the output was forced to a V_{OL} = 0.5V, the current sinking was 80.78 mA for an average output impedance of 6.2Ω. For V_{OL} = 0.2 V, the output impedance is 6.2Ω at V_{DD} = 3.0 V and 5.7Ω at V_{DD} = 3.6 V.

The output impedance of the ON20G and OD20G at V_{DD} = 5.0 V was also very linear over a wide range of current loading. They were capable of sinking 20.86 mA at a V_{OL} = 0.2V which is an output impedance of 9.6Ω. When the output was forced to a V_{OL} = 0.5V, the current sinking was 51.05 mA for an average output impedance of 9.8Ω. For V_{OL} = 0.2 V, the output impedance is 9.8Ω at V_{DD} = 4.5 V and 9.4Ω at V_{DD} = 5.5 V.

The output impedance of the ONL20G and ODL20G at V_{DD} = 3.3 V was also very linear over a wide range of current loading. They were capable of sinking 18.26 mA at a V_{OL} = 0.2 V which is an output impedance of 11.0Ω. When the output was forced to a V_{OL} = 0.5 V, the current sinking was 42.84 mA for an average output impedance of 11.7Ω. For V_{OL} = 0.2 V, the output impedance is 11.6Ω at V_{DD} = 3.0 V and 10.7Ω at V_{DD} = 3.6 V.

This information can be used to determine transmission line reflections that cause overshoot and undershoot. Equations 7-3 and 7-4 along with a graphical solution are described in section 7.2.

6.2 GTL Operating Frequencies

The typical output voltage amplitude was measured over the frequency and V_{DD} range using the test circuit shown in Figure A-4. Also, the minimum input voltage amplitude required for the IGN to drive a divide by 8 counter was measured using the test circuit shown in Figure A-5. The results of these measurements are plotted in Figure 6-1 for V_{DD} = 4.5 V and 3.0 V. At these V_{DD}'s, a minimum value is produced for 5.0 V or 3.3V operation. The two independent measurements indicate that the typical frequency of operation is greater than 425 MHz at V_{DD} = 4.5 V and 300 MHz at V_{DD} = 3 V. When the outputs of circuit Figure A-4 were used to drive the circuit inputs of Figure A-5 with 12 inches of 50Ω coax, the typical frequencies were slightly lower, 378 MHz at V_{DD} = 4.5 V and 252 MHz at V_{DD} = 3.0 V. The main reason for the differences is that the output voltage is a peak to peak measurement that has logic 1 and logic 0 midpoint that is not centered around the input reference voltage. The midpoint voltage for the BON40G at V_{DD} = 4.5V driving 25Ω measured 0.82 V at 50 MHz rising to 0.9 V at 300 MHz.

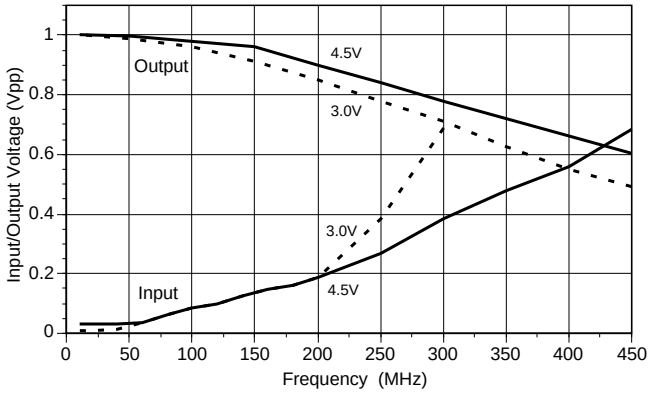


Figure 6-1 Typical GTL Output and GTL Minimum Input Amplitude versus Frequency for Single-Ended Macros

Table 6-1 shows the worst case operating frequencies as well as the minimum I/O voltages when using GTL outputs to drive a terminated 50Ω line or a doubly terminated 25Ω bus.

Table 6-1 GTL Operating Limits

Operating Conditions		Tj = -40 to 85° C			
		Min. I/O Voltage		W.C. Frequency	
		Vin mVpp	Vout mVpp	Clock MHz	Data Mb/s
Single-Ended	3.14 - 3.6 V	400	600	165	210
	4.5 - 5.5 V	400	600	210	265
Differential	3.14 - 3.6 V	300	500	200	275
	4.5 - 5.5V	300	500	275	350

Operating limits and voltages are for the ON20G with a 50Ω load and the ON40G with a 25Ω or 50Ω load.

These values were calculated using conservative K factors to modify the typical lab results in order to compensate for process, temperature, V_{DD}, and noise margins. The input and output voltages were first modified to agree with typical lab operating frequencies as discussed above. Then the output voltage was reduced by the worst of either a 30% reduction at the measured frequency or the voltage at 1.3 times the frequency while the input voltage required by the receiver was increased by 50%. It should be noted that V_{out} in the table has been modified to be smaller than the measured peak to peak value in order to account for the smallest voltage that is measured across the receiver when the output is a logic 1 or a logic 0 state.

The worst case noise margin can be calculated from Table 6-1 by subtracting the worst case input voltage swing per pin (V_{in}) of the receiver from the worst case output voltage per pin (V_{out}) of the driver. For a V_{DD} = 5 V or 3.3 V ±10%, the worst case noise margin at the worst case frequency is 200 mV.

It is recommended that differential lines be used whenever possible and especially for clock signals. Differential drive reduces simultaneous switching current, reduces ground bounce, and provides superior noise margin through common mode noise rejection. It is still very important to separate sensitive differential clock inputs so they are not adjacent to fast switching outputs. Crosstalk noise can be a problem when traces on a PC board are adjacent for sensitive inputs. Some Fast BiCMOS Static RAMs use a differential GTL signal for the clock while the data and address lines use single-ended GTL to reduce the number of I/O pins. From Table 6-1 for V_{DD} = 5 V, the differential clock can operate at 275 MHz, while the single-ended lines can operate at 265 Mb/s.

6.3 GTL Common Mode Input Range

Measurements of the common mode range input versus amplitude are plotted for the IGN and ILGN input macro. The test circuit is given in Figure A-5. Figures 6-2 through 6-5 are graphs showing the common mode range for several frequencies at VDD ±10% at 3.3 and 5.0V. The junction temperature is 25°C while the process is typical. These plots specify the mid-point of the voltage amplitude required at the reference input pin (INPVR08) for operation at the given frequency and supply voltage. For example, for 50 MHz operation, Figure 6-2 suggests that an input voltage (X-axis) of 300 mVpp, centered around the reference voltage, at a supply voltage of 4.5 V, would require the amplitude mid-point to be between -0.17 V to 3.41 V. Note that for differential GTL input macros, the required input voltage is 1/2 of the amount shown in Figures 6-2 to 6-5 for single-ended GTL macros. The reason is that for differential signals, only one-half the voltage is needed at each input to achieve the full voltage required on only one input.

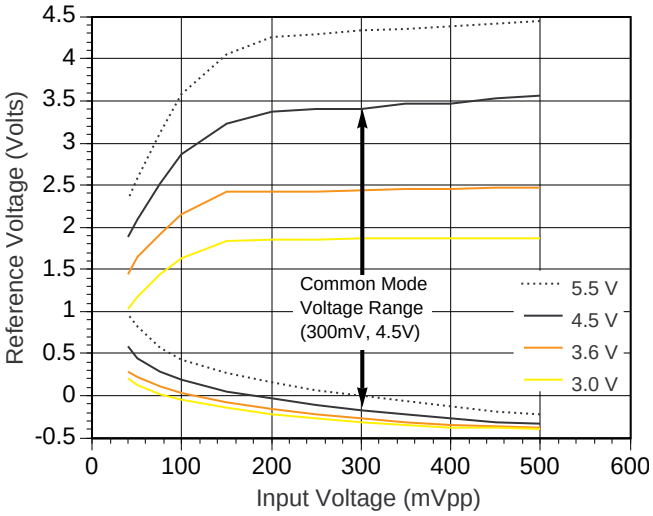


Figure 6-2 IGN/ILGN Operating Common Mode Range for V_{DD} Voltages at 50 MHz

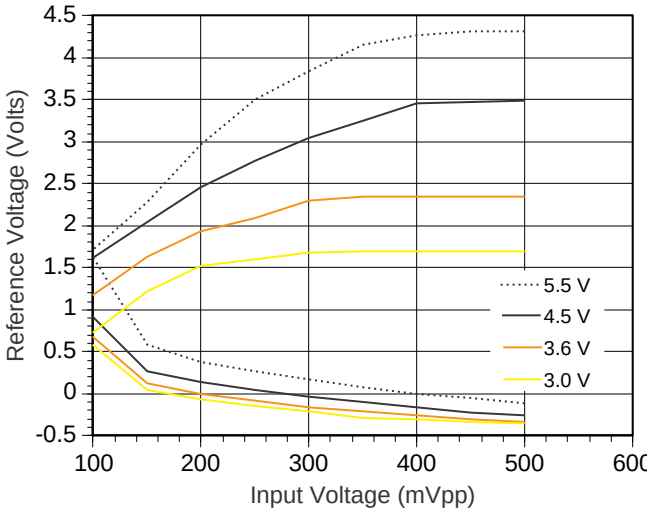


Figure 6-3 IGN/ILGN Operating Common Mode Range for V_{DD} Voltages at 120 MHz

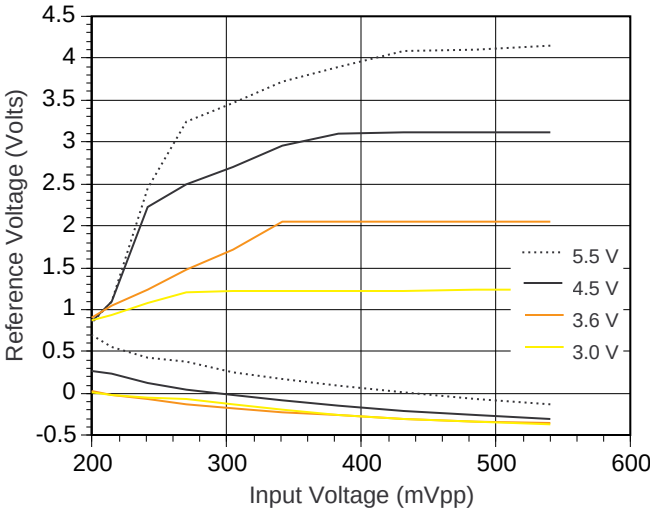


Figure 6-4 IGN/ILGN Operating Common Mode Range for V_{DD} Voltages at 200 MHz

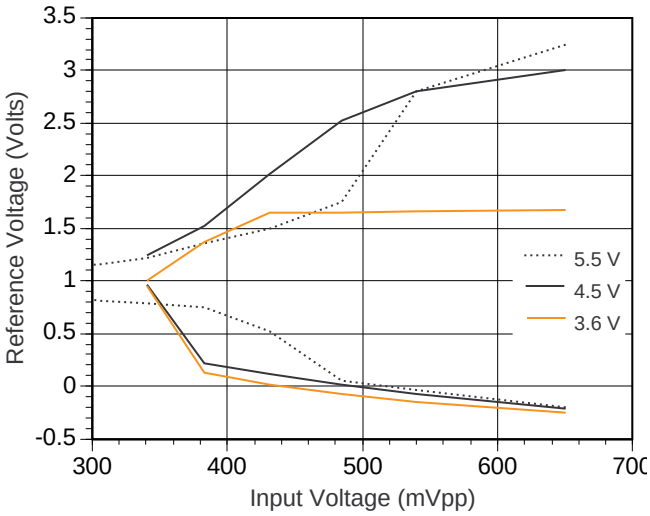


Figure 6-5 IGN/ILGN Operating Common Mode Range for V_{DD} Voltages at 300 MHz

7. CMTL Measurements and Specifications

7.1 CMTL Output Impedance and Voltages

It is important to understand the effects of output impedance and termination when driving transmission lines. Reflections on a line are caused by a mismatch in impedance between the line and the load. If all the power delivered to the line is absorbed by the load then there will be no reflected power back at the source. This can be achieved by matching the load with the characteristic impedance of the transmission line. CMTL outputs that have the active termination (Figure 2-1) can be used to drive non-terminated lines. The active termination provides a load at the CMTL output to reduce that voltage swing for open lines and keep them from floating to V_{DD} or to ground. The output impedance for both the active and nonactive outputs, when driving 50Ω transmission lines or a 100Ω twisted pair, was calculated first by measuring the peak to peak output voltage at 20 MHz with a 200Ω load and then a 100Ω load resistor across the outputs. The difference in voltage was divided by the difference in current to determine the output impedance. The impedance for both the rising and falling outputs was calculated by measuring the DC voltage change for a 1 mA delta over a wide range in load currents. Figures 7-1 to 7-3 contain the calculated output impedance versus current as well as curves for determining the load current versus V_{DD} for a given transmission line impedance. These figures can be then be used with Figures 7-4 to 7-6 to determine the output voltages and the common mode offset voltage. As can be seen, the output impedance decreases with an increase in supply voltage or an increase in load current due to lower impedance lines.

As an example for using these figures, assume that an OD32CMT is driving two pc traces, each with a characteristic impedance of 50Ω. A 100Ω resistance (or two 50Ω resistors with a capacitor to ground between the resistors) is placed across the two lines near the receiver, ICMD, to match the lines. Since the impedance of each line is 50Ω, the load current is determined from Figure 7-1. The current is 12.5 mA for a V_{DD} = 5.0 V. The output impedance falling is 36Ω and the output impedance rising is 29Ω for an average of 32.5Ω

The output voltage can be read from Figure 7-4. For 12.5 mA, the V_{OH} is 3.28 V, V_{OL} is 2.03 V and the common mode offset voltage is 2.65 V. Similarly, the current is 10 mA and 15.2 mA for V_{DD} equal to 4.5 V and 5.5 V respectively. Then the output impedances and the output voltages are read from the graphs.

For a bidirectional bus or if the driver was driving more than one receiver from the center of the transmission line, then both ends of the transmission line must be terminated with 100Ω at each end. The equivalent load being driven would be 25Ω. From Figure 7-1, the load current is 18 mA for a V_{DD} = 5.0 V. The output impedance falling is 31Ω and the output impedance rising is 26Ω for an average of 28.5Ω. The output voltage can be read from Figure 7-4. For 18 mA, the V_{OH} is 3.13 V, V_{OL} is 2.23 V and the common mode offset voltage is 2.68 V. The current, output impedances and output voltages can be found for the other V_{DD} voltages. Also, these values can be determined for other load conditions.

The single-ended CMTL output macro called O32CM that is intended to be used to drive standard single-ended PECL gates as previously shown in Figure 4-5. Since the output circuit of O32CM is the same as OD32CMT, Figures 7-1 to 7-4 should also be used for the O32CM macro.

For the CMTL output with the active network (OD32TCMT) Figure 7-2 shows the output impedance and load current while Figure 7-5 shows the output levels. The active network starts to draw current when the voltage across the CMTL outputs is about 1 V (threshold voltage of N-channel device). The current drawn through the active network with no load can be calculated by measuring the V_{OH} levels from Figure 7-5 for a current of 0 mA, then using the V_{OH} values with Figure 7-4 to find the current in the active network. For instance, from Figure 7-5, V_{OH} = 3.56 V for 0 mA (no load) and V_{DD} = 5 V. The current in the active network is then found from Figure 7-4 to be about 4.2 mA. The output impedance for no load is found from Figure 7-2 to be 32Ω for the falling edge and 24Ω for the rising edge for an average of 28Ω. Note that the active network clamps the differential output at about 52Ω when reflections are returned to the driver that turns off the CMTL output causing a negative current in the driver.

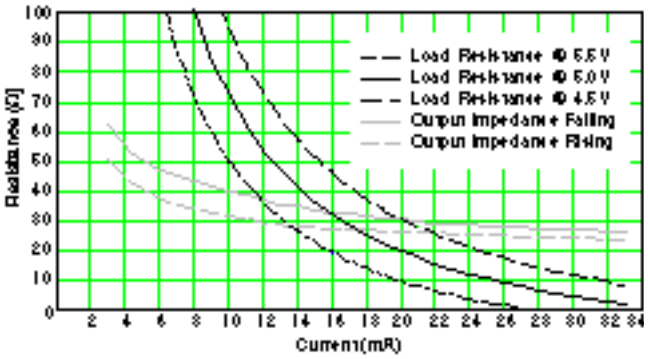


Figure 7-1 OD32CMT Output Impedance

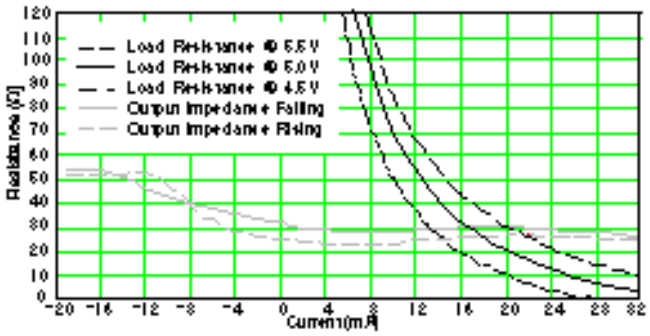


Figure 7-2 OD32TCMT Output Impedance

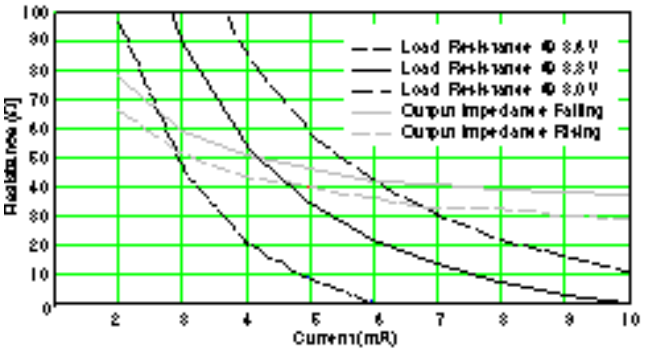


Figure 7-3 ODL32CMT Output Impedance

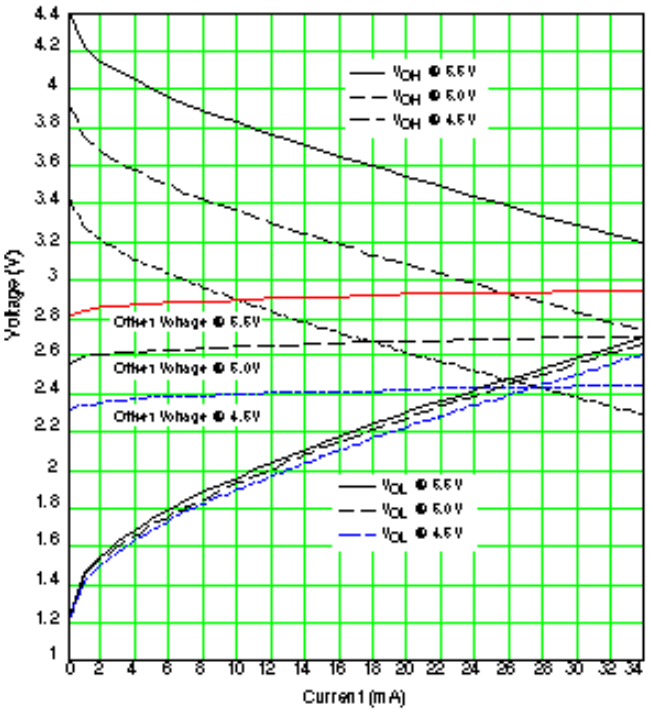


Figure 7-4 OD32CMT Output Levels

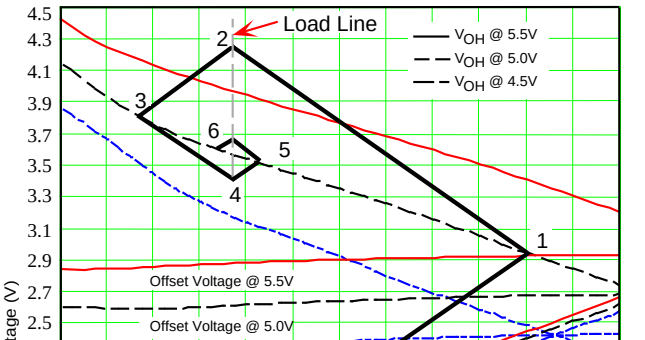


Figure 7-5 OD32TCMT Output Levels with Bergeron Graphical Techniques

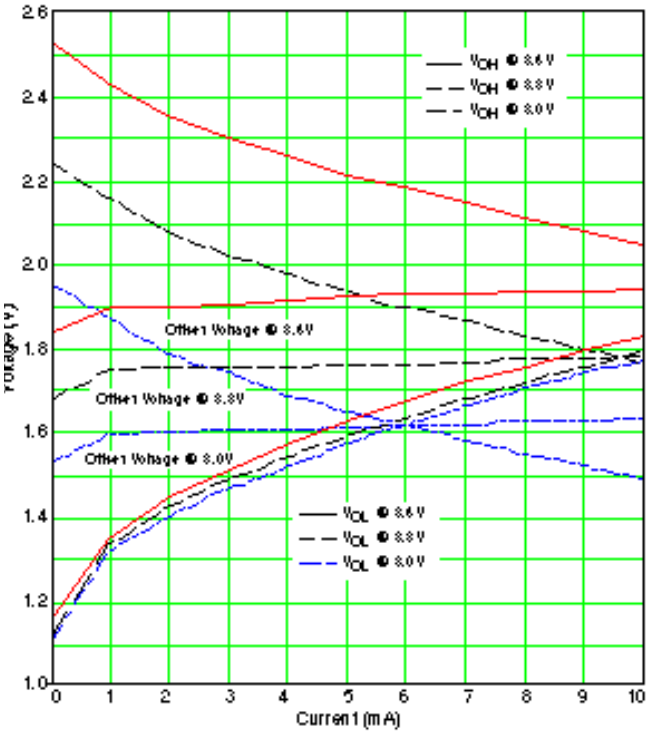


Figure 7-6 ODL32CMT Output Levels

7.2 Transmission Line Reflections

An open line can be driven by the OD32TCMT since the undershoot caused by the mismatch in impedance for an open line can be held to less than 15% of the logic swing if the signal pulse width (PW) is greater than four times the line delay, (Tpd), or PW ≥ 4Tpd. If the PW is less than 4 times the line delay, the overshoot and undershoot can double from the calculated values (see equations below) for certain line lengths due to standing waves. The voltage doubles when it arrives at the load for an open line causing overshoot. The undershoot is caused by the returning reflection from the mismatch in source impedance. From equation 94 and 102 in reference 2, the maximum value of undershoot (US_{max}) and overshoot (OS_{max}) for fast rise and fall times when driving an open line can be found from equations (7-1) and (7-2):

$$US_{max} = 100 \cdot \left[1 - \frac{2 \cdot Z_0}{Z_0 + R_0} \cdot (1 + \rho_s)\right] \quad (7\text{-}1)$$

$$OS_{max} = 100 \cdot \left(\frac{2 \cdot Z_0}{Z_0 + R_0} - 1\right) \quad (7\text{-}2)$$

where:

$$\rho_s = \frac{R_0 - Z_0}{R_0 + Z_0}$$

For Z_O = 50, the average output impedance can be found from Figure 7-2 which is $R_{O(avg)}$= 27.5Ω. The average output impedance can be used when the output is driven differentially. This results in US_{max} = 8.4% and OS_{max} = 29.0%. The overshoot enhances the noise margin while the undershoot subtracts from the noise margin.

The undershoot and overshoot equations for driving a transmission line were derived for a load (RL) that doesn't match the characteristic impedance of the line. The equations are:

$$US_{max} = 100 \cdot (1 - \left(\frac{2 \cdot RL \cdot (V_{OHT} - V_{OLT})}{(V_{OH} - V_{OL}) \cdot (Z_0 + RL)^2} \times [(Z_0 + RL) + \rho_s \cdot (RL - Z_0)]\right)) \quad (7\text{-}3)$$

$$OS_{max} = 100 \cdot \left[\frac{(V_{OHT} - V_{OLT}) \cdot (1 + \rho_L)}{V_{OH} - V_{OL}} - 1\right] \quad (7\text{-}4)$$

where:

$$\rho_L = \frac{RL - Z_0}{Z_0 + RL}$$

V_{OH} and V_{OL} are the DC voltage levels that can be found by using Figures 7-1 to 7-3 to find the load current for the load resistor RL and then finding the voltage levels from Figures 7-4 to 7-6. The V_{OHT} and V_{OLT} terms are the output voltage levels when the transmission line is properly terminated. Again, Figures 7-1 to 7-3 and Figures 7-4 to 7-6, can be used to find the levels. These equations are useful when a load resistor is used that is larger than the line impedance in order to save power while reducing the overshoot and undershoot.

7.2.1 Graphical Techniques

There is another very accurate way to find the voltages and currents at both the driver and the receiver for long transmission lines [Tr<2Tpd(line)]. The method uses a simple graphical technique, called a Bergeron diagram in reference 3, that is very useful for non-linear outputs. The method is illustrated in Figure 7-5 for the OD32TCMT driving an open line for V_{DD}= 5 V. The starting point is a graph of the voltage and current characteristics of the driver. First, two lines are drawn from the quiescent voltage and current state that the output is switching from. For the output in the logic 0 state, this is point 0 on the graph at 0 mA and a voltage of 1.67 V. The first line drawn is the load line which is drawn at point 0 with a slope of R_L, where R_L is the load resistance at the end of the line. Since R_L is a high impedance for an open line, the load line is infinity which is represented by a vertical line at 0 mA. [Note that if the load was 100 ohms (200 ohms across the differential outputs), the current would be 8 mA using Figure 7-2 and then using Figure 7-5, the voltage would be 1.9 V for a logic 0 and 3.4 V for a logic 1. Since the current flow of a logic 0 and a logic 1 are in opposite directions, point 0 would have to start at -8 mA and 1.9 V on the graph of Figure 7-5.] Note that the R_L load line connects the output characteristic curve at the final steady state voltage. For this example, the steady state logic 1 voltage is 3.55V at 0 mA. The second line that is drawn at point 0 is a load line of the characteristic impedance, Z_O, of the transmission line with a slope = Z_O. The intersection of this line with the logic 1 output curve is labeled point 1 and it represents the voltage and current being sourced at the driver after the output switches from a logic 0 to a logic 1. This difference in the voltage and current from point 0 to 1 is the amount of initial voltage and current that travels down the transmission line to point 2 at the receiver.

The signal then travels back and forth between the driver and receiver with the even numbers on the graph representing the voltage and current being sourced at the receiver and the odd numbers representing the voltage and current being sourced at the driver starting at point 1. The procedure continues by drawing a line with a slope = $-Z_O$ at point 1 until it intersects the load line which is labeled point 2. For this example, point 2 represents an overshoot voltage since it exceeds the steady state voltage. From point 2 a line is drawn with a slope = $+Z_O$ until it intersects the logic 1 output curve which is labeled point 3. From point 3 a line is drawn with a slope = $-Z_O$ until it intersects the load line which is labeled point 4. For this example, point 4 represents an undershoot voltage since it is smaller than the steady state voltage. This procedure can be continued by drawing lines with alternating slopes of $+Z_O$ and then - Z_O. Note that the current at the driver at point 3 is at -8 mA compared to the +25 mA at point 1. The active termination is sinking the negative current that is caused by the positive overshoot reflection returning from the open line at the receiver. The steady state voltage swing is 3.56V - 1.65V = 1.91V. The overshoot voltage is 4.2V - 3.56V = 0.64V or 33.5% overshoot (0.64/1.91). The undershoot voltage is 3.56V - 3.4V = 0.16V or 8.4%. This compares to the previous calculations using the equations of 29% overshoot and 8.4% undershoot.

The Bergeron method can also be used to find the logic 0 voltage for the single-ended CMTL driving PECL shown in Figure 4-5. For instance, if the Thevenin equivalent load was 50Ω at 4.1V for a V_{DD} = 5 V, then a load line would be drawn on Figure 7-4 with a slope of -50Ω starting at 4.1V until it in-

tersects the logic 0 output curve. This results in a logic 0 of 2.55 V sinking a current of 30 mA. Table 4-3 used equations to derive the values shown in the table and it shows a logic 0 of 2.53 V sinking a current of 31.4 mA.

7.3 CMTL Operating Frequencies

The typical output voltage amplitude was measured over the frequency and V_{DD} range using the test circuit shown in Figure A-1. Also, the minimum input voltage amplitude required for the ICMD to drive a divide by 8 counter was measured using the test circuit shown in Figure A-2. The results of these measurements are plotted in Figures 7-7 to 7-8 for V_{DD} = 5.0 V ±10% and 3.3 V ±10%. The two independent measurements indicate that the typical frequency of operation is greater than 350 MHz. However, when the outputs of circuit Figure A-1 are used to drive the circuit inputs of Figure A-2 with 12 inches of 50Ω coax, the typical frequency was 304 MHz for a V_{DD} = 5 V. Several reasons were found to contribute to the less than expected frequency. The input voltage to the ICMD used a square wave, while the CMTL output at higher frequencies is similar to a distorted sine wave. The output voltage in Figure 7-8 used the Alternate peak to peak measurement which is a standard in the industry for measuring peak to peak voltages. Using the Alternate amplitude oscilloscope measurement, the output voltage produced about 25% smaller numbers at the higher frequencies resulting in a more conservative measurement. This is due to the waveform smoothing algorithm used by the Alternate amplitude method. Also, at the higher frequencies there are some differences in the amplitude of the differential voltage between complementary states, as well as in the output offset voltage, that must be taken into consideration when determining the worst case frequency of operation. For instance, if the single-ended outputs were 0.5 V and the difference in common mode was 0.25 V then the differential voltage would be one volt in one of the logic states and 0 V in the complementary state. If the common mode was 0 V, the differential voltage would be a normal ± 0.5 V. Also, if there is any phase shift in the two signals, the differential voltage is reduced by an amount equal to the change in offset voltages between the logic 1 and logic 0 states while the single-ended voltages remain unchanged. Another factor that must be taken into consideration when the positive and negative differential voltages are not equal is that the pulse width becomes smaller for the smaller signal. A smaller pulse increases the amount of voltage that the receiver requires due to the higher frequency component. This information was used to generate equations that would modify the lab measurements to generate a modified reduced output voltage as well as a modified increased input voltage (due to the potentially higher frequency component in the waveform). The final result was that the lab data agreed with the calculated typical operating frequency.

Table 7-1 shows the worst case operating frequencies as well as the minimum I/O voltages when using the CMTL differential driver to drive a terminated 50Ω line with 100Ω load across one end or 100Ω load across both ends of the lines. These values were calculated using conservative K factors to modify the typical lab results in order to compensate for process, temperature, V_{DD}, and noise margins. The input and output voltages were first modified to agree with typical lab operating frequencies as discussed above. Then the output voltage was reduced by the worst of either a 30% reduction at the measured frequency or the voltage at 1.3 times the frequency while the input voltage required by the receiver was increased by 50%. A worst case noise margin of about 15% of the loaded DC voltage swing was also used. The worst case noise margin can be calculated from Table 7-1 by subtracting the worst case input voltage swing per pin (V_{in}) of the receiver from the worst case output voltage per pin (V_{out}) of the driver. For a V_{DD} = 5 V ±10%, the worst case noise margin at the worst case frequency is 100 mV for a 100Ω load or 75 mV for a 50Ω load across the outputs. For 3.3V operation, a range of -5% to +10% was chosen since the worst case frequency of operation drops rapidly at lower voltages. For a V_{DD} = 3.14 V to 3.63 V, the worst case noise margin at the worst case frequency is 50 mV for a 100Ω load or 35 mV for a 50Ω load across the outputs. Testing showed that the CMTL output with the active termination (OD32TCMT) driving differentially with no resistor terminations at the end of the lines had typical operating frequencies that were about the same as the case when loading a 50Ω load across the outputs. Therefore, for this open load case, use the worst case frequencies shown for the 50Ω load across the outputs.

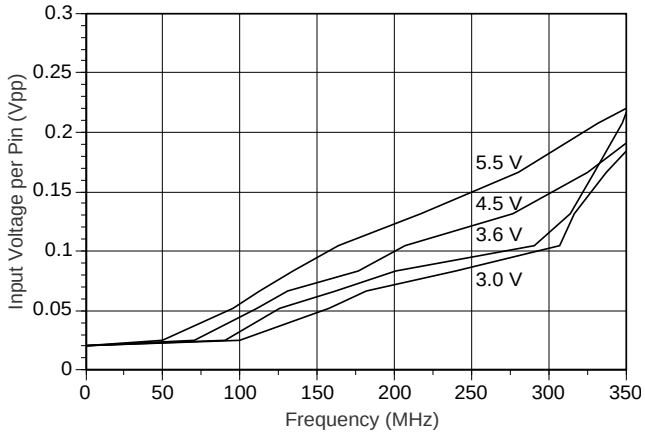


Figure 7-7 Typical CMTL Minimum Input Amplitude versus Frequency

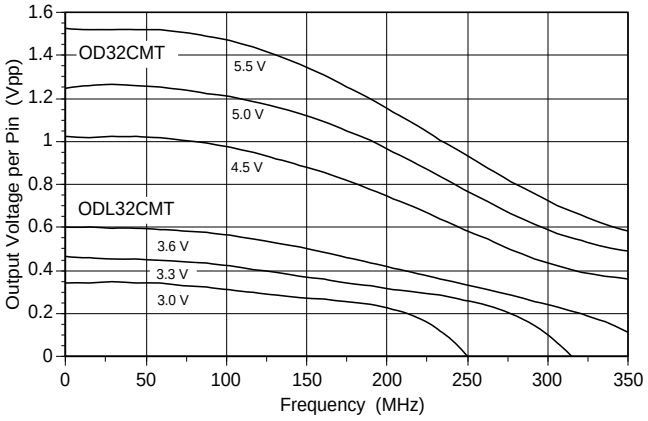


Figure 7-8 Typical CMTL Output Amplitude versus Frequency

Table 7-1 Differential CMTL Operating Limits

Operating Voltage	Tj = -40 to 85° C					
	Min. I/O Voltage			W.C. Frequency		
	Vin mVpp	Vout[1] mVpp	Vout[2] mVpp	Clock[1] MHz	Clock[2] MHz	Data Mb/s
3.14 - 3.6 V	100	135	150	100	105	160
4.5 - 5.5 V	200	275	300	195	210	250

1. Minimum V_{out} and W.C. clock frequency for 50Ω load across differential output. 2. Minimum V_{out} and W.C. clock frequency for 100Ω load across differential output.

7.4 CMTL Common Mode Input Range

Measurements of the common mode range input versus amplitude are plotted for the ICMD input macro. The test circuit is given in Figure A-2. Figures 7-9 through 7-12 are graphs showing the common mode range for several frequencies at V_{DD} ±10% at 3.3 and 5.0 V. The junction temperature is 85°C while the process is typical. These plots specify the mid-point of the voltage amplitude required at the input for operation at the given frequency and supply voltage. For example, for 50 MHz operation, Figure 7-9 suggests that an input voltage (X-axis) of 300 mV (peak-to-peak per pin), at a supply voltage of 4.5 V, would require the amplitude mid-point to be between 0.35 V to 3.7 V.

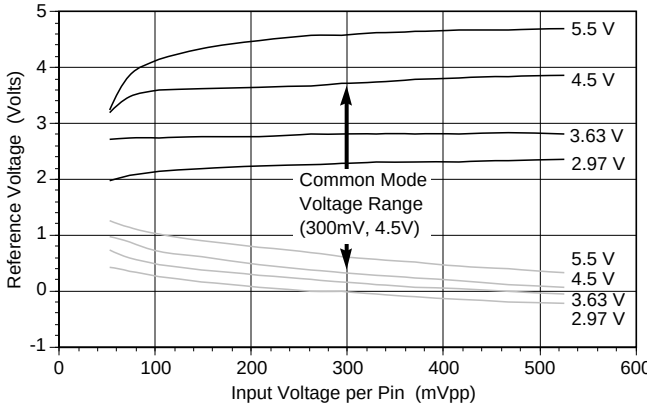


Figure 7-9 ICMD/ILCMD Operating Common Mode Range for V_{DD} Voltages at 50 MHz

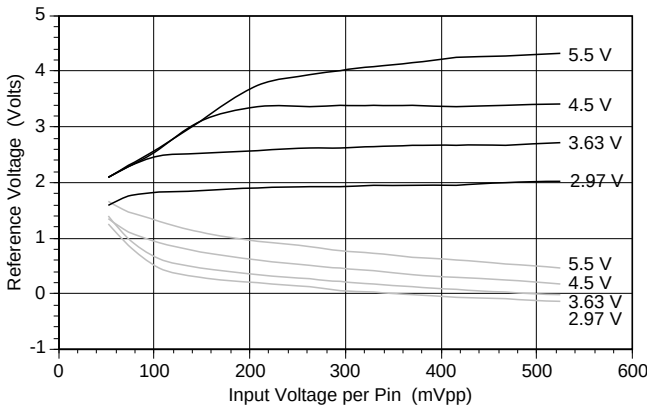


Figure 7-10 ICMD/ILCMD Operating Common Mode Range for V_{DD} Voltages at 150 MHz

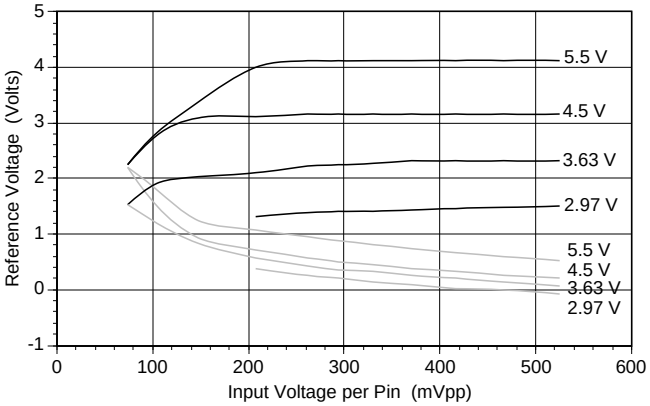


Figure 7-11 ICMD/ILCMD Operating Common Mode Range for V_{DD} Voltages at 250 MHz

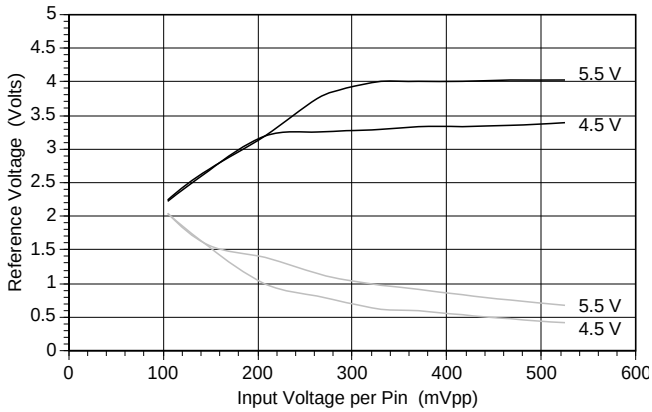


Figure 7-12 ICMD/ILCMD Operating Common Mode Range for VDD Voltages at 350 MHz

8. PECL and LVDS Measurements and Specifications

8.1 PECL and LVDS Operating Frequencies

Worst case frequency testing was performed on the various ways of interfacing the H4CP array with Standard PECL and LVDS logic devices as described previously. Based on these tests, a method was developed to determine the worst case frequencies using some conservative techniques to accommodate variations in process, temperature, and voltage while maintaining an AC noise margin of at least 10% of the typical logic swing. The results are shown in Table 8-1 to Table 8-5. The data rates shown in the tables were conservatively estimated, based on previous data, by multiplying the frequencies by a factor ranging from 1.2 to 1.4 depending on conditions such as single-ended or differential operation. The frequency component is 1/2 the data rate. If the data rate is 200 Mb/s, the maximum frequency is 1/2 this rate or 100 MHz. For testing standard PECL logic devices driving the various PECL input macros on the H4CP array, the MC100EL16 ECLinPS Lite device was used to drive 12 inches of 50Ω cable which connected to a PECL receiver that drove a divide by 8 counter. The input circuit is similar to the one shown in

Figure A-2. The operating frequency was tested for correct operation of the internal counter over the power supply range. Also, the minimum input voltage amplitude required for the differential PECL input to drive a divide by 8 counter was measured and plotted as shown in Figure 8-1. For the single-ended PECL input macros (IPN, IPXN, ILPN), the input voltage shown in Figure 8-1 should be multiplied by 2.

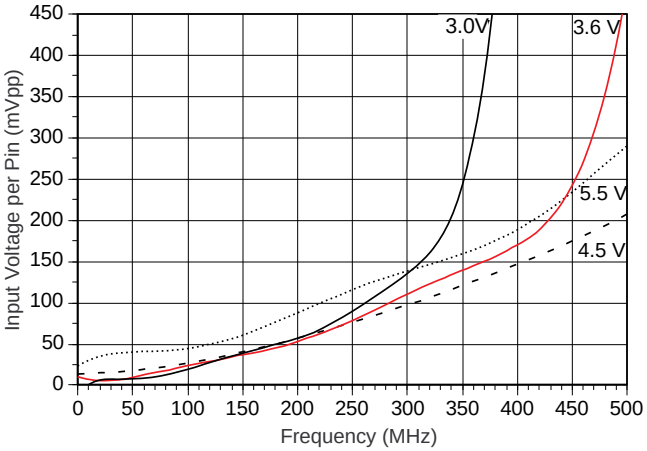


Figure 8-1 Typical Differential PECL (IPD/ILPD) Minimum Input Amplitude versus Frequency

Table 8-1 shows the worst case operating frequencies as well as the minimum I/O voltages for both single-ended and differential PECL receivers. The output voltage (V_{out}) is estimated to exceed 650 mVpp for frequencies up to 650 MHz for devices such as the 100EL16. The worst case noise margin at the worst case frequency can be obtained by subtracting the worst case input voltage from the worst case output voltage. The worst case input voltage was conservatively determined by the worst condition of increasing the typical input voltage by 50% or using the input voltage at 1.5 times the worst case frequency. For 3.3 V operation, a range of -5% to +10% was chosen to maximize the frequency of operation. It is expected that standard 3.3 volt PECL logic devices will be offered by vendors in order to reduce power. Note that for V_{DD}=5 V, the worst case system operation of 325 Mb/s can be obtained by using the differential PECL for the clock (400 MHz worst case), and using single-ended PECL for the data lines at 325 Mb/s.

Table 8-1 Operating Limits for PECL Receivers Using IPD/ILPD/IPN/ILPN

Operating Conditions		Tj = -40 to 85° C			
		Min. I/O Voltage		W.C. Frequency	
		Vin mVpp	Vout[1] mVpp	Clock MHz	Data Mb/s
Single-Ended	3.14 - 3.6 V	450	650	225	270
	4.5 - 5.5 V	450	650	275	325
Differential	3.14 - 3.6 V	350	600	250	325
	4.5 - 5.5 V	450	650	400	550

1. Output voltage is dependent on the standard PECL device chosen to drive H4CP inputs; most standard PECL drivers will exceed 650 mVpp at frequencies up to 650 MHz.

For testing the frequency capabilities of CMTL and GTL for driving standard PECL logic (such as the MC100EL16 ECLin PS Lite), the circuits used to generate Table 4-3 were tested. For each test, 12 inches of 50Ω cable was connected between the driver and receiver. The criteria used to determine the typical operating frequency was to increase the frequency until the amplitude of the at the output of the PECL receiver was less than 650 mV over the power supply range. Also, for single-ended interface, the duty cycle of the output should be within the 30 to 70% range.

Table 8-2 and Table 8-3 show the worst case operating frequencies as well as the minimum I/O voltages when using CMTL and GTL to drive standard single-ended and differential PECL receivers. The minimum input voltage was not measured on the standard PECL logic device since this is specified on the data sheet. The output voltage amplitude and levels were measured and plotted although not shown in this report. The max output amplitude (V_{out}) was determined by multiplying by 2 the smallest voltage that is measured across the receiver when the output is a logic 1 or a logic 0 state at 1.3 times the worst case frequency. This was needed so that the worst case noise margin at the worst case frequency can be obtained by subtracting the worst case input voltage from the worst case output voltage. For 5 V interface, the highest frequencies are obtained using CMTL to drive PECL. However, the on-chip power is much higher than when using GTL as shown in Table 4-3.

Table 8-2 Operating Limits for CMTL Driving Standard PECL[1]

Operating Conditions		Tj = -40 to 85° C			
		Min. I/O Voltage		W.C. Frequency	
		Vin[2] mVpp	Vout mVpp	Clock MHz	Data Mb/s
Single-Ended	4.75 - 5.25V	400	600	250	300
Differential	4.75 - 5.25V	150	750	300	400

1. See Table 4-3 for circuit configurations.
2. Input voltage is dependent on the PECL device chosen to receive signals.

Table 8-3 Operating Limits for GTL Driving Standard PECL[1]

Operating Conditions		Tj = -40 to 85° C			
		Min. I/O Voltage		W.C. Frequency	
		Vin[2] mVpp	Vout mVpp	Clock MHz	Data Mb/s
Single-Ended	3.14 - 3.6 V	400	600	225	270
	4.75 - 5.25V	400	600	200	230
Differential	3.14 - 3.6 V	150	300	225	300
	4.75 - 5.25V	150	400	225	300

1. See Table 4-3 for circuit configurations.
2. Input voltage is dependent on the PECL device chosen to receive signals.

For GTL driving single-ended PECL, the worst case frequency is 200 MHz (300 MHz typical) for V_{DD} = 5 V and 225 MHz (400 MHz typical) for V_{DD} = 3.3 V. However, due to the slow rise time compared to the fall time (discussed in section 5.2), the clock duty cycle will range from 30 to 70% for V_{DD} =

5 V. It is recommended that the single-ended GTL to PECL at V_{DD} = 5 V be used for the data rates up 225 Mb/s to limit the number of pins required and that the differential GTL to PECL be used for the clock rates at 225 MHz in order to achieve a tighter control on the clock duty cycle.

Table 8-4 and Table 8-5 show the worst case operating frequencies when using GTL to drive and receive standard LVDS signals. The methods in generating these tables was similar to the method discussed previously for GTL driving and receiving PECL signals. LVDS receivers were not available for testing so that the specified LVDS input and output voltages were assumed to be correct. For driving LVDS receivers, the voltage at the end of the line was observed and measured so that the worst case output voltage was the voltage measured at 1.3 times the worst case frequency. For receiving LVDS signals, Figure 6-1 was used to determine the differential input voltage required. The input voltage shown in Figure 6-1 was dividing by 2 in order to convert from single-ended to differential operation. Then, the typical input voltage was increased by 50%. When driving the LVDS receivers, the minimum input amplitude is specified at 100 mV. However, when using the GTL to receive the LVDS signals, Table 8-5 shows the input amplitude to be slightly higher at 150 mV. Also, when using LVDS to drive GTL the output is specified as 250 mV minimum while Table 8-4 shows the GTL circuit having a slightly lower minimum output amplitude of 200 mV in order to operate at higher frequencies. However, the AC noise margin of 100 mV is still quite acceptable for both driving and receiving LVDS signals.

Table 8-4 Operating Limits for GTL Driving Standard LVDS[1]

Operating Conditions	Tj = -40 to 85° C			
	Min. I/O Voltage		W.C. Frequency	
	Vin[2] mVpp	Vout mVpp	Clock MHz	Data Mb/s
3.14 - 3.46V	100	200	200	275
4.75 - 5.25V	100	200	225	300

1. See Table 4-3 for circuit configurations.
2. Input voltage is dependent on LVDS input specification.

Table 8-5 Operating Limits for receiving LVDS Using GTL Receivers[1]

Operating Conditions	Tj = -40 to 85° C			
	Min. I/O Voltage		W.C. Frequency	
	Vin mVpp	Vout[2] mVpp	Clock MHz	Data Mb/s
3.14 - 3.46V	150	250	150	215
4.75 - 5.25V	150	250	200	275

1. See Table 4-3 for circuit configurations.
2. Output voltage is dependent on LVDS output specification.

8.2 PECL Common Mode Input Range

Measurements of the common mode range input versus amplitude are plotted for differential PECL input macros. The test circuit is given in Figure A-2. Figures 8-2 through 8-6 are graphs showing the common mode range for several frequencies at VDD ±10% at 3.3 and 5.0V. The junction temperature is 25°C while the process is typical. These plots specify the mid-point of the voltage amplitude required at the input for operation at the given frequency and supply voltage. For the single-ended PECL input macros (IPN, IPXN, ILPN), the input voltage shown in Figures 8-2 to 8-6 should be multiplied by 2.

It is important to show that standard PECL outputs can meet the input common mode range over frequency and input voltage. The common mode output voltage or crossing point of standard differential PECL normally ranges from 1.2 to 1.5 V below V_{DD}. For 200 MHz differential operation with 450 mV input voltage and V_{DD} = 5.5 V, the common mode range can be found from Figure 8-4 to operate in the range of 1.25 to 4.85 V with reference to ground or 0.65 V to 4.25 V below V_{DD}. This provides a common mode noise rejection of 0.55 V positive or 2.75 V negative for the normal PECL range of 1.2 to 1.5 V below V_{DD}. The common mode operating range gets smaller at the higher frequencies and at smaller input voltage amplitudes. From Figure 8-5 at 300 MHz, the common mode operating range is 0.7 V to 4.05 V below V_{DD}. This shows that the PECL receivers can easily meet the common mode range to receive standard PECL signals.

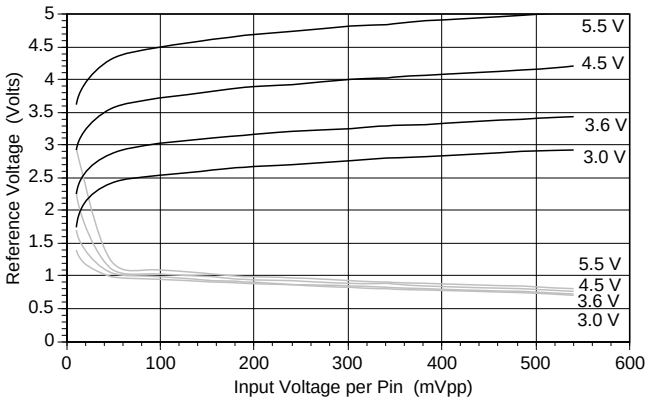


Figure 8-2 PECL Operating Common Mode Range for V_{DD} Voltages at 50MHz

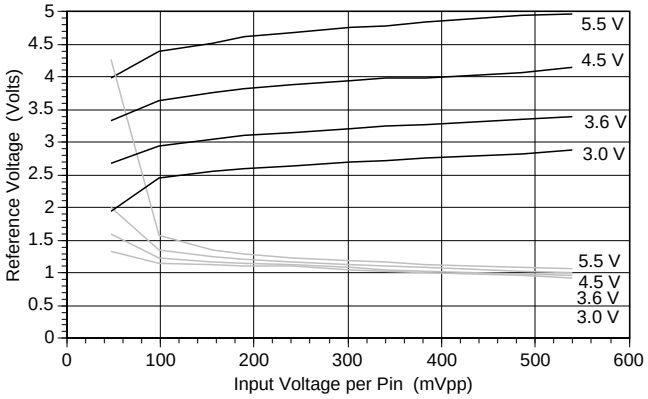


Figure 8-3 PECL Operating Common Mode Range for V_{DD} Voltages at 150MHz

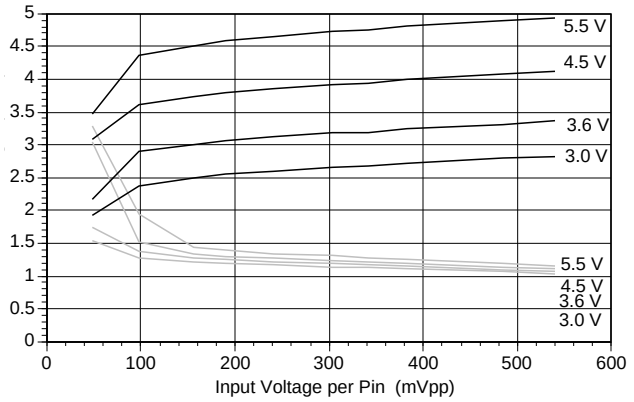


Figure 8-4 PECL Operating Common Mode Range for V_{DD} Voltages at 200MHz

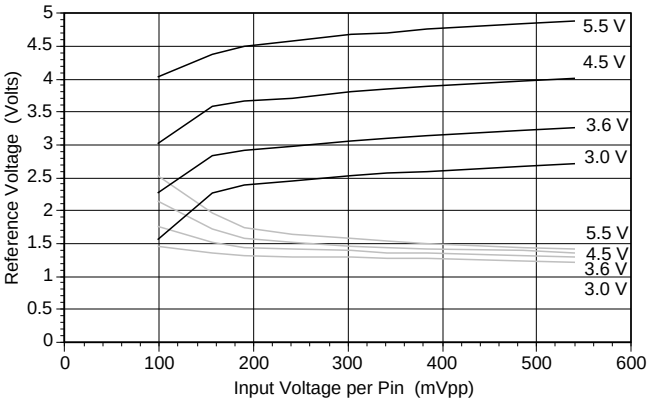


Figure 8-5 PECL Operating Common Mode Range for V_{DD} Voltages at 300MHz

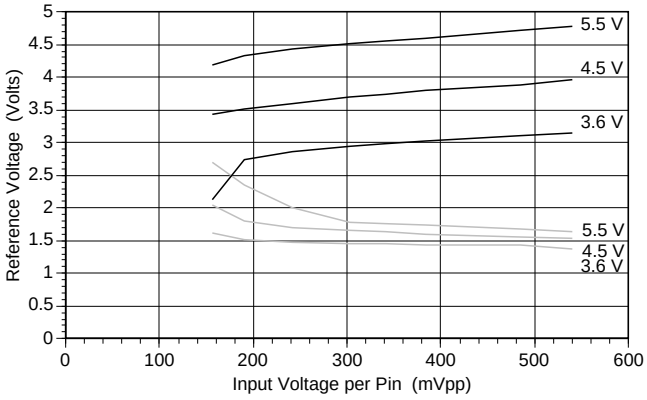


Figure 8-6 PECL Operating Common Mode Range for V_{DD} Voltages at 400MHz

8.3 CMTL Driving ECL

A test was performed to show a point-to-point connection between CMTL driving ECL without a termination resistor. Twelve inches of 50Ω coax were used between the OD32TCMT output and the MC10E116 ECLinPS part.

The test circuit is shown in Figure A-3. Differential voltage measurements were taken at the driver (R4 and P6) and the receiver (pin3 and pin4). The differential voltage waveforms (Figure 8-7) at the driving end of the line may look distorted due to reflections that occur at the receiving end of the line. This is normal for series termination especially since the output impedance of the OD32TCMT is about 28Ω (see Figure 7-2) which is acceptable but not the ideal 50Ω. For applications that require driving PECL receivers near the sending end of the line, parallel termination should be used as described in Figures 4-3 and 4-4. This will give very clean signals at both ends of the line. When looking at the waveforms, the most important signal is the one that the receiver sees differentially across pin3 and pin4 (see Figure A-3). At 10 MHz, the differential voltage at the receiver has some overshoot of about 25% which increases the noise margin. The undershoot is 5 to 10% which decreases noise margin. The overshoot is due to the mismatch of the 28Ω OD32TCMT output impedance and the 50Ω characteristic impedance of the coax cable.

The undershoot is due to the return reflection that occurs at two times the line delay (T_{line} = 2.25 ns). The voltage across the receiver reaches $\pm$ 2.8 V during the overshoot which reduces to $\pm$ 1.7 V during the undershoot and finally reaches a steady state voltage of $\pm$ 1.9 V. The 10E116 receiver only requires $\pm$ 0.15 V worst case.

At 100 MHz, the signals at the driver look noisy due to reflections. At the receiver, the waveform looks good with the voltage across the receiver increasing to $\pm$ 3.1 V. The reflections that previously caused the undershoot are absorbed resulting in slower rise and fall times.

At 200 MHz, the signal at the receiver has very little overshoot and undershoot since the line delay is approaching one-half of the wavelength which causes the reflections to cancel. The amplitude is attenuated to a voltage of $\pm$ 1.5 V.

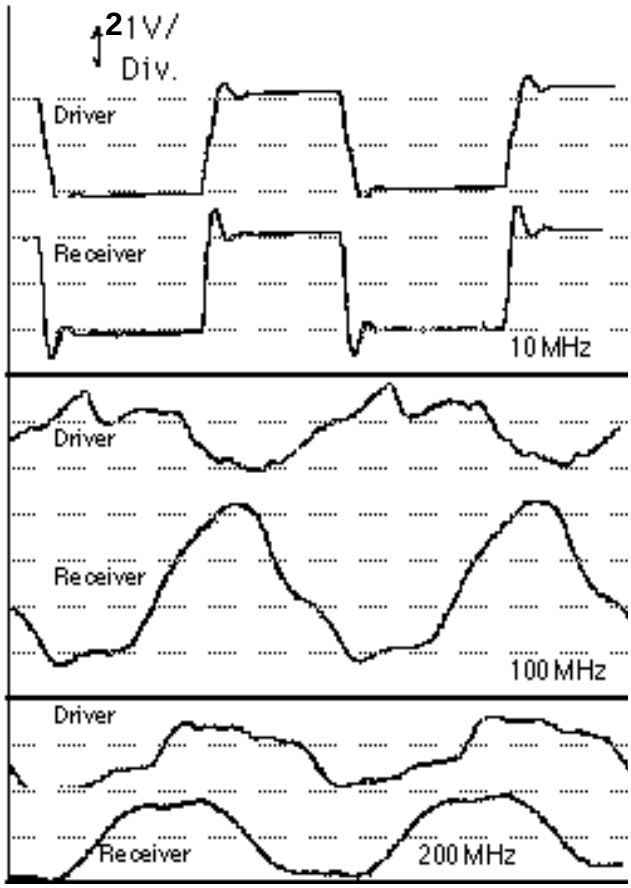


Figure 8-7 OD32TCMT Output Driving ECLinPS

9. Recommendations for Placement of Sensitive Inputs

The CMTL, GTL, and PECL receivers are high gain comparators that will operate with very small voltage amplitudes. Therefore it is very important to prevent crosstalk voltage from coupling to these and other edge sensitive or level sensitive inputs such as CLOCK, RESET, and SET signals. It is recommended that differential lines be used whenever possible and especially for clock signals since differential drive reduces simultaneous switching current, reduces ground bounce, and provides superior noise margin through common mode noise rejection. Since an output that is adjacent to a differential input will cause crosstalk voltage on only one of the inputs, care must also be taken for placing outputs next to sensitive differential inputs. It is recommended that all sensitive inputs, single-ended and differential, not be connected to a pad that is adjacent to an output signal. Also, this applies to package pins. For some packages, it is possible that although they are not adjacent on the chip, they could be adjacent in the package. Therefore, the routing in the package is also important in preventing sensitive pins from being adjacent to output signals. The PC board routing must also prevent routing of outputs next to sensitive inputs. Power and ground pads are allowed to be adjacent to sensitive input pads.

References

(1) J.H. Quigley, J.S. Caravella, W.J. Neil, Current Mode Transceiver Logic (CMTL) for Reduced Swing CMOS, Chip to Chip Communication, Proceedings of the IEEE ASIC Conference 1993.

(2) B. Blood, MECL System Design Handbook, Motorola Semiconductor Products.

(3) R. Quinnell, “High-Speed Bus Interfaces”, EDN, September 30th, 1993, pp 43-50.

Appendix A: Test Circuits

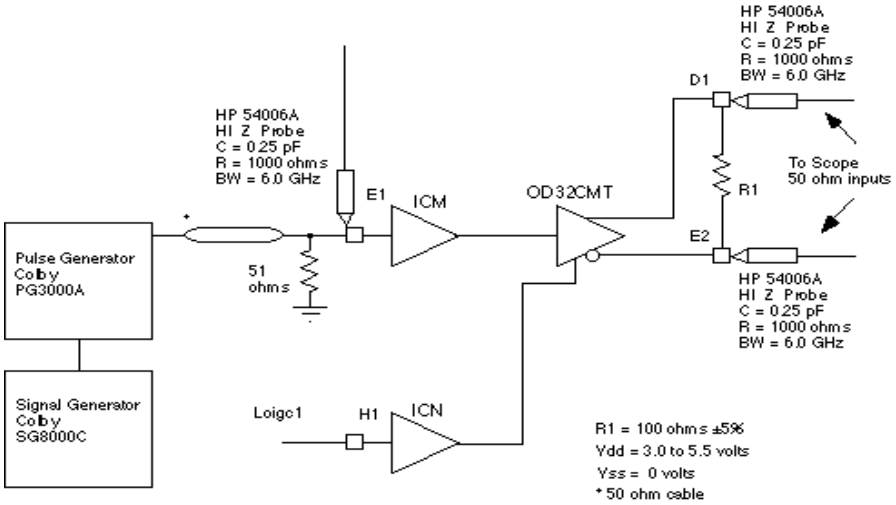


Figure A-1 Circuit for CMTL Output Voltage Measurement

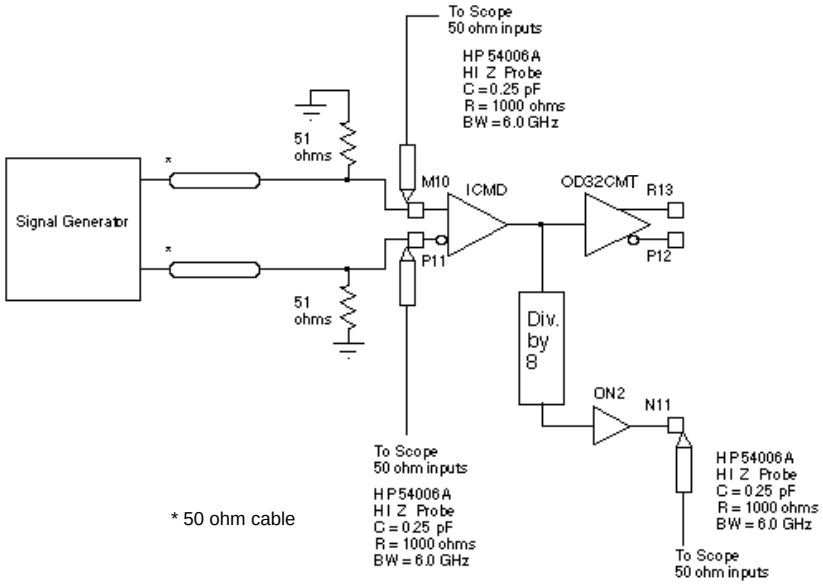


Figure A-2 Circuit for CMTL Common Mode Input Measurement

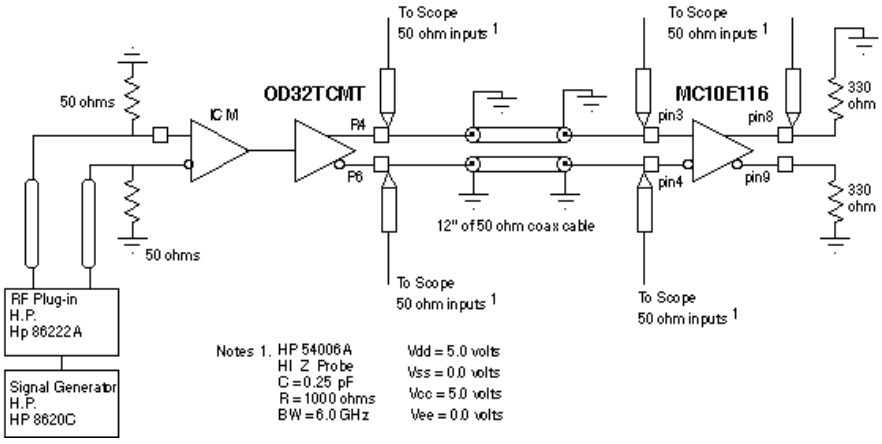


Figure A-3 Circuit for CMTL Driving PECL

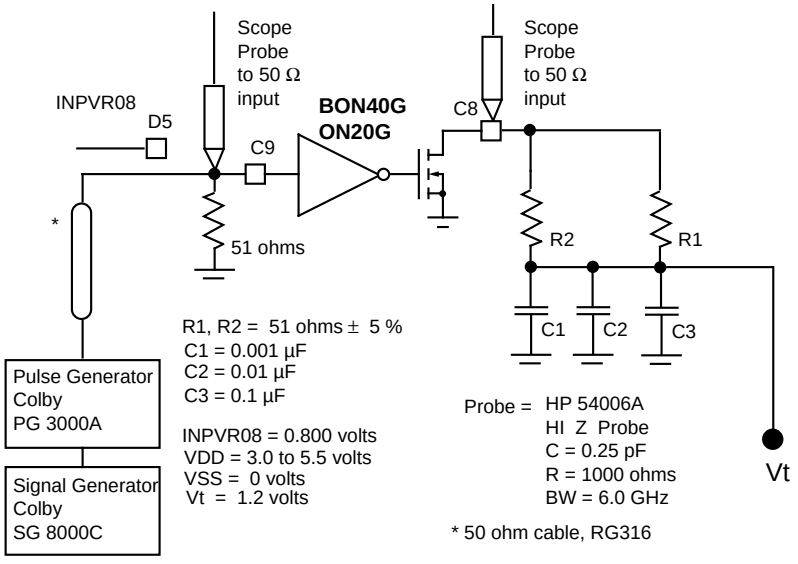


Figure A-4 Circuit for GTL Output Voltage Measurement

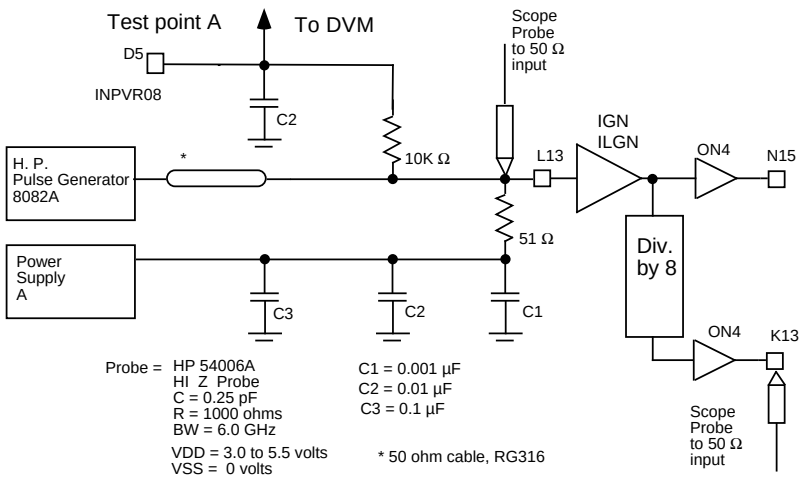


Figure A-5 Circuit for GTL Common Mode Input Measurement

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