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RF Power Circuit Concepts Using FETs and BJTs

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Similarities and differences in RF power circuits using silicon Field Effect Transistors and Bipolar Junction Transistors are discussed along with their characteristics and performance. The discussion is limited to amplifiers and multipliers. Oscillators are usually designed for low signal levels, which are then amplified. Although power oscillators are employed in some applications, requirements for them are few. RF power is normally considered as power levels above 1 Watt. Below this we are talking about small signal RF, and the circuit design concepts are quite different.

Basic Characteristics

Since the first power FETs came to the market, it has been repeatedly noted in the literature, that the FET will probably never replace the BJT in all applications. Even with the significant advances in FET technology, and their increased use at frequencies below 1 GHz, this still appears to be an accurate overall assessment of FETs and bipolar transistors in the field of RF. Increased use of FETs is a result of their lower prices along with a greater variety of product and a variety of good higher frequency devices offered by several manufacturers. Most RF power design engineers accustomed to circuit design with BJTs are slowly beginning to look at the FET designs and learn about the differences in parameters and behavior between the two types of semiconductors. Circuit design with each type is very much similar. The same RF design practices, such as grounding, filtering, by–passing and creating a good circuit board lay–out apply in each case.

All commercially available RF power FETs, excluding the SIT (Static Induction Transistor which is a depletion mode junction FET) and Gallium Arsenide FETs (which are depletion mode MESFETs) are of the enhancement mode N–channel type. Thus the main difference between the FET and the BJT may be that the FET always requires positive gate bias to bring the input signal voltage swing closer to or to the gate threshold voltage. Otherwise only the positive peaks of the input signal will turn the device on, resulting in nonlinear operation and loss of power gain. This effect is lessened at increasing frequencies, where the input voltage swing is usually higher due to the lower power gain of the device. The bias source may be a simple resistor divider since no current is drawn. For linear operation the BJT also requires D.C. base voltage, which is positive for an NPN type transistor. Best results are obtained with a constant voltage source of 0.6 – 0.7 V, which should be able to supply a current of I_C(peak)/h_{FE}.

Precautions must be taken with each type device, when designed into a particular application. The FETs are sensitive to gate rupture. It can be caused by excessive D.C. potential source. This can be compared to exceeding the voltage rating of a capacitor, which usually results in a short or leakage. A power FET can be “restored” in some instances by applying a voltage lower than the rupture level between the gate and the source. It must be at a sufficient current, but not higher than 1 – 1.5 A to clear the gate short. A higher current would fuse one of the bonding wires to the area of the short on the die. A number of cells will always be destroyed, but with larger devices, such as 30 W and higher no difference in performance may be noticed. Long term reliability after such an operation may be jeopardized, and is not recommended in cases where reliability is required.

A weak spot with the BJTs is a possibility for thermal runaway. Devices with diffused silicon emitter ballast resistors are less susceptible to thermal runaway than devices having nichrome resistors. The diffused silicon resistors have a slight positive temperature coefficient, while the nichrome resistors have about a zero coefficient. However, the diffused resistors are nonlinear with current, and devices using them are less suitable for applications requiring good linearity. The main reason for the thermal runaway with the BJTs is the increasing h_{FE} with temperature, while the g_{fs} of a MOSFET goes down, trying to turn the device off. In contrast, the gate threshold voltage decreases by about 1 mV/°C, which makes the temperature profile of a gate biased device dependent on the initial value of the G_{FS} and the voltage of operation.

The figures of merit of a BJT and FET are defined as emitter periphery/base area and gate periphery/channel length respectively. In practical terms these relate to the ratio of feedback capacitance to the input impedance since finer geometries result in lower feedback capacitances. This only applies to common emitter and common source configurations. Thus it would appear that higher figure of merit devices are more stable than those with low figure of merit. This would actually be true, except that in the first case the power gain is also higher, which can cause instabilities as a result of stray feedback or at a high frequency, where the feedback capacitance produces positive feedback due to phase

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BJT, which is a result of a varactor effect in its diode junctions, mainly the collector–base. It is commonly known as “half f_o”, which is usually a steady spurious signal half the frequency of the excitation. Due to the lack of junctions in a FET, this phenomenon is virtually unknown in MOSFET power circuits.

The term f_T, which is the frequency at which $h_{FE} = 1$, is not really applicable to FETs, although it is commonly used. In a FET the unity gain frequency is determined by the ratio of Z_{in}/C_{RSS}, as discussed earlier, rather than by the charge storage effects of a BJT. A definition for it can be approximated as: $g_{fs}\{2\pi[C_{ISS} + (g_{fs} \times C_{RSS})]\}$. However, for an equal power rating the MOSFET requires almost twice the die area of a BJT, which somewhat equalizes the gain–bandwidth performance of the two. The plot of Alpha cutoff frequency shown in Figure 1, does not apply to FETs since it is not practical to operate them in a common gate configuration as explained later.

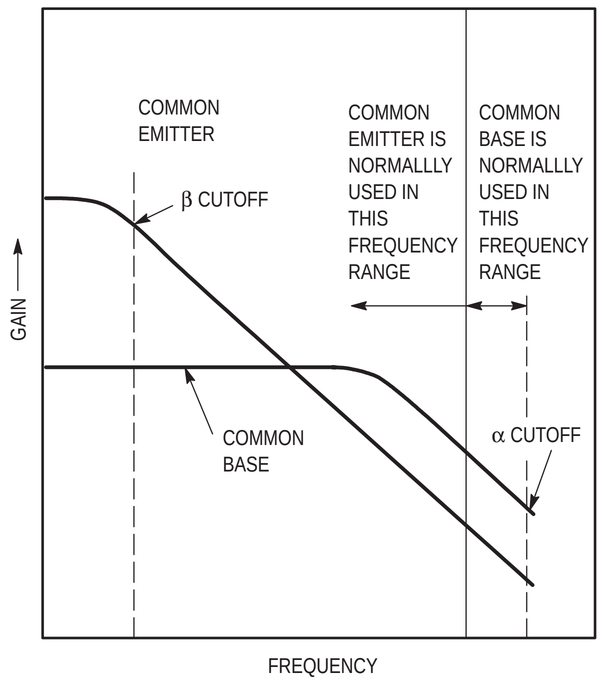

Figure 1. Common Emitter and Common Base Gain Slopes

Regarding impedance matching, the largest difference can be noticed in the base–emitter and gate–source impedances. At D.C. the MOSFET has an infinite gate–source impedance, whereas the BJT exhibits the impedance of a forward biased diode. At higher frequencies, depending on the device’s electrical size, the gate–source capacitance (C_{ISS}) enhanced by the Miller effect, together with the wire bond inductances e.t.c. will form a complex impedance that may be lower than that of the BJT’s. The output capacitance (C_{OB}/C_{OSS}) is almost equal for each type of device of equivalent electrical size. The output capacitance has a large effect in the efficiency of an amplifier. The power loss due to the output capacitance for example for a single ended FET amplifier is defined as: $P_S = (2C_{OSS})(V_{DD})^2(f)$ and the efficiency $(P_{out}/P_{out} + P_S)$. The formula proves wrong the common belief that higher efficiencies are possible at higher voltage operation. We can see that the power loss is in direct relation to the capacitance and to the square of the supply voltage. At relatively low operating voltages, other factors like the saturation voltage may become more dominant offsetting the situation.

Common Emitter and Common Source

The Common emitter (C_E) and common source (C_S) are the most widely used circuit configurations. They exhibit good stability, good linearity and high power gain up to UHF. C_E and C_S are the only circuit configurations, where the input and output are out of phase. This enhances the stability, except for the half f_o mode and at frequencies where the feedback capacitance delays are close to 180°. Figures 2 and 3 show examples of such narrow band circuits with lumped constant matching elements that are usable to UHF.

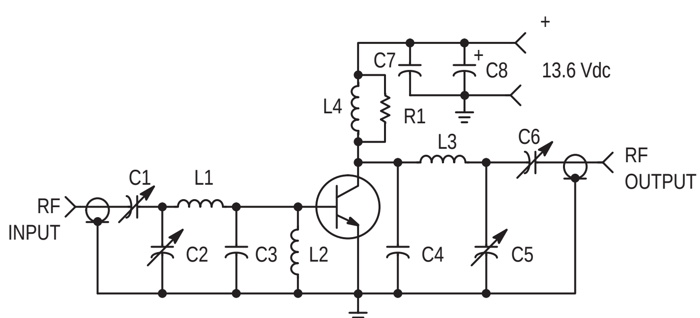

Figure 2. A Typical Narrow Band BJT Amplifier Circuit up to 200 – 300 MHz

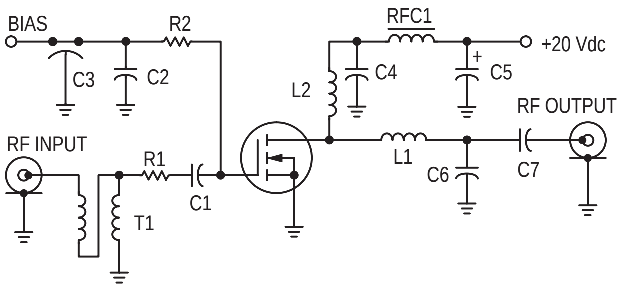

Figure 3. A Typical Narrow Band MOSFET Amplifier Circuit up to 200 – 300 MHz

At frequencies over 300 – 400 MHz, stripline techniques or a combination of stripline and transformer impedance matching techniques are normally used. See Figures 4 and 5 for typical examples. If broadband performance is desired, push–pull configuration makes the impedance matching easier to implement to a 50 Ohm interface due to the initially higher device impedance levels. In multistage systems the interstage impedance matching is usually done at lower than 50 Ohm levels, and in some instances very little impedance transformation is required. This may result in better broad band performance than deploying 50 Ohm interface between each stage, but the latter has the advantage that each stage can be individually tested in a standard 50 Ohm set–up. Up to VHF and low UHF, the input impedance of a MOSFET is high compared to that of BJT but at higher frequencies they will reach similar values and the matching procedures become almost identical.

In practice virtually all multioctave amplifier designs independent of the frequency spectrum and device type are of push–pull circuit configuration. Another advantage with push–pull is that the power levels of two devices are automatically combined for higher power output levels which allows the use of electrically smaller individual devices. RF power transistors housed in push–pull headers have been available since the mid 70s, but only since the development of high frequency FETs the concept has become popular. Both FETs and BJTs are now available in push–pull headers, most of them in the so called “Gemini” type. The term Gemini (twins) refers to two individual and independent transistors mounted on a common cooling flange next to each other. The Gemini package is manufactured in several physical sizes, the largest being able to dissipate up to 500 – 600 watts. An obvious advantage with any push–pull transistor, whether in a single push–pull header or in a Gemini package, is the close electrical proximity of the two units. This greatly enhances the device performance of a push–pull circuit, where the important factor is a low emitter–to–emitter (source–to–source) inductance and not the emitter–to–ground inductance. In all Gemini housed devices, the emitter (or source) is connected to the mounting flange, which is considered to be the electrical ground.

For these push–pull devices the two die are usually selected as adjacent from one semiconductor wafer. For the BJTs this procedure is normally sufficient, but with the MOSFETs, where the gate threshold voltages cannot be more than within 50 – 100 mV maximum apart, other techniques such as die mapping may be required. In a BJT the power gain is determined primarily by die geometry (figure of merit), the values of the emitter ballast resistors and to a lesser extend the value of h_{FE}, whereas in a MOSFET the power gain is determined primarily by g_{fs} and the amount of drain–source bias current. Thus the MOSFET is much more critical in the matching procedure for a push–pull design. As stated earlier, these criteria apply to all circuit configurations.

The base–to–base impedance in class C push–pull is approximately to four times that of the base to ground impedance of one device, however when biased to class A, it approaches 2x the base–to–ground impedance primarily because of the heavily forward biased base–emitter junctions. With MOSFETs, which lacks this diode junction, the gate–to–gate impedance is always about twice that of the gate impedance of one device to ground. The outputs of each type device behave more or less identically. Since in push–pull the output voltage swing is twice that of a single ended device, the impedance will be four times higher. Up to frequencies at which the device output Smith chart plot becomes inductive, the simple formula relating to the supply voltage and P_{out} gives accurate results for all practical purposes, but the output capacitance may have to be taken into account especially in narrow band circuits.

There are no considerable differences in the efficiencies with amplifiers using either type devices, although it is believed that the higher saturation voltage of the FETs would make them less efficient. This may, however, be true only at low operating voltages (12 V and lower). At higher frequencies the device output capacitance has a much larger effect in efficiency, however part of it can be “tuned out” in narrow band circuits.

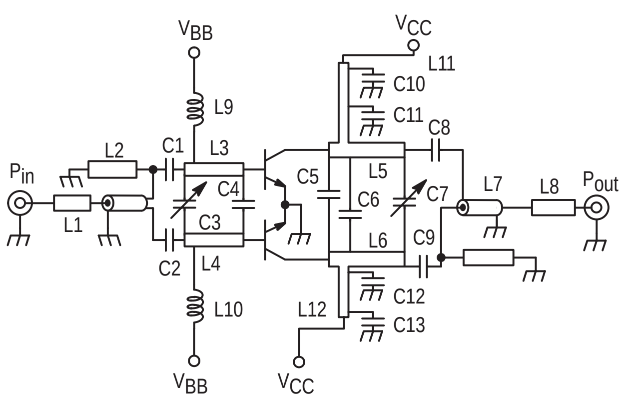

Figure 4. A Typical 225 – 400 MHz Amplifier Using the MRF392 BJT

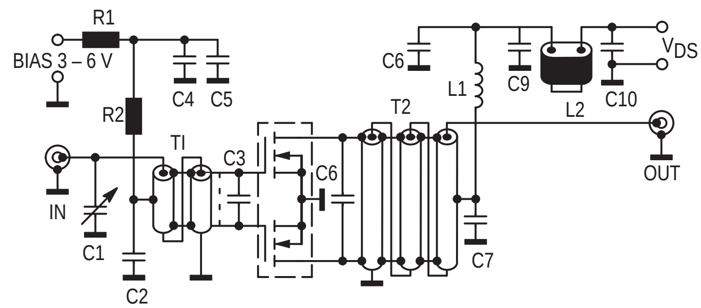

Figure 5. A Typical 10 – 225 MHz Amplifier Using the MRF175GV Device

Common Base and Common Gate

Common base circuits with the BJTs are widely used at UHF and microwave frequencies due to the higher alpha cut–off (see Figure 1). This means that higher power gains are possible at these frequencies in common base than in common emitter configuration. Some disadvantages of common base when compared with common emitter circuits are lower input impedance and decreased stability since the input and the output are in the same phase. The input impedance level can be increased to practical levels by internal matching, i.e., provide matching networks inside the headers, close to the transistor chip. A basic common base, class C, single ended circuit is shown in Figure 6. Stability can be improved by using die with very high f_{TS}, which have low feedback capacitance relative to the input impedance of the die. Stable single frequency or narrow band circuits with fractional octave bandwidths are possible using the common base configuration, but wideband circuits are difficult to design if internal matching is required. The stability is also greatly affected by the common base inductance, which should be minimized including the internal package inductances. Neutralization is employed in some instances to improve the stability, but it is not easy to implement in designs using stripline techniques. The linearity should be at least comparable to or better than common emitter configurations since the feedback capacitance, (which is usually higher) and the output capacitance are now reversed.

In high power circuits, the biasing to linear mode is somewhat difficult as an opposite polarity supply is required at the emitter. In small signal circuits this can be accomplished with an amount of by–passed base to ground resistance to generate a self bias. Push–pull common base circuits are not commonly seen at higher power levels, which usually operate at high UHF or higher frequencies. One reason may be that the 180 degree phase shift is difficult to achieve and hold except for very narrow bandwidths. However, push–pull common base circuits are widely employed at power levels up to 1 – 2 watts in applications such as cable TV amplifiers (as shown in Figure 7) where an un–bypassed common base resistance can be used for self biasing to a linear mode of operation. In each configuration, common emitter and common base, the push–pull design offers the same advantages, of which the most important one is the noncritical base or emitter common mode inductance. The power gain and stability of the push–pull circuit depends to a large extent on base to base inductance.

Since the MOSFET does not have a characteristic like the Alpha cutoff frequency of a BJT, there is no real advantage to operate it in a common gate configuration. In fact the feedback capacitance of a MOSFET is lower than its output capacitance in a common source configuration. These two will be reversed in a common gate configuration, which results in a very unstable condition, (although the Miller effect is not present in contrast to common source configuration) unless the input can be damped with a resistance low enough to suppress the positive feedback to a level of stability. Even then the internal feedback, depending on the device type and package, may be sufficient to make complete stability unattainable. In any case the nonlinearity of the feedback capacitance would result in poor linear performance.

The MOSFET would always have to be biased to a level close to or over the gate threshold voltage in order to overcome that amount of voltage drop with the RF input drive. (This excludes class D and other switchmode systems.) The bias source must be able to carry the full drain current, which at a gate threshold voltage of 4 – 5 volts would amount to a considerable level of dissipation. With the BJTs the voltage is only 0.6 – 0.7 V, and thus much more tolerable. The common gate MOSFET circuit could be useful in relatively low power applications, at frequencies where neutralization can be easily realized and its high AGC range (power gain/gate voltage) can be of advantage.

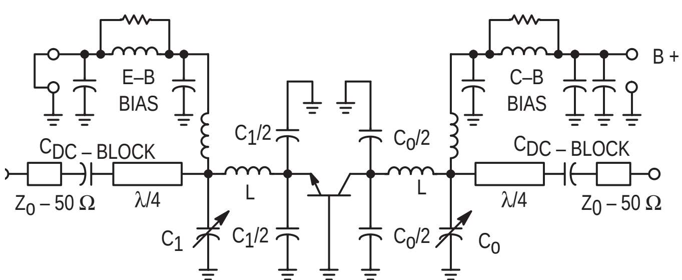

Figure 6. A Common Base Class C UHF Single Ended Amplifier Circuit

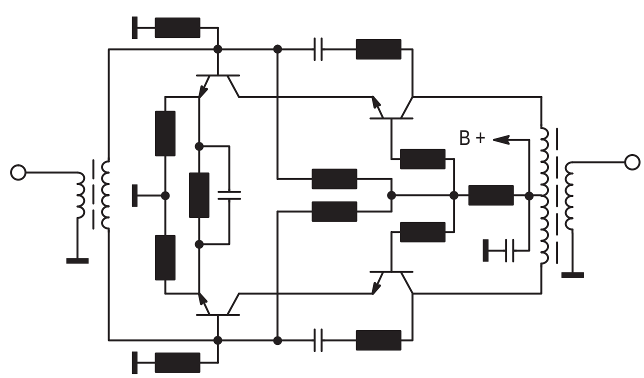

Figure 7. A Common Base Push–Pull Amplifier Stage Used in CATV Linear Hybrids up to 500 MHz

Common Collector and Common Drain

A common collector (emitter follower) circuit is widely used where high input and low output impedance levels are desired. As in a common base configuration, there is no phase reversal between the input and the output. The emitter follower has a voltage gain of less than unity, and amplification is obtained from the current gain through impedance transformation. The output impedance is directly related to the source impedance divided by the current gain (h_{FE}). Conversely the input impedance equals the output load multiplied by the h_{FE}. This makes the emitter follower less suitable for RF power amplifiers than the two other circuit configurations since any variations in the load impedance are directly reflected back to the input. For this reason it is most widely used as a wideband buffer amplifier to drive low impedance or capacitive loads. Especially in a complementary configuration, which provides active "pull–up" and "pull–down" in the output, the circuit offers one of the best drivers for capacitive loads. Some of the applications include CRT video drivers and MOSFET gate drivers in class D/E amplifier systems.

A common drain or source follower circuit configuration represents the emitter follower in bipolar circuits. As in the emitter follower, the input impedance is high and output impedance low. The input capacitance (drain to gate) is low compared to common source and common gate circuits, and considerably lower for the FET than a bipolar of comparable electrical size. This is due to the absence of the forward biased collector–base diode junction. A source follower also has a voltage gain of less than unity, and since it is not a current amplifier, one cannot talk about current gain either. However, the amplification takes place through impedance transformation as in a bipolar circuit. Due to the extremely high input impedance, which varies more with frequency than does the input impedance in common source and common gate circuits, heavy resistive loading at the gate is necessary for any type broadband application. Negative feedback is not necessary, nor is it easy to implement due to equal phases of the input and output. For these reasons, a common source circuit exhibits exceptional stability, but excessive stray inductances in the circuit lay–out can lead to low frequency oscillations. Unlike the emitter follower, variations in the load impedance in a source follower are not reflected to the input. This makes the source follower suitable for RF power amplifier applications at least up to VHF. Push–pull broadband circuits for a frequency range of 2 – 50 MHz have been designed for 200 to 300 watt power levels. Figure 8 shows the basic circuit configuration for a source follower using the MRF140. Their inherent characteristics are good linearity, stability and gain flatness without any leveling networks. High power linear amplifiers are probably the most suitable application for this mode of operation. The AGC range is comparable to that in common source, but a higher voltage swing is required. In high voltage operation it must be noted that the gate rupture voltage can be easily exceeded since during the negative half cycle of the input signal the gate voltage can approach the level of V_{DS}.

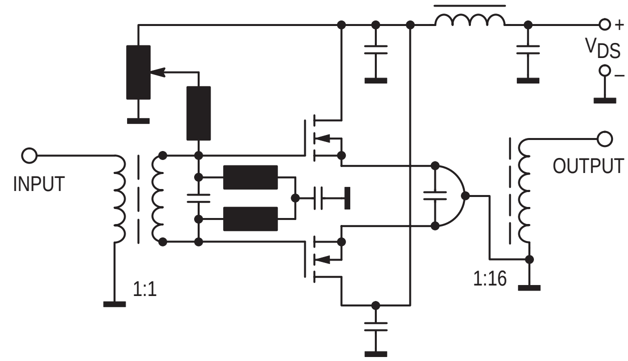

Figure 8. A 300 W Source Follower Push–Pull RF Amplifier Using the MRF140 Power MOSFET

Harmonic Generation

Because harmonic generation is based on nonlinearities, BJTs perform well in this function. The nonlinearity inherent in the base–emitter voltage to collector current transfer characteristics is ideal for harmonic generation. Any class of operation can be employed, but classes C – F are in general the most efficient for high order products. A frequency multiplier is simply a narrow band amplifier stage such as shown in Figure 2, where the input is tuned to the fundamental frequency and the output tank circuit has a higher Q than normal, and is designed to resonate at the desired harmonic frequency. The conduction angle must be adjusted for the best efficiency. Efficiencies exceeding 60% for the 2nd and 40% for the 3rd order products are possible. Class C – F multipliers are best suited for large signal applications such as radar, other microwave and UHF, whereas classes A and B are mostly employed in small signal circuits for receiver and low power transmitter designs. The selected transistor parameters should include an f_T at least twice that of the desired harmonic in order to have sufficient power gain at the harmonic frequency. Other parameters such as the saturation voltage and output capacitance are also important. In applications requiring only odd harmonic extraction, a push–pull circuit configuration may prove to be more efficient than a single ended one due to the automatic suppression of even order amplitudes.

The FETs because of their square–law transfer characteristics are feasible only for second order generation in classes A and B. Efficiencies up to only 20% are typical, but in classes D – F comparable numbers to those of the BJTs are possible due to the FET's high unity gain frequency and high switching speed. In fact the lack of the stored charge effect in a FET may give extremely good results in these classes of operation.

Frequency multiplication up to microwave frequencies has in the past been predominantly done with varactor or step recovery diodes at relatively low power levels. The recent development of fine geometry RF power transistors with their f_T's in the GHz range has pushed the diode superiority to above 5 GHz.

Pulse Power

Semiconductors are increasingly being designed into pulsed applications from low frequencies, such as switching power supplies, to microwave radar. Other applications at HF to UHF include the over the horizon radar, magnetic resonance imaging and laser drivers. The pulse widths range from below a microsecond to several hundreds of milliseconds and the repetition rates can be from less than 1% up to 50%. Unfortunately the semiconductor data sheet information for this mode is given only for devices specifically designed for pulse operation.

In certain short pulse applications the thermal aspects can be ignored to a large degree because of reduced average power dissipation. The temperature time constant of a silicon die itself is around one millisecond, meaning that only the junction or channel will heat up instantaneously during the pulse, the bulk silicon and the die insulator (usually B_{EO}) will remain near the ambient temperature. Thus the device thermal resistance, which is a function of the power dissipated and the temperature of the two materials, will largely depend on the pulse width and the duty cycle and is considerably reduced from the numbers given for CW. Figure 9 shows a graph of the MRF154 RF power FET, which has been used for MRI with pulse–widths up to 5 ms and duty cycles of approximately 10%. The lower thermal resistance makes it possible to obtain peak power outputs much higher than the saturated CW level of a given device. Depending on the exact conditions of operation and certain device parameters, the increase can reach a factor of five or higher. Some of the important device parameters to consider are: 1) The maximum current carrying capability, which is usually given as the maximum continuous current or maximum peak current determined by the number and size of the emitter or source wires to the die as well as the area and type of die metallization. 2) The maximum current where the h_{FE}/g_{fs} will go into compression. The h_{FE}/g_{fs} values are only given for a current at which the device typically operates and at a low nominal voltage.

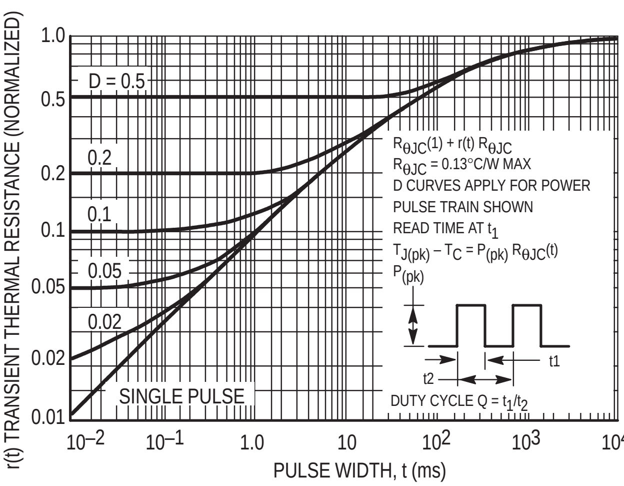

Figure 9. The MRF154 Theta$_{JC}$ vs Pulse Width and Duty Cycle

A pulsed power amplifier is designed much like an amplifier for FM or linear operation except that the output load matching must be done at the peak power level, and less emphasis is required for the efficiency, thermal design and passive component selection due to the low average power. The BJTs are almost exclusively used at microwaves and in unsaturated applications, where the pulse shape must be precisely controlled. The fact that the g_{fs} of a FET controls its power gain to a high degree, and is inversely proportional to the temperature, makes the FET less suitable for unsaturated long pulse applications. Flat top pulses may be difficult to achieve due to the instantaneous heat generated in the channel, which causes the power gain of the FET to be reduced during the pulse period. This results in a decay of the pulse amplitude toward its trailing edge, which might prove harmful at pulsewidths longer than 0.5 – 1.0 ms. Pulse shape compensation is possible by adjusting the input drive or gate bias during the pulse, but depending on the specifications this may require complex circuitry. The BJTs are much more stable with their power gain versus temperature slope. In fact the gain can be controlled by adjusting the values of the emitter ballast resistors and the h_{FE}. The common base circuit configuration is the most common for pulsed circuits since their main use is at microwave frequencies. The FETs are mostly used in common source circuit configuration and at frequencies through UHF in saturated applications, or where the pulse shape is less critical.

We can conclude by noting that both types of RF power semiconductors discussed have their own advantages and disadvantages. Although the circuit design with each is similar, FETs and bipolar transistors will have optimum configurations for different applications, frequency ranges and operating voltages. The FET being a newcomer as a power semiconductor will likely go through new and revolutionary developments in the near future, in a manner similar to the evolution in BJTs with the introduction of emitter ballasting.

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