AN1532

Using the Motorola MRFIC1806/1807 Dual Demonstration Board

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DESCRIPTION

The MRFIC1806/1807 Dual Demonstration board (hereafter referred to as the "dual board"), combines Motorola's MRFIC1806 Driver/Ramp IC and the MRFIC1807 PA/Switch IC on a common evaluation board. Together, these two ICs form a system solution for the 1.9 GHz DECT transmit power amplifier and transmit/receive (T/R) antenna switch. The functionality includes a 3.6 V three–stage power amplifier, bias circuits for single–point control, transmit burst shaping to meet the DECT requirement, and a T/R switch. Digital control pins for the T/R switch and ramp circuit are compatible with 3 V CMOS logic levels. Also included on the board are a 900 MHz filter at the PA RF IN port to trap VCO fundamental feedthrough, a low–pass filter at the ANTENNA port to attenuate harmonics, and a MOSFET battery switch. A photograph of the dual board is shown in Figure 1. A complete schematic is shown in Figure 2. The dual board allows evaluation of system level transmitter performance specifications including:

- Transmit power versus time response (attack time, NTP, and release time)
- Adjacent channel interference
- Out of band emissions when transmitting
- Emissions between bursts
- Supply current

In the receive mode, T/R switch performance can be evaluated. Finally, the last section describes how the dual board can be modified for PHS applications.

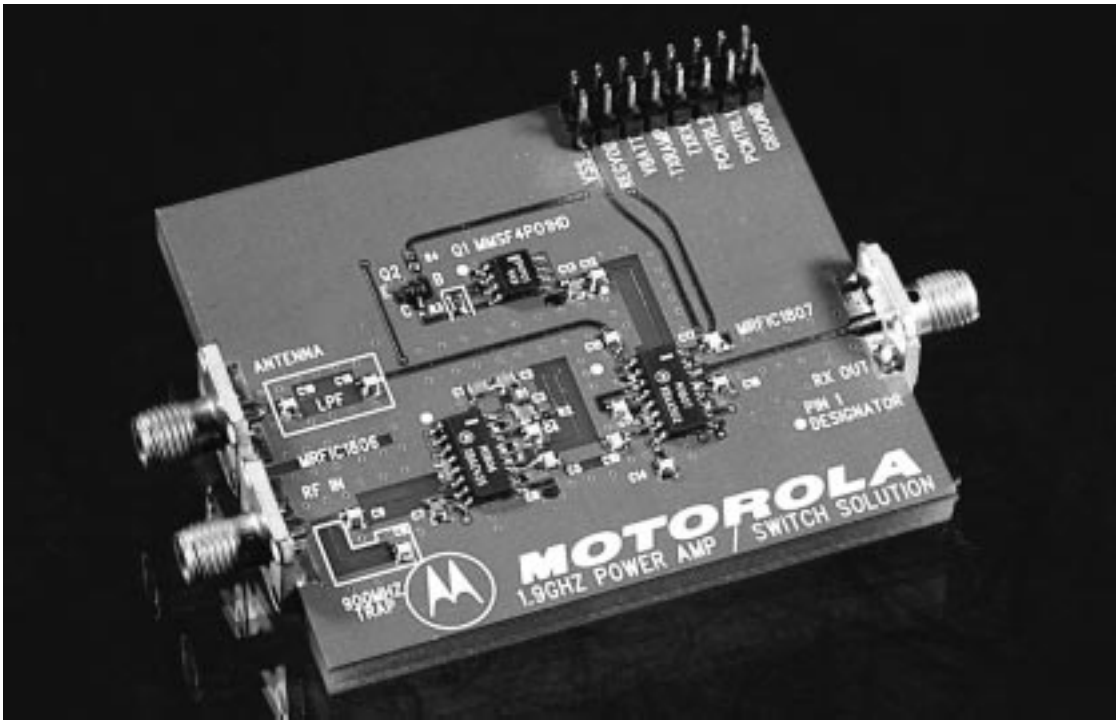


Figure 1. Dual Board Photogragh

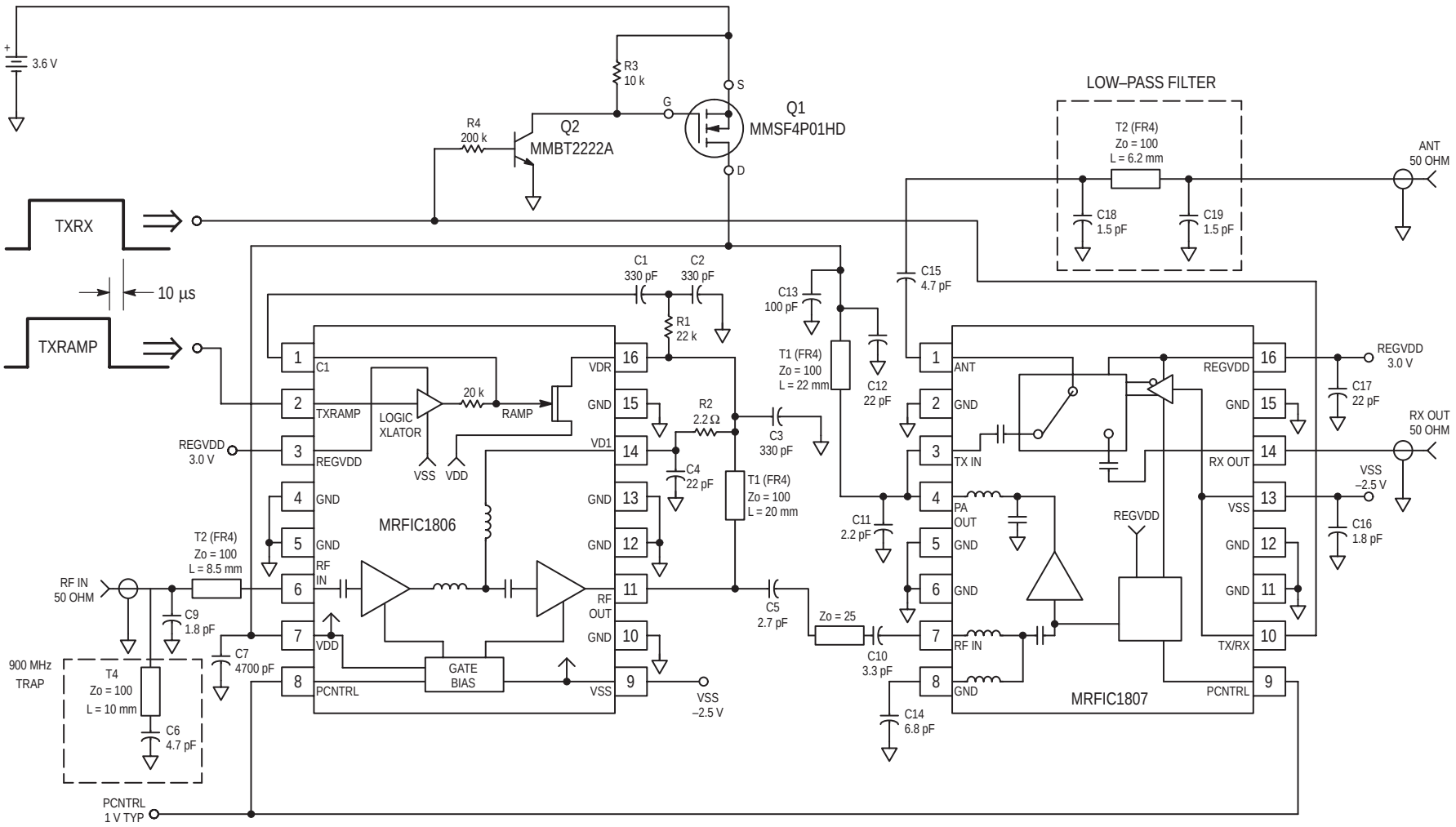


Figure 2. Dual Board Schematic and Part List (DECT Application)

REF DES	VALUE	FUNCTION
C1, C2	330 pF	Ramp ckt rise/fall time
C3	330 pF	RF bypass
C4, C12, C17	22 pF	RF bypass
C5	2.7 pF	1806 RF output match
C6	4.7 pF	900 MHz trap (optional)
C7	4700 pF	Video bypass
C9	1.8 pF	1806 RF input match
C10	3.3 pF	1807 RF input match
C11	2.2 pF	1807 RF output match
C13	100 pF	RF bypass
C14	6.8 pF	1807 900 MHz trap (optional)
C15	4.7 pF	1807 ANT port tuning/dc block
C16	1.8 pF	RF bypass
C18, C19	1.5 pF	ANT low–pass filter (optional)
R1	22 kΩ	Ramp ckt rise/fall linearity
R2	2.2 Ω	1806 UHF stability
R3	10 kΩ	MOSFET pull–up
R4	200 kΩ	TXRX inverter
Q1	MMSF4P01HD	Battery switch
Q2	MMBT3904	TXRX inverter

To evaluate the dual board in the transmit mode, apply the following dc voltages and RF power.

SUPPLY	VOLTAGE	CURRENT	PURPOSE
V_{SS}	–2.5 V	0.6 mA	Negative supply
$REGV_{DD}$	3.0 V	0.6 mA	Logic circuits, T/R switch bias
V_{BATT}	3.6 V (typ)	250 mA	3–stage PA supply

Normally the negative supply (V_{SS}) should be applied before V_{BATT} is applied, otherwise, the three–stage PA would draw excessive current. However, on the dual board the MOSFET switch prevents battery voltage from being applied to the PA when the TXRX control line is low. Next, apply the voltages below to the control lines.

There are two PCNTRL lines on the dual board, PCNTRL1 and PCNTRL2. PCNTRL1 control bias for the 1806 driver stages. PCNTRL2 controls PA bias for the 1807. **The PCNTRL circuits in both ICs have been designed such that the two lines can be tied together for a DECT application. Therefore, only one power control line is needed for transmitter output power adjustment.**

For systems such as PHS that employ linear modulation, it might be desirable to bias PCNTRL2 slightly higher than PCNTRL1. Higher bias on PCNTRL2 will cause the 1807 to operate closer to Class A resulting in improved linearity. Finally, connect a power meter or spectrum analyzer to the ANTENNA connector, terminate the RX OUT connector, and apply –3 to 0 dBm to the RF IN connector. Adjust the PCNTRL voltage for the desired output power. Typical output power and supply current versus PCNTRL is shown in Figure 3. Note that the output power from the 1807 ANT pin (pin 1) is 0.7 dB higher than measured due to line loss (0.3 dB) and low–pass filter loss (0.4 dB) on the dual board.

CONTROL	VOLTAGE	CURRENT	PURPOSE
TXRAMP	3 V	50 μA	1806 ramp control
TXRX	3 V	250 μA	T/R switch control, MOSFET on/off
PCNTRL	1.4 V (typ)	30 μA	PA bias adjust

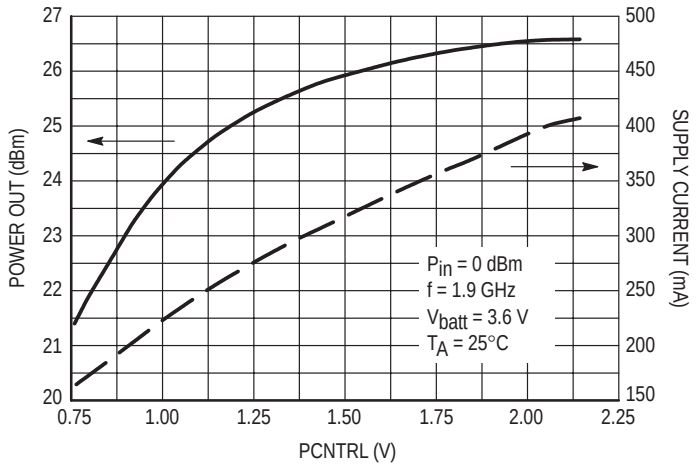
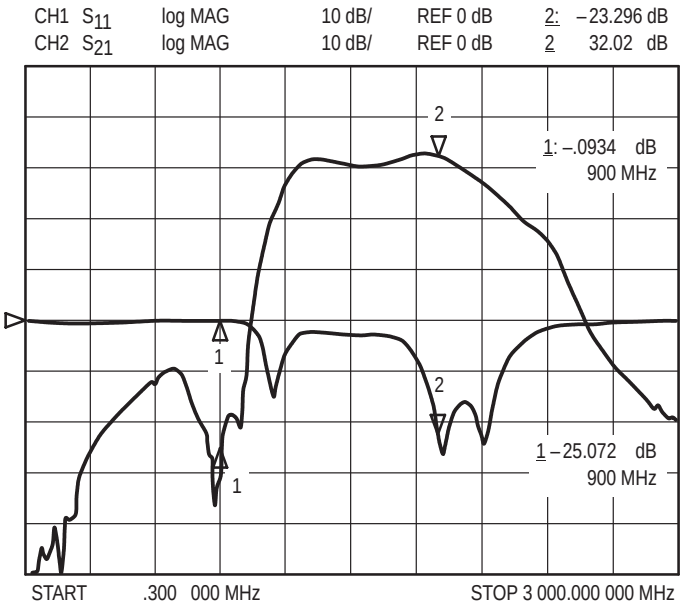
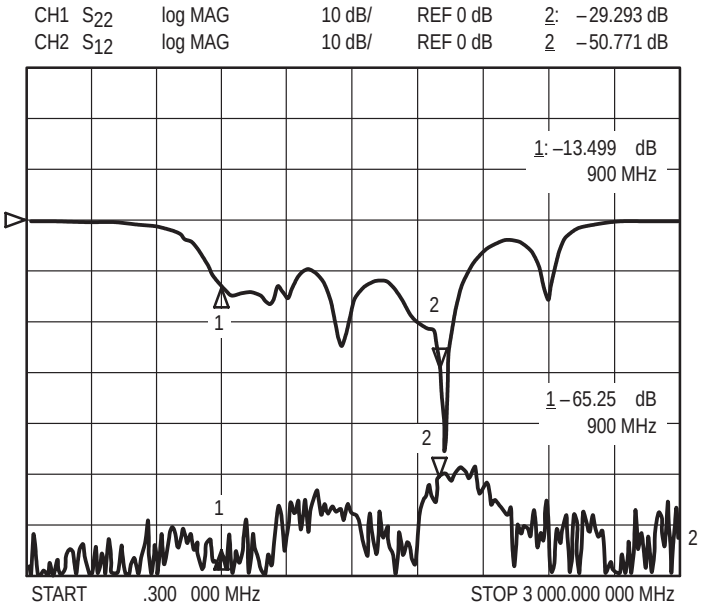


Figure 3. Typical Transmit Mode RF Output Power and Supply Current versus PCNTRL

Measured transmit mode small–signal performance (S11, S21, S12, S22) from RF IN to ANTENNA connectors is shown in Figures 4(a) and 4(b). PCNTRL was set for I_{BATT} = 300 mA before measuring small–signal performance. The roll–off above 2 GHz is primarily due to the low–pass filter on the dual board. The notch at 900 MHz is due to the 900 MHz trap at the RF IN port on the dual board.



(a) Small–Signal Gain (S21), Input Return Loss (S11)



(b) Reverse Isolation (S12), Output Return Loss (S22)

Figure 4. Transmit mode small–signal gain, return losses and reverse isolation. Port 1 is RF IN connector. Port 2 is ANTENNA connector. T_A = 25°C.

TBURST MODE TRANSMIT OPERATION

To evaluate the burst response in the transmit mode, apply the correct digital control signals to the TXRAMP and TXRX control lines. When high (3 V), TXRX enables the MOSFET switch which applies battery voltage to the 1806 V_{DD} (pin 7) and the PA portion of the 1807 (pin 4). TXRX also places the T/R switch of the 1807 in the TX mode. When TXRAMP transitions from 0 V to 3 V, the ramp circuit of the 1806 applies drain voltage to the first and second stage of the driver amplifier through pins 14 and 11, respectively. The drain voltage ramp rate at VDR (pin 16) for the two driver stages is controlled by the value of the external components C1, C2, and R1. C1 and C2 are normally of equal value. R1 adjusts the symmetry of the rise and fall characteristic. For C1, C2 = 330 pF and R1 = 22 kΩ, output power from the 1806 ramps up and down in 10 μs with greater than 40 dB dynamic range. Decreasing the value of C1 and C2 will reduce the ramp up/down time. If C1 and C2 were omitted, the output power from the 1806 would ramp up and down in less than 1 μs.

The rising edges of TXRX and TXRAMP are coincident as shown in Figure 6(a). The falling edge of TXRAMP precedes the falling edge of TXRX by 10 μs as shown in Figure 6(b). Measured burst output power versus input power, with PCNTRL as a parameter is shown in Figure 5. **The graph suggests that for a DECT application, where transmit power at the antenna may not exceed 24 dBm, the optimum PA input power is approximately –3 dBm.** At this RF input level, the PCNTRL pins have sufficient capability to allow output power adjustment at the time of radio manufacturing. The output power shown in Figure 5 is measured at the ANTENNA connector on the dual board. The output power from pin 1 of the 1807 is 0.7 dB higher than measured due to line and filter losses on the board.

The dual board was tested with the following conditions to approximate performance in a DECT application:

V_{BATT} = 3.6 V, V_{SS} = –2.5 V, REGV_{DD} = 3.0 V, Frequency = 1.9 GHz

TXRAMP: Period = 10 ms, Pulse Width = 405 μs

TXRX: Period = 10 ms, Pulse Width = 415 μs (Duty Cycle ≈ 1/24).

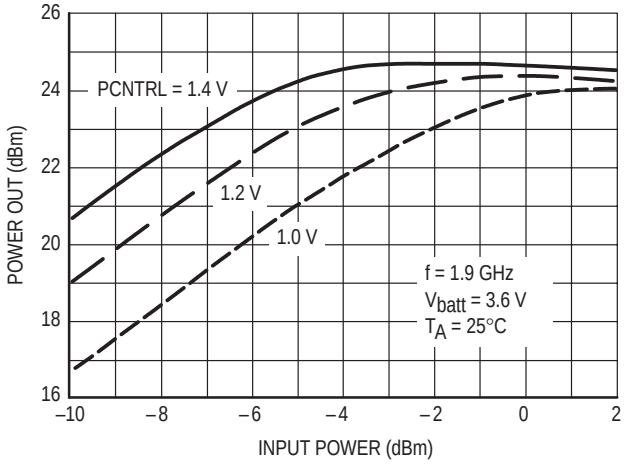
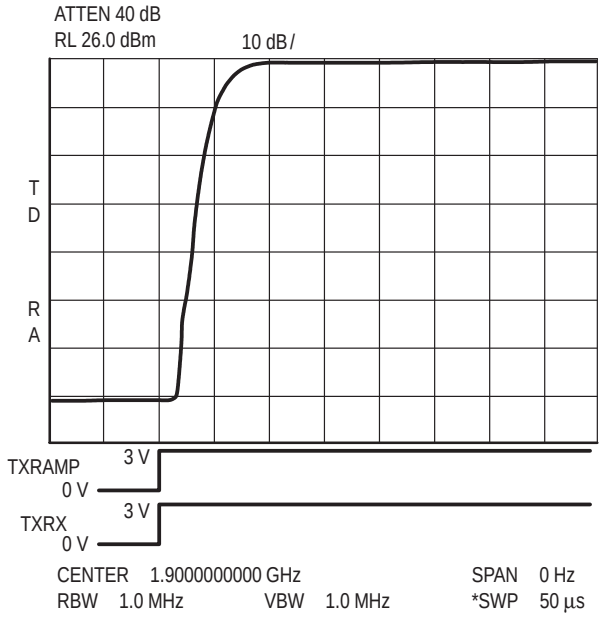
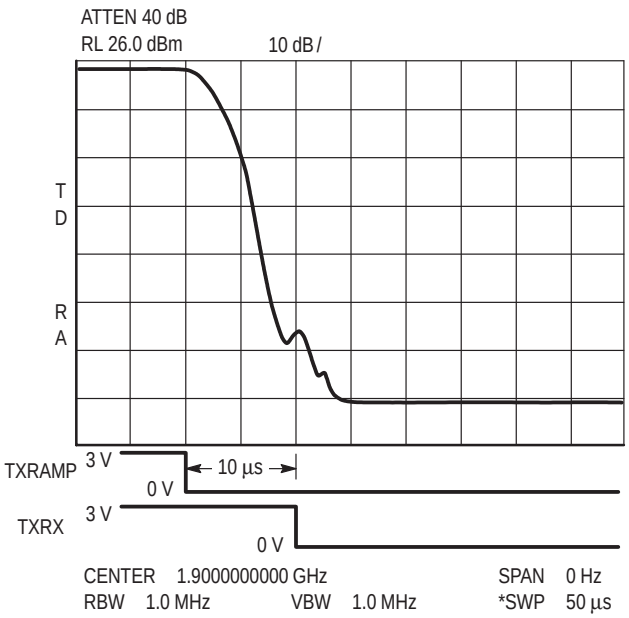


Figure 5. Burst Mode Output Power versus Input Power

Measured output power versus time for the “ramp–up” and “ramp–down” portions of the burst are shown in Figures 6(a) and 6(b), respectively. An HP8563 spectrum analyzer set for zero–span was used for the measurement. The TXRAMP signal was used to externally trigger the spectrum analyzer sweep.



(a) Output Power versus Ramp–Up Time (Horizontal: 5 µs / Division, Vertical: 10 dB / Division)



(b) Output Power versus Ramp–Down Time (Horizontal: 5 µs / Division, Vertical: 10 dB / Division)

Figure 6. Transmit Mode Output Power versus Time

ALTERNATIVE RAMPING SCHEMES FOR HIGHER OUTPUT POWER OR BASEBAND RAMPING

The dual board burst mode burst performance and circuit implementation discussed in the previous sections focused on applications where TDMA ramping will be developed at the power amplifier for antenna output power up to 24 dBm. Some applications require more output power or do not need ramping at the power amplifier due to burst shaping at baseband. Higher output power may be required to overcome additional loss between the PA and the antenna or may be desired as part of system specifications other than DECT.

A simple modification to the 1806 ramp circuit, as shown in Figure 7, will yield about 1.5 dB more burst output power. This change is effected by disabling the on–chip logic translator, adjusting the values of C1, C2, and R1, and supplying a level–shifted control signal through a 2 kΩ resistor connected to pin 1. Logic translation can be accomplished with a PNP transistor followed by an NPN emitter follower. Alternatively, a low current op amp could be used as an integrating comparator to set the rise and fall time and the output is applied to pin 1 with C1, R1 and R2 removed.

Some TDMA implementations have the burst shaping integrated into the baseband encoder. For such realizations, the TXRAMP signal is absent and pin 1 is pulled up to V_{DD}. The power amplifier is now turned on and off by the TXRX signal alone and must linearly amplify the upconverted baseband signal. Generally, the amplifier must back–off from full saturated output power to avoid spectral regrowth.

A comparison of the dual board output power versus input power for internal versus external logic translators is shown in Figure 8.

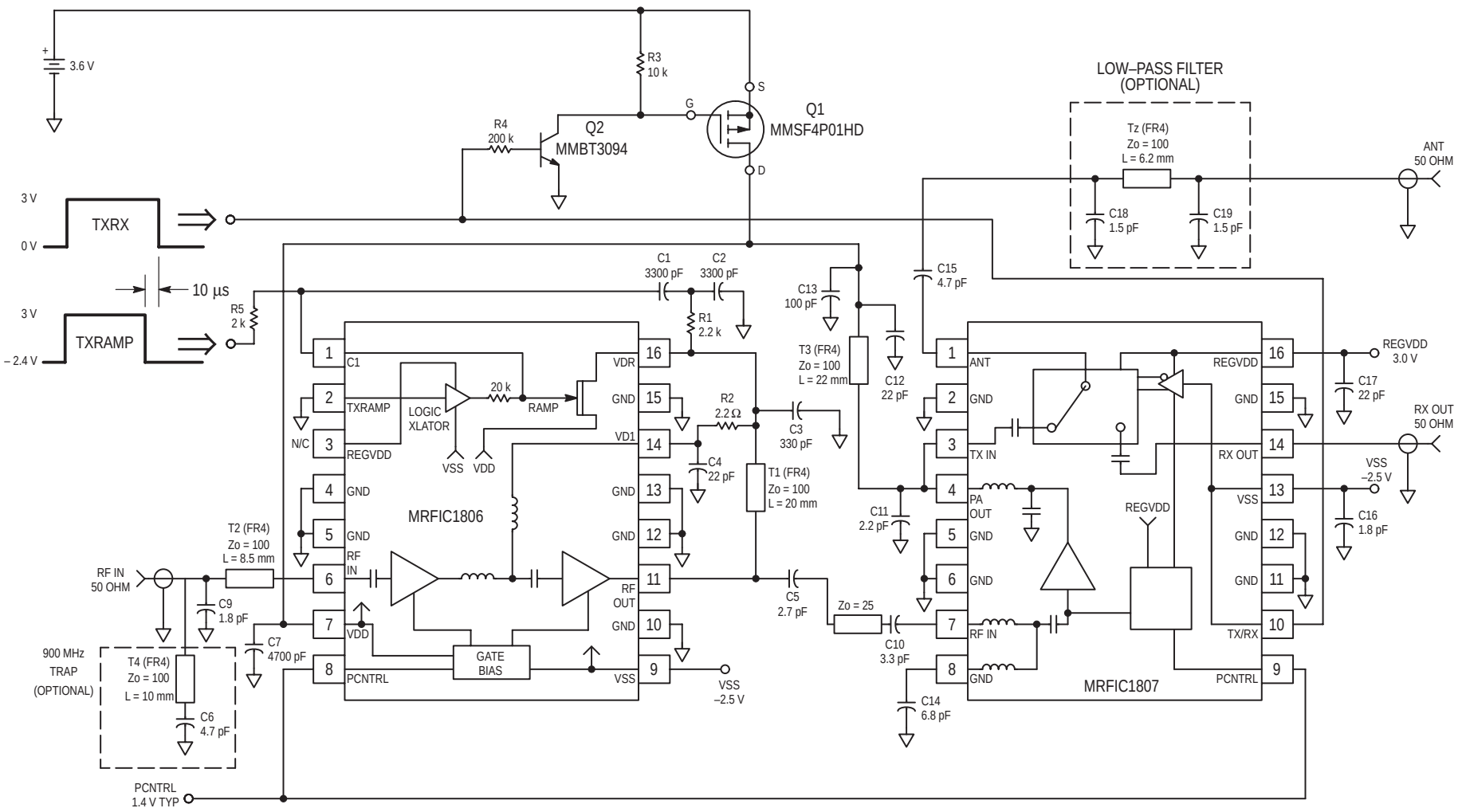


Figure 7. Modified Dual Board Schematic for Higher Burst Output Power (DECT Application)

REF DES	VALUE	FUNCTION	REF DES	VALUE	FUNCTION
C1, C2	330 pF	Ramp ckt rise/fall time	C14	6.8 pF	1807 900 MHz trap (optional)
C3	330 pF	RF bypass	C15	4.7 pF	1807 ANT port tuning/dc block
C4, C12, C17	22 pF	RF bypass	C16	1.8 pF	RF bypass
C5	2.7 pF	1806 RF output match	C18, C19	1.5 pF	ANT low–pass filter (optional)
C6	4.7 pF	900 MHz trap (optional)	R1	22 kΩ	Ramp ckt rise/fall linearity
C7	4700 pF	Video bypass	R2	2.2 Ω	1806 UHF stability
C9	1.8 pF	1806 RF input match	R3	10 kΩ	MOSFET pull–up
C10	3.3 pF	1807 RF input match	R4	200 kΩ	TXRX inverter
C11	2.2 pF	1807 RF output match	Q1	MMSF4P01HD	Battery switch
C13	100 pF	RF bypass	Q2	MMBT3904	TXRX inverter

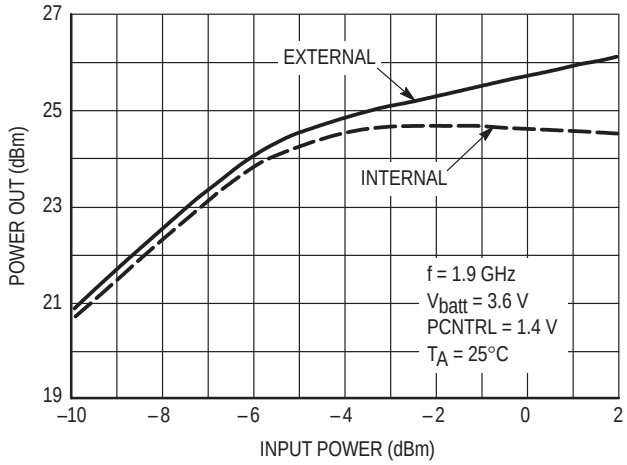


Figure 8. Burst Mode Output Power versus Input Power Using External and Internal Logic Translators

TRANSMIT MODE SUMMARY

Two methods of applying the 1806 to a DECT system have been discussed. The first method implements ramping with the integrated ramp circuit on the 1806. The second method uses an external logic translator to drive the ramp circuit for higher transmit power. The output power capability of both techniques is summarized below.

	INPUT POWER	OUTPUT POWER
Method 1 (internal translator)	–3 dBm	24.8 dBm (25.5 dBm from pin 1 of 1807)
Method 2 (external translator)	+2 dBm	26.1 dBm (26.8 dBm from pin 1 of 1807)

RECEIVE MODE OPERATION

To evaluate the receive path characteristics of the dual board, set the TXRX control pin to logic 0 (less than 0.2 V). On the dual board, this control line simultaneously disables the MOSFET battery switch and places the T/R switch in the receive mode. $REGV_{DD}$ (3 V) and VSS (–2.5 V) are required to operate the T/R switch in the receive mode. V_{BATT}, PCNTRL, and TXRAMP have no effect.

Insertion loss measured from the ANTENNA connector to the RX OUT connector is shown in Figure 9. The plot shows 1.9 dB insertion loss at 1.9 GHz. The actual switch insertion loss is 1.0 dB after subtracting board losses (0.7 dB ANTENNA side, 0.2 dB RX OUT side). Also shown in the same figure is ANTENNA port return loss.

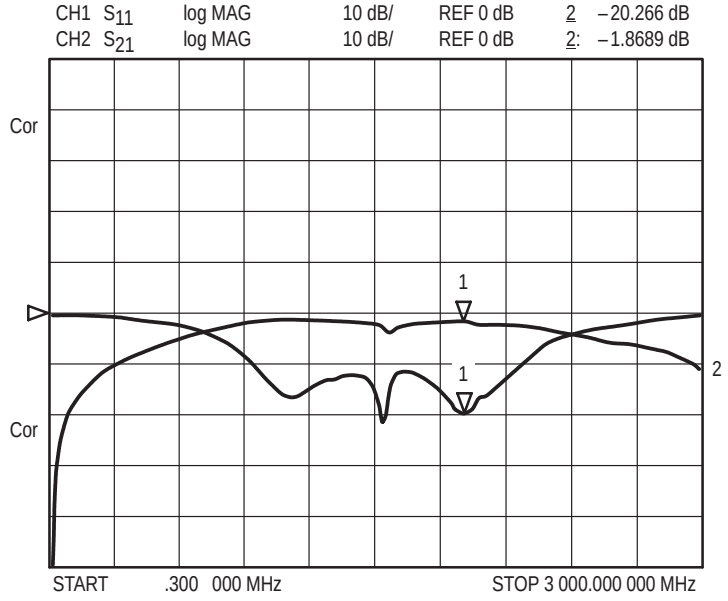


Figure 9. Receive mode small–signal insertion loss and ANTENNA port input return loss. Measurement includes 0.9 dB board loss.

APPLICATION OF THE MOTOROLA MRFIC1806/1807 TO JAPAN PHS

Background

Together, Motorola's MRFIC1806 Driver/Ramp IC and MRFIC1807 PA/Switch IC form a system solution for the power amplifier (PA) and transmit/receive (T/R) antenna switch functions for 1.9 GHz personal communicators. The 1806 includes an integrated ramp circuit for DECT applications, or any other TDMA system employing constant–envelope modulation such as GMSK. In these applications, the 1806 is operated near Class–AB while the 1807 PA stage is operated closer to Class–B for high efficiency. The 1806 ramp circuit shapes the rising and falling portions of the burst by ramping the drain voltages in a controlled manner.

For TDMA systems employing linear modulation such as the $\pi/4$ DQPSK used for Japan PHS, the three power amplifier stages must be biased closer to Class–A to minimize adjacent channel power (ACP) regrowth. The amplifiers are typically operated a few dB below 1 dB compression. In this application, transmit burst shaping is best implemented at IF or baseband. The 1806 ramp circuit would be ineffective due to the lower operating level. Furthermore, ramping the drain voltages would most likely increase ACP.

PHS Application

A schematic of the 1806/1807 dual board modified for a PHS application is shown in Figure 10. On the 1806, the ramp circuit has been disabled by grounding TXRAMP (pin 2) and open circuiting $REGV_{DD}$ (pin 3). C1 (pin 1) is connected to V_{DD} through resistor R1. PA on/off control is achieved with a MOSFET switch in series with the battery. A simple inverter circuit is tied to the TXRX control line and the gate of the MOSFET. When TXRX is high, battery voltage is applied to the three PA stages and the T/R switch is in the transmit mode. When TXRX is low, battery voltage is disconnected from the PA and the switch is in the receive mode.

Biasing

The PCNTRL lines, PCNTRL1 and PCNTRL2, set the bias for the 1806 and 1807, respectively. For linear operation, the 1806 should be biased at 120 mA and the 1807 at 180 mA for 300 mA total. As shown in Figure 11, typical PCNTRL voltages to achieve this bias condition is PCNTRL1 = 1.4 V and PCNTRL2 = 1.9 V. Over temperature, the 1806 bias current has little variation and less than 0.5 dB small–signal gain variation. The 1807 bias increases more significantly over temperature and a compensation circuit would be required. Consult the 1807 data sheet for more information.

Measured Performance with Modulation

The modified dual board shown in Figure 10 has been evaluated for a PHS application.

RF output power versus input power is plotted in Figure 12. Also shown in the same plot is ACP at 600 kHz and 900 kHz offsets. RF input power is measured at the 1806 input, RF output power is at the ANT pin of the 1807. **The results in Figure 12 show compliance to the PHS specification at +21 dBm output from the T/R switch. At this operating level, the 600 kHz ACP was –63 dBc and the 900 kHz ACP was –67 dBc.**

	1806/7 PERFORMANCE	PHS SPECIFICATION
ACP @ 600 kHz offset	–63 dBc	< –50 dBc
ACP @ 900 kHz offset	–67 dBc	< –55 dBc

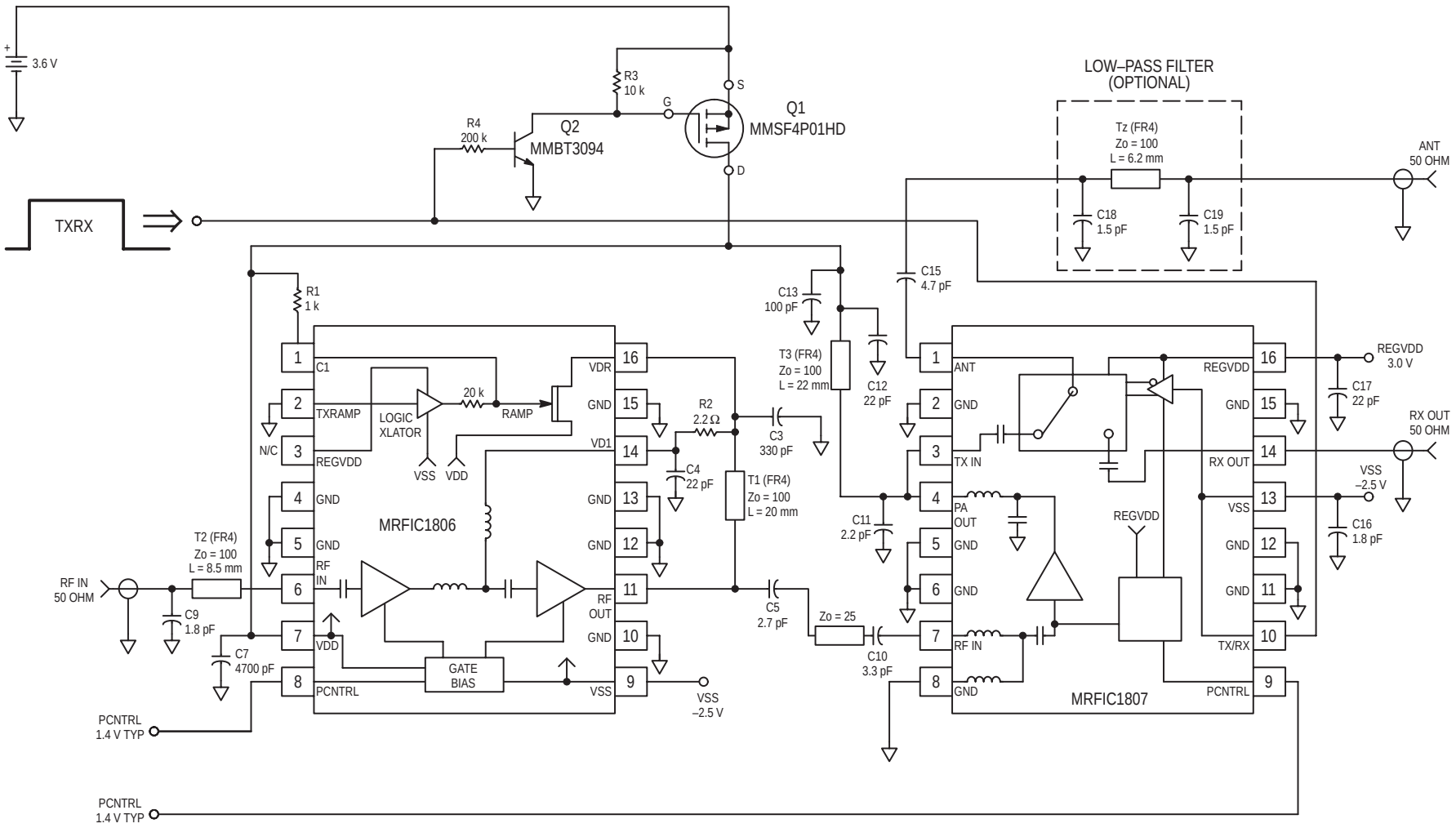


Figure 10. MRFIC1806/MRFIC1807 Schematic and Part List (PHS Application)

REF DES	VALUE	FUNCTION
C3	330 pF	RF bypass
C4, C12, C17	22 pF	RF bypass
C5	2.7 pF	1806 RF output match
C7	4700 pF	Video bypass
C9	1.8 pF	1806 RF input match
C10	3.3 pF	1807 RF input match
C11	2.2 pF	1807 RF output match
C13	100 pF	RF bypass
C15	4.7 pF	1807 ANT port tuning/dc block

REF DES	VALUE	FUNCTION
C16	1.8 pF	RF bypass
C18, C19	1.5 pF	ANT low–pass filter (optional)
R1	1 k Ω	V_{DD} pull–up
R2	2.2 Ω	1806 UHF stability
R3	10 kΩ	MOSFET pull–up
R4	200 kΩ	TXRX inverter
Q1	MMSF4P01HD	Battery switch
Q2	MMBT3904	TXRX inverter

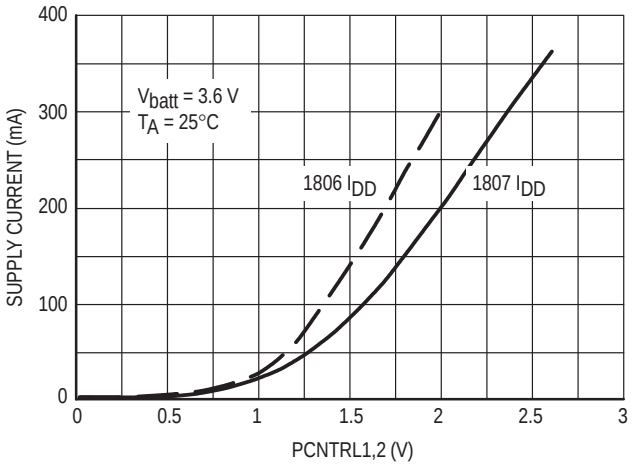


Figure 11. MRFIC1806 and MRFIC1807 Supply Currents versus PCNTRL1 and PCNTRL2 Voltages

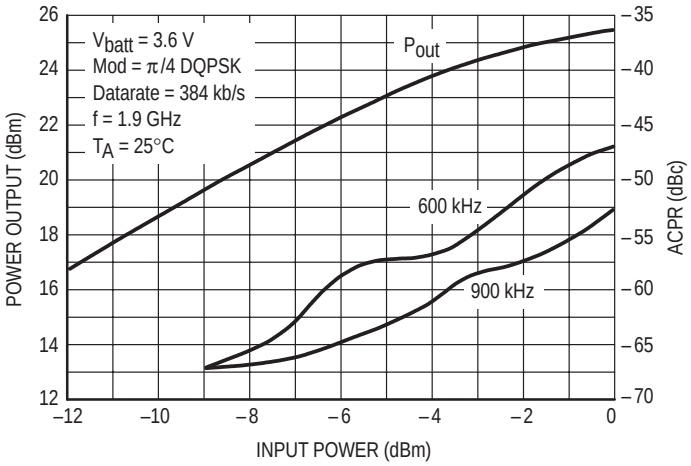


Figure 12. Power Output and Adjacent Channel Power Ratio versus Input Power

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