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Design Considerations of Plastic Ball Grid Arrays for CMOS Gate Arrays

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OBJECTIVE

The purpose of this application note is to familiarize the reader with package characteristics, usage, attachment, and pc board design for the OMPAC (Over-Molded Pad Array Carrier), also known as the plastic ball grid array (PBGA) package. In general, much of this information applies to all BGAs, however, specific attention is given to the styles and distinctions of plastic packages for the CMOS application specific integrated circuits (ASIC) user.

INTRODUCTION

Several BGA type packages are currently available for a variety of semiconductor products. Ceramic pad array packages have been in use for over twenty years with chip to substrate interconnect via wirebond, TAB, and C4. More recently, Motorola extended its pad array carrier technology by substituting Bismaleimide-Triazine (BT) resin epoxy substrates for ceramic, and adding solderballs to form substrate connection points.

This development was initially implemented to enhance portable products with low profile, minimal outline, surface mountable, and cost effective integrated circuits. The first plastic BGAs contained typically less than 80 I/O, and were no larger than 15 mm on a side. Due to the relatively large pitch between solderballs (also called bumps), and self-alignment tendencies during the controlled collapse at reflow, excellent soldering assembly yields are achieved thus making this technology an attractive replacement for fine pitch leaded packages commonly required for high I/O, low cost, moderate power, CMOS ASICs.

For further information regarding many of the topics here, including other BGA configurations, the reader is referred to [1].

1. Characteristics of the Plastic BGA

1.1 BGA Construction

The construction of a PBGA begins with a single layer BT resin epoxy pc board (see Figure 1-1). The die is attached to a gold plated surface on the topside of the board with a silver filled epoxy. Conventional plastic transfer molding encapsulates the die. Interconnection between the die and package pc board is through thermosonic gold wire bonding. From there, copper traces are routed to an array of metal pads on the bottom side of the board. Connections from the topside to the bottom side require vias (plated through-holes) which are typically located around the periphery of the board. Recently, substrate designs have included distributed vias such that connection lengths are reduced. Solder bumps (62%SN, 36%Pb, 2%Ag) are partially reflowed to the electroplated Ni/Au pads to provide the package connection points.

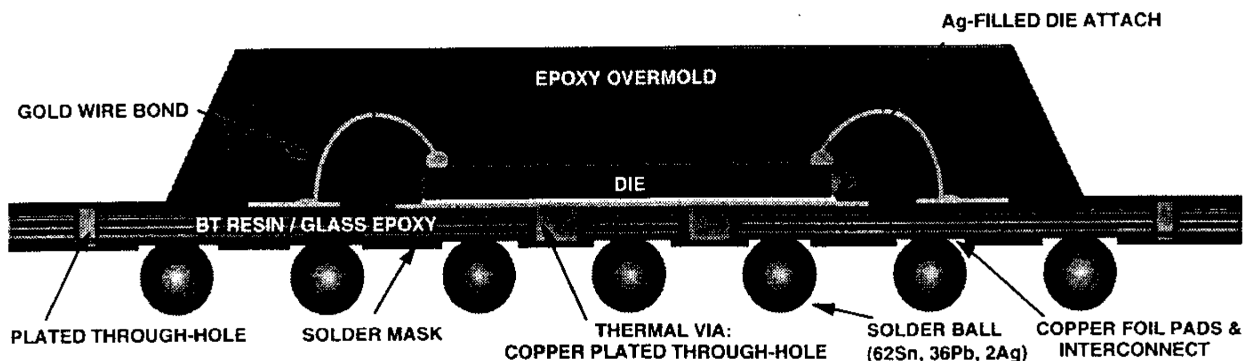

Figure 1-1 Typical Plastic BGA Cross-Sectional View

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For increased heat dissipation, PBGAs employ thermal vias (copper plated-through holes) directly beneath the die. Copper foil on the bottom of the package substrate distributes the heat to several solder balls which ideally are connected to the system pc board ground plane(s). PBGAs can meet or exceed the heat dissipation capability of thermally enhanced QFPs when connected in this manner (see section 2.2).

Possibly the largest strength and weakness of the BGA package is derived from its array configuration. On the positive side, no pins means most problems caused by lead coplanarity and skew are eliminated. Screen printing and placement tolerances are well within the capability of today's production equipment. Achieving high lead counts without fine pitches or large footprints make PBGAs easy to manufacture while providing a space savings. On the other hand, the nature of any area-leaded device creates a large distribution of lead inductances, increased system board routing complexities, and hidden solder joints beneath the package.

Many of the potential disadvantages are often not a problem when closely observed. For instance, PBGAs with up to 400 bumps often use either a standard 1.5 or 1.27 mm pitch allowing enough space for vias inside the footprint next to pads. To keep board layers at a minimum, PBGA power and ground leads are primarily towards the center of the package, thus easing signal escape. A two signal-layer pc board is sufficient for routing most common PBGAs. To solve the inspectability issue, process control coupled with low BGA solder joint defects (<0.5 ppm/j possible) should eliminate the need for 100 percent inspection. Reliability studies done at Motorola regarding the controlled collapse solder joint suggest that electrical test is a sufficient indicator of yield and reliability.

1.2 Plastic BGA Standards

Plastic BGAs up to 503 pins and body sizes measuring up to 40 mm on a side are in use today. JEDEC standards have been established for the Plastic Ball Grid Array. Body sizes range from 7 to 57.5 mm square in increments of 2 mm and 2.5 mm for sizes over 35 mm. Lead pitch standards are 1, 1.27, and 1.5 mm. Two of the early popular sizes for ASICs are the 169 (23 mm) and 225 bump (27 mm) packages at a 1.5 mm pitch (see Figure A-2 to Figure A-5). A 35 mm body size was recently introduced with 313 bumps. In order to facilitate system board routing, a 1.27 mm staggered pitch was employed. Additional patterns for the 27 and 35 mm substrates utilize a 1.27 mm pitch with balls only around the outer four rings of the package. This results in 256 and 352 leads respectively.

Table 1-1 contains the plastic BGAs that are currently offered by the Motorola ASIC Division as mechanical samples. These same packages are available with 0.7 to 0.5 micron L_{eff} CMOS gate arrays ranging from 28,000 - 557,000 available gates.

Table 1-1 Plastic BGA Mechanical Samples

Ball Count	Body Size (mm)	Style	Part Number
169	23 x 23	PBGA	SX38ZZ999NQ01
		GTPAC	SX38ZZ999NA01
225	27 x 27	PBGA	SX38ZZ999NS01
		GTPAC	SX38ZZ999NI01
256	27 x 27	PBGA	SX38ZZ999ZP01
		GTPAC	SX38ZZ999SQ01
313	35 x 35	PBGA	SX38ZZ999BL01
		GTPAC	SX38ZZ999BM01
352	35 x 35	GTPAC	SX38ZZ999SR01

For tape and reel samples, add R2 to the end of part number.
Consult factory for daisy chain sample availability.

1.3 Glob-Top Pad Array Carrier (GTPAC)

All ASIC over-molded BGAs are available in a glob-top version or GTPAC. For fastest turn around times, prototype orders are packaged in the GTPAC while production orders are manufactured off-shore in over-molded versions. Future plans are to migrate many of the PBGAs towards GTPAC for production orders.

2. PBGA Electrical and Thermal Performance

2.1 Electrical Performance

Simultaneous switching noise, crosstalk and propagation delay will affect the electrical performance of a package. Due to the small size of a PBGA the parasitics are reduced, and thus, electrical performance is generally superior to that of comparable pin count PQFPs.

2.1.1 Power and Ground Path Inductance

The power (or ground) net self inductance is the most sensitive element of package parasitics associated with simultaneous switching noise. As output driver speeds increase, shorter rise and fall times create larger current surges on the power and ground distribution nets [2]. Single-layer double-sided PBGAs can provide very low power and ground inductance paths. This is achieved by designing the die attach substrate, ground, and power wirebond pads to form large metal features. Several ground or power wirebonds from the die may be attached to a metal feature typically in the form of rings, see Figure 2-1. These top-side rings have several vias through the substrate to form a direct connection to bottom-side metal islands. These islands are masked

to form pads for solder ball attach. It is not uncommon that a power or ground ring could have 20 to 30 wirebond connections and just 9 to 18 solder balls. Therefore, power and ground lead inductance is then reduced to mostly a parallel combination of several wirebonds, since its path to the device leads is just the thickness of the substrate and solder balls. As a results, the net power and ground inductances are typically less than 1 nH for any BGA designed with these features.

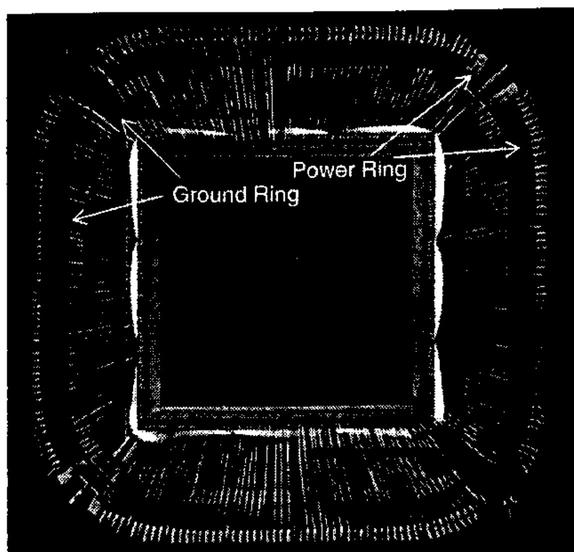

Figure 2-1 225 PBGA Substrate Showing Power and Ground Rings (soldermask is covering non-contact points on the power ring)

An example of this application can be seen by examining a 225 lead package designed for the H4C086, an 86,000 gate CMOS array. The die has 200 signal leads and 56 power and ground pads, all of which can be bonded into an improved 225 lead package. This is achieved by using a common ground metal feature which is a square that encompasses the entire die flag. Attached to the square are finger shaped metal traces that project out from the die flag towards the signal wirebond ring to form 29 wirebond pads. This metal feature is connected to an underlying metal island in the shape of a diamond. Thirteen solder balls are attached to this island thus composing the ground and thermal via connections to the system pc board. Power connections are done in a similar manner with four separate triangle shaped metal features each connecting six to eight (total of 27) wirebond pads to three solder balls. Thus a total of 56 (29 ground and 27 power) die pads are connected to 25 solder balls.

These parallel wires result in a lead equivalency to a QFP of much higher pin count. The number of power and ground leads required to satisfy simultaneous switching of outputs is reduced by approximately 25%. Therefore, an improved design 225 PBGA is roughly equivalent electrically to a much larger fine-pitch 240 QFP (32-mm body, 0.5-mm pitch), which has 207 I/O and 33 power/ground. It is clearly superior to the 208 QFP which would allow only 175 I/O once the 33 power/ground lead requirements were met.

Capacitance differences are only minor, with no signal pins larger than 1pF. There are, however, no long runs of parallel leads as in a QFP lead frame, reducing the potential for coupling across adjacent leads.

2.1.2 Signal Inductance

The area connection of BGAs allow shorter paths, on average, than perimeter connection QFPs. While the worst-case lead inductance of a PBGA may be larger than a comparable pin-count QFP, the distribution is highly skewed to the low end of the range, often resulting in one-half of the leads having lower inductance than a comparable QFP, see Table 2-1. For instance, a 225 PBGA has signal lead inductance values ranging from 3 to 9 nH, an average of 5.6 nH, and over two-thirds of all leads less than 6 nH.

Table 2-1 Measured Signal Trace Inductance for 169 - 313 PBGAs

Inductance (nH)	169	225	256	313
Lowest	2.46	3.03	1.32	1.84
Highest	7.02	9.02	6.51	9.56
Average	4.43	5.6	3.74	6.31
Die Size (mils/side)	337	391	391	476

Values do not include wirebond inductance (~1nH).

Improvements towards lower inductance and smaller distributions were incorporated in the 35 mm 313 pin PBGA through the use of distributed vias Figure 2-2. Rather than placing all vias around the perimeter of the array, as many vias as possible were located towards the center such that top and bottom side trace lengths were at a minimum. This package, recently designed at Motorola, has signal trace inductances ranging from 1.84 to 9.56 nH with an average of 6.3 nH. The majority of traces fall in the 4 to 8 nH range. Compare this to the smaller 225 pin PBGA with all vias located around the periphery of the substrate. Its signal inductances range from about 3 to 10 nH with the majority in the 4 to 7 nH range. It can thus be seen that improvements were achieved in the 313 despite increasing the area by 68%.

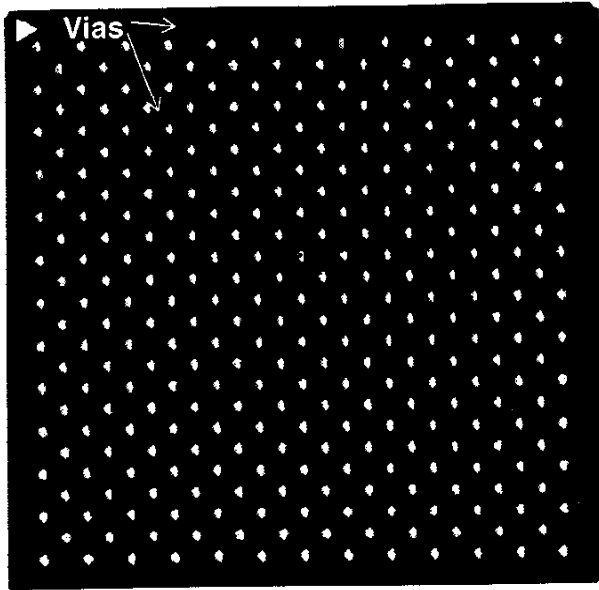

Figure 2-2 313 PBGA with Distributed Vias

2.2 Thermal Performance

The thermal performance of the PBGA is a result of having many parallel heat paths through the substrate and solder balls. However, up to 30% of the heat may be dissipated through the top. This is almost always true for standard PBGAs since the die top-side is always facing up. PBGAs are typically designed with thermal vias (copper plated-through holes) directly beneath the die, see Figure 2-3. Copper foil on the bottom of the package substrate distributes the heat to several solder balls. These balls also act as ground connections to the chip. When these balls are connected to one or more system pc board ground planes, PBGA heat dissipation can exceed the capability of standard QFPs.

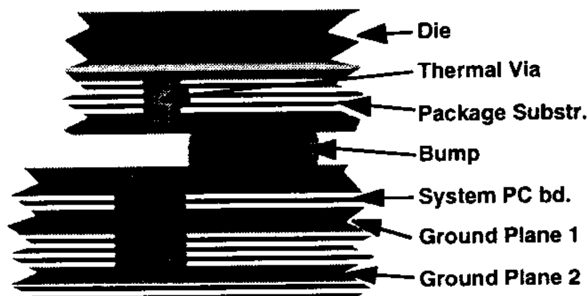

Figure 2-3 PBGA Thermal Via Cross-Section From Die Through Package to System PC Board

Table 2-2 contains thermal resistance (ØJA) values for common QFP and PBGA packages. Ground leads on both packages were connected to each of the 1 mil thick ground planes in the test board. A 20 - 30% improvement is realized when pc board ground planes are connected to the PBGA ground balls. As can be seen, heat dissipation is 10 - 20% better for PBGAs when compared to QFPs having a similar number of leads. In fact, the mere presence of ground planes in the motherboard can result in heat transfer improvement greater than 40% for both packages (free air environment).

Table 2-2 Junction to Ambient ($Ø_{JA}$) Values for Common QFP and PBGA Packages

Package Type	Free Air	100 LFM	200 LFM	300 LFM	500 LFM
160 QFP	28.0	25.7	24.2	23.4	22.5
208 QFP	27.6	25.0	24.2	23.7	23.2
240 QFP	25.0	21.1	19.7	18.9	17.8
169 PBGA	23.9	20.5	19.3	18.6	17.8
225 PBGA	23.1	19.6	18.2	17.4	16.1
256 PBGA	28.7	25.6	24.2	23.3	22.1
313 PBGA	22.2	18.8	17.5	16.7	15.5

1. Die size for the 240 QFP, 256PBGA, and 313 PBGA are 391 $mils^2$. All others are 337 $mils^2$.
2. Modeled data using four-layer test board.

3. BGA to System Board Attachment

3.1 Handling and Placement

Although different from periphery leaded devices in that a PBGA mounting process results from the controlled collapse of solder bumps, it is compatible with most surface mount assembly processes and equipment. Bumping (or attaching solder balls to the package) is performed through reflowing 0.76 mm diameter solder balls into semispherical 0.56 mm high leads. Properly designed PBGAs can be assembled on both sides of a pc board using sequential two sided reflow (one side at a time). The surface tension of the solder will hold the PBGAs on the flip side during the second reflow.

Like most plastic components, molded BGAs are subject to "popcorn" failure and die bond delamination during reflow. The failure process occurs from moisture absorption by the package (especially into the die attachment epoxy), and rapid expansion of moisture during solder reflow. A "popcorned" PBGA can often be seen with the naked eye because the pc board substrate is bulged out under the die region. A study using a 225 pin PBGA with packages exposed to 30 °C and 70% relative humidity resulted in a

weight gain of about 0.15% after 48 hours and 0.21% at 72 hours. Popcorning occurred on parts with 0.24% weight gain while slight delamination occurred at 0.21%. Based on accelerated weight gain evaluations, "popcorning" may occur with as low as 0.18% weight gain. Therefore, it is recommended that parts exposed to more than 48 hours of floorlife be baked in a N_2 purged oven at 125 °C for eight hours.

Package edges can be used as physical or optical placement guides due to the precise alignment of the solder bump array to the package edge. Therefore, device placement is achieved through mechanical centering, package outline vision, or fiducial recognition with upward looking vision. The self-alignment tendency of solder balls during reflow, coupled with the recommended 25 - 30 mil pad diameter allows for placement errors up to 12 mils. Additionally, self-alignment corrects for undersized solder balls and pc board warpage thus lowering defect levels.

3.2 Reflow

The most widely used method of BGA attachment to a pc board is IR mass reflow with 0.2 mm thick solder paste (60Sn/40Pb, 62Sn/36Pb/2Ag, or similar) applied to the full diameter of the pc board pad. However, solder flux, as well as other infrared reflow techniques can also be used. Through using select low residue fluxes, all cleaning processes can be removed from the flow. As with most SMT components, accurate profiling of the oven is critical to yielding good quality solder joints. By using thermocouples attached directly to the BGA solder joints and other locations on the board, the following solder joint characteristics are relevant:

- Maximum temperature < 240 °C
- Above 183 °C (or liquidus) for 60-90 seconds
- Between 210 - 215 °C is best

Typical final solder joint heights of 0.41 mm are realized following a collapse of about 0.15 mm due to the wetting of the pc board solder pad and weight of the package. It is recommended that lines which assemble PBGAs utilize nitrogen atmosphere for reflow.

PBGA mechanical samples with daisy-chain configurations can be useful in establishing a reflow profile and attachment reliability. Typically, the daisy-chain is made by connecting together every other solder pad on the device bottomside as opposed to wirebonding to a daisy-chain die. Electrical testing is achieved by connecting the test board pads together such that a complete loop or net is made. It is possible to make several nets, one connecting the outer row, the second connecting the next row inside, and so on. The daisy-chain configurations available for the 169, 225, and 313 PBGAs are shown in Figure A-1. Included in the figure for the 169 and 225 PBGAs are the suggested pc board connections for making six independent daisy-chain nets.

3.3 Rework

Rework requires component replacement since solder joints are inaccessible. Removal is simplified through dispensing liquid flux underneath the carrier and applying heat (210 - 220 °C) to the topside by positioning a nozzle 1/8" to 1/4" above the component. Once solder has liquefied, pull straight up on the component with a vacuum tip. This procedure does not require board baking prior to rework since neighboring components are not likely to see temperatures above 185 °C, a "safe temperature" that moisture saturated PBGAs can be subjected to. Site preparation requires using a solder wick and soldering iron to remove excess solder on pads. Pads should be cleaned with alcohol and a small brush. Once dried and inspected, a moisture free PBGA may be installed. First, fresh paste flux must be attached to package solder balls. A brass or stainless flux block with a 10 - 14 mil trench works well. Dip the PBGA into the "doctor bladed" flux basin and check that the solder nodules bear flux. Align part to pc board and apply heat (as above) to reflow solder. No flux cleaning is required.
Further information regarding rework can be found in [3] and [4].

4. PC Board Design for PBGAs

Typical FR-4 PCBs are well suited for PBGA mounting. An important parameter for a board material is the coefficient of thermal expansion (CTE). Solder joints proximate to the perimeter of the die fail first in thermal cycling due to increased stresses and strains as the die has a much lower CTE than the PBGA circuit board [5]. Ideally, the package substrate and the motherboard CTEs should be within 2-4 ppm/°C. CTE mismatches as high as 10 ppm/°C have resulted in highly reliable solder joints. A typical BT resin BGA has a CTE of 14 ppm/°C. How close a match should be will depend on the number of on and off cycles, the rate of temperature change during the on and off cycles, and the maximum temperature of the pc board.

Equally important is the system board planarity or warpage. A good target is no greater than 7 mils/inch to assure that all solder balls reach the 0.2 mm high solder paste before reflow. Final board warpage should be kept within 10 mils/inch. It should further be noted that the location of PBGAs on the system board is best kept to areas less prone to warpage during processing.

4.1 PC Board Pad Considerations

The ideal exposed copper land pattern on a pc board is 25 to 30 mils diameter for 1.5 and 1.27 mm pitch BGAs (see Figure 4-1). Soldermask defined (SMD) pads are recommended for increased pad to pc board adhesion strength as well as joint definition. The suggested solder resist overlap coverage is from 5 to 10 mils over the periphery of the metallization. More recently, some users have gone to non-soldermask defined (NSMD) pads to ease motherboard routing as compared to SMD pads. A drawback of the SMD pads approach is that trace routing space is reduced. A standard 25 mil NSMD pad and 6 mil soldermask opening on a 60 mil pitch provides room for three traces and four spaces (both 4 mils). A SMD pad allows only two traces and three spaces. With two traces between pads, the outer three rows of pins may be routed on top layer metal while three traces allow top layer escape of the outer four rows. Pads inside these rows must via to another layer. Although not necessary, larger pads may be used at the corners of the pad array to further ease alignment requirements which may be helpful during hand placement.

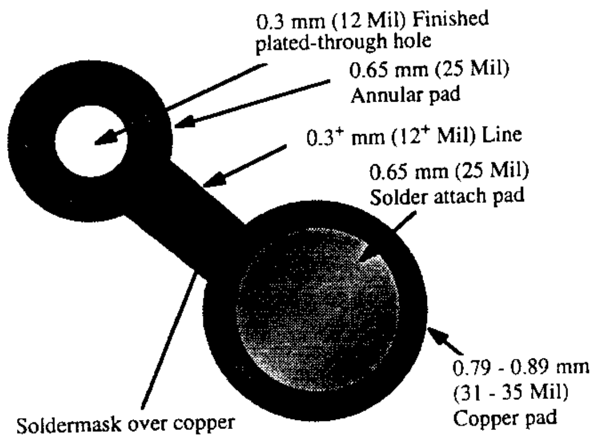

Figure 4-1 Solder Mask Defined Pad with Via

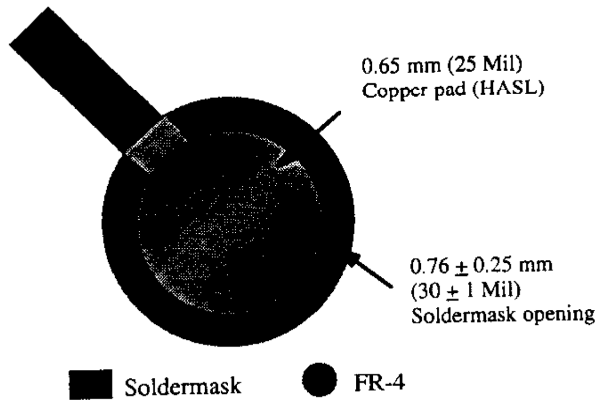

Figure 4-2 Non-Solder Mask Defined

X-ray inspection during the assembly flow development cycle and for subsequent process monitoring is helpful but somewhat limited in providing data. X-ray images looking directly down upon a BGA package attached to an FR-4 pc board may reveal a short between solder balls. With a standard circular pad on the pc board, X-ray viewing indicates only the presence of the solder bump and not whether it has joined the pc board. Solder bumps wetted to non-circular pads create an X-ray image in the shape of the pad thus indicating that the solder joint has been formed. A commonly suggested pad shape is that of a tear drop (Figure 4-3). Another approach is using pc board pads larger than the package pad to verify reflow with X-ray. Although this approach may reduce available top layer pc board traces, reliability studies have shown that the resulting volcano shaped solder joint (wider at the pc board) reduces stress at joint/pad interfaces. Fractures initiated at these interfaces are the primary solder joint failure mechanisms.

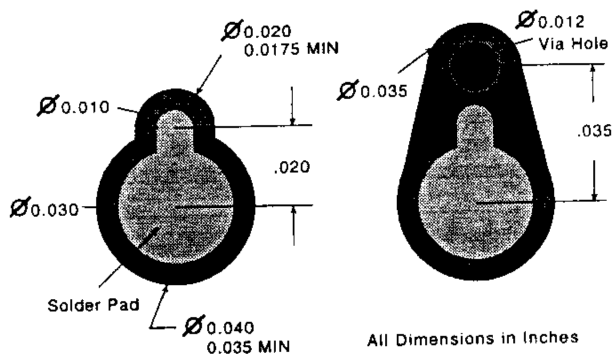

Figure 4-3 Tear Drop Shape Pad for X-Ray Viewing

4.2 PC Board Routing

A physical advantage which may not be readily seen is that of simplified pc board complexity. Fine-pitch QFPs do not allow routing to pass under the component without using a via. BGAs allow up to five traces between 1.5-mm pitch pads (depending on your particular pc board layout rules and pad size). This may simplify bussing from package to package. Routing congestion caused by vias around components is therefore reduced.

All 200 I/O signals in a 225 PBGA can be routed on a two layer board using fairly conservative 8 mil traces and spaces, see Figure 4-4 and Figure 4-5. This is achieved by connecting the center-most 25 power and ground pads through vias to other layers. A total of 112 I/O signals can escape on the top surface while the remaining 88 I/O signals can be routed on the second layer.

A 35 mm square 313 PBGA can also be routed on two layers using no less than 7 mil lines and spaces and a 35 mm pad size. As can be seen in Figure 4-6, 184 pc board top-layer signal I/O escapes are possible through the 1.27 mm staggered matrix ball pattern which allows two 7 mil lines and three 7 mil spaces between solder bump pads. The remaining 96 signal I/O's can be easily routed on a second layer which may also allow power and ground routing or other signals to pass through. If a smaller pad were used, such as 31 or 32 mil, 8 mil geometry would be possible.

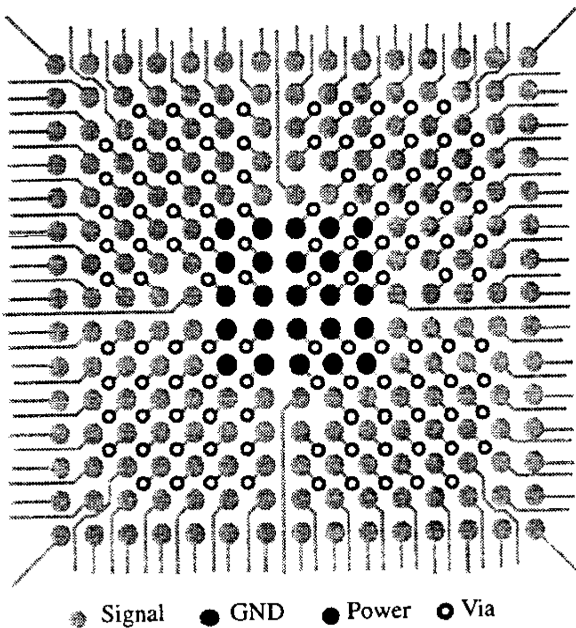

Figure 4-4 PC Board Top Surface Routing for 225 PBGA 112-Signal I/O Escapes

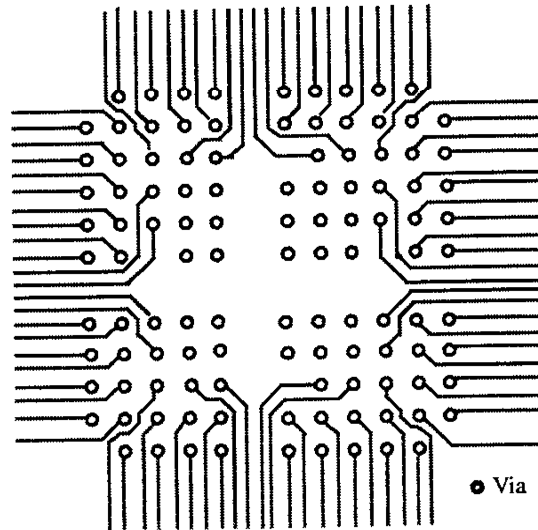

Figure 4-5 PC Board Second Signal Layer Routing for 225 PBGA 88-Signal I/O Escapes

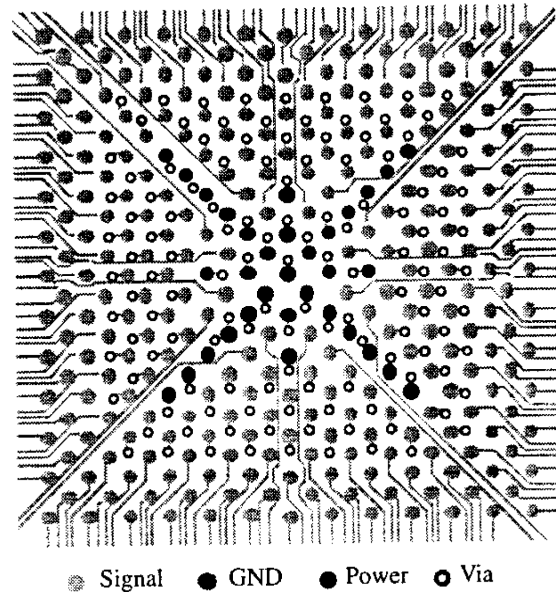

Figure 4-6 PC Board Top Surface Routing for 313 PBGA 184-I/O Signal Escapes

4.2.1 Perimeter PBGAs

Tighter pitch and larger body size PBGAs could force additional signal layers and/or finer geometries. However, some low cost applications which limit the pc board trace widths and board layers may have difficulty accessing all signals in a full array PBGA. Although a standard 225 bump, 1.5 mm pitch PBGA may be routed on two signal layers without

going below 8 mil geometry, tighter pitch and larger body size versions could force additional signal layers and/or finer geometries.

One way to insure all signals can be routed on two signal layers is through the use of a perimeter array pattern which eliminates contacts in the center area of the package. By going to the next smaller JEDEC standard pitch of 1.27 mm, a 27 mm 225 PBGA becomes a 256 PBGA (see Figure 4-7). This perimeter array has four rows of balls around the periphery thus simplifying pc board routing by bringing two rows out on each of the two signal layers. At a 1.27 mm pitch, escape routing requires no finer than five mil traces and can be greater than six mils depending on the pc board pad size.

Other perimeter arrays likely to emerge are a 31 mm square 304 I/O, and a 35 mm square 352 I/O, both on a 1.27 mm pitch. All of the perimeter arrays are likely to have a version that includes a small matrix of solder balls in the center for applications requiring improved thermal dissipation. These thermal/ground balls work in the same manner as their full array counterparts. Perimeter arrays without thermal/ground balls in the center still have thermal vias which connect the die attach to a bottom-side metal island which covers the non-contacted center area of the package. This island contains fingers which connect directly to all inner row ground bumps. Due to the size of the island and the ability to have a larger number of thermal vias, perimeter arrays provide slightly less heat dissipation to that of full array PBGAs without solder balls directly beneath the die. As much as a 20% improvement in thermal performance is possible when perimeter PBGAs incorporate solder balls in the center.

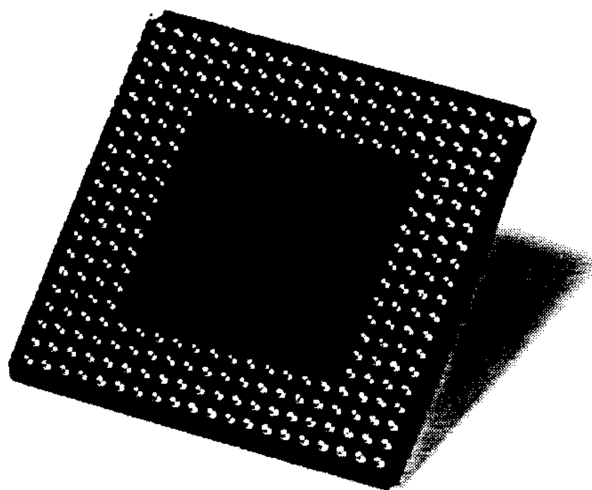

Figure 4-7 256 Lead Perimeter PBGA with 1.27 mm Pitch

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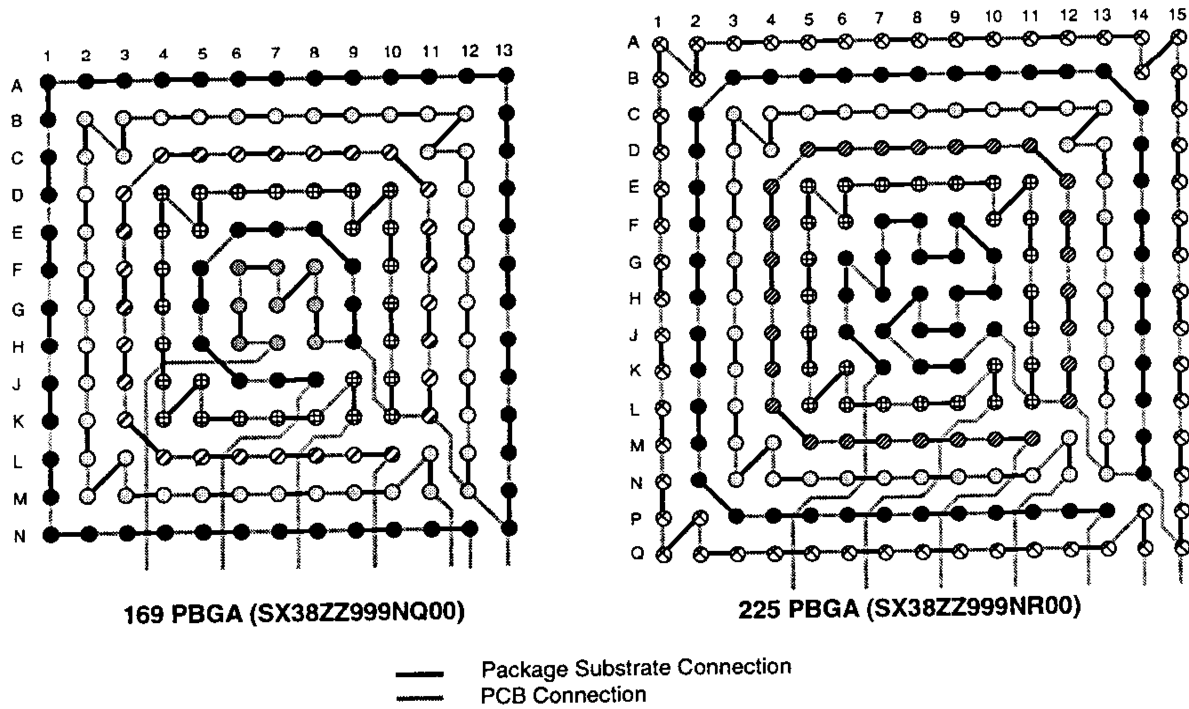
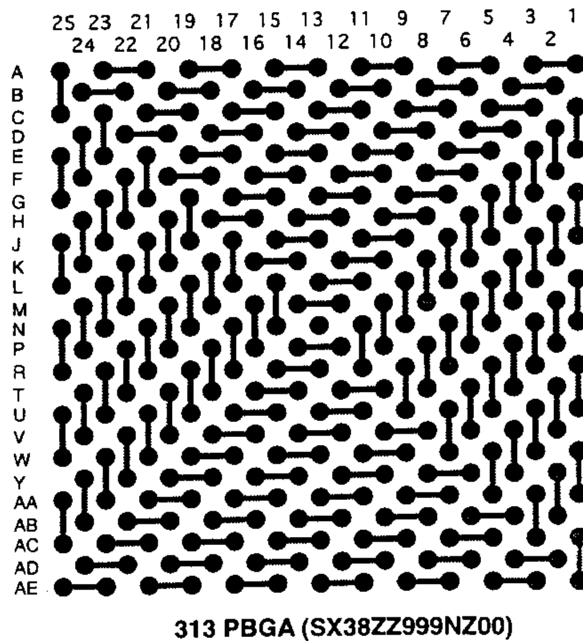
1. APPENDIX



169 PBGA (SX38ZZ999NQ00)

225 PBGA (SX38ZZ999NR00)

Package Substrate Connection
PCB Connection

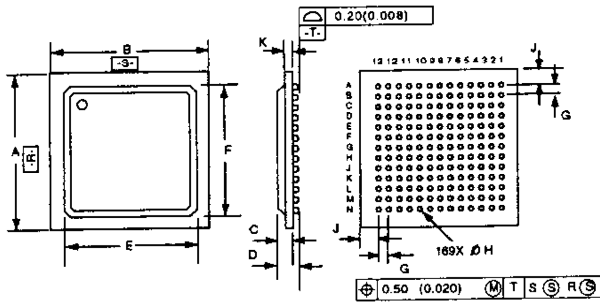


313 PBGA (SX38ZZ999NZ00)

Figure A-1 Plastic BGA Daisy Chain Versions with Suggested PCB Features for 169, 225, and 313 Ball Configurations.

CASE 938

CASE 971-01 GTPAC (used for prototypes only)



Dimensions for OMPAC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.90	23.10	0.902	0.909
B	22.90	23.10	0.902	0.909
C	1.33	1.73	0.052	0.068
D	1.83	2.43	0.072	0.096
E	19.30	19.70	0.76	0.776
F	19.30	19.70	0.76	0.776
G	1.50 BSC		0.0590 BSC	
H	0.690	0.810	0.027	0.032
J	2.400	2.600	0.094	0.102
K	0.310	0.410	0.012	0.016

Dimensions for GTPAC

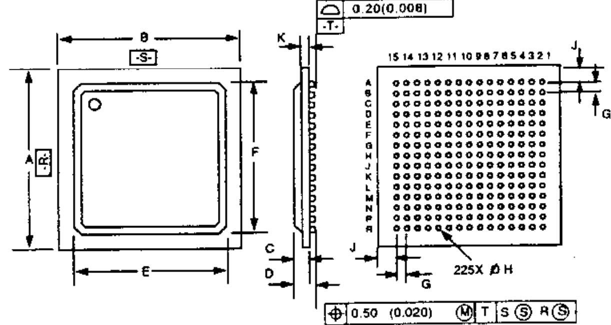
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.90	23.10	0.902	0.909
B	22.90	23.10	0.902	0.909
C	1.526	2.134	0.060	0.084
D	2.026	2.834	0.080	0.112
E	15.300	19.300	0.602	0.760
F	15.300	19.300	0.602	0.760
G	1.50 BSC		0.0590 BSC	
H	0.690	0.810	0.027	0.032
J	2.400	2.600	0.094	0.102
K	0.510	0.610	0.020	0.024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: MILLIMETER

Figure A-2 169 OMPAC and GTPAC Mechanical Drawing

CASE 938A

CASE 970-01 GTPAC (used for prototypes only)



Dimensions for OMPAC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	26.90	27.10	1.059	1.067
B	26.90	27.10	1.059	1.067
C	1.330	1.730	0.052	0.068
D	1.830	2.430	0.072	0.096
E	23.80	24.20	0.937	0.953
F	23.80	24.20	0.937	0.953
G	1.50 BSC		0.0590 BSC	
H	0.690	0.810	0.027	0.032
J	2.900	3.100	0.114	0.122
K	0.310	0.410	0.012	0.016

Dimensions for GTPAC

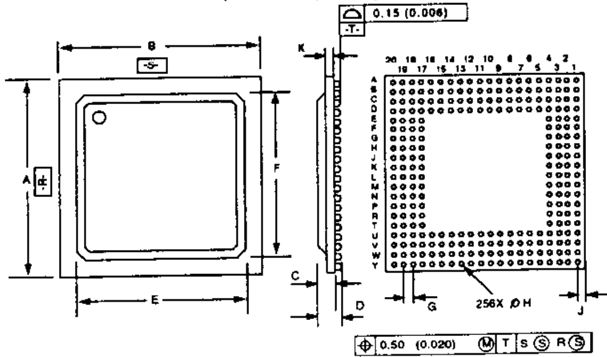
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	26.90	27.10	1.059	1.067
B	26.90	27.10	1.0590	1.067
C	1.526	2.134	0.060	0.084
D	2.026	2.834	0.080	0.112
E	17.78	22.86	0.700	0.900
F	17.78	22.86	0.700	0.900
G	1.50 BSC		0.0590 BSC	
H	0.690	0.810	0.027	0.032
J	2.900	3.100	0.114	0.122
K	0.510	0.610	0.020	0.024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: MILLIMETER

Figure A-3 225 OMPAC and GTPAC Mechanical Drawing

Preliminary

GTPAC (used for prototypes only)



Dimensions for OMPAC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	26.90	27.10	1.059	1.067
B	26.90	27.10	1.059	1.067
C	1.330	1.730	0.052	0.068
D	1.830	2.430	0.072	0.096
E	23.80	24.20	0.937	0.953
F	23.80	24.20	0.937	0.953
G	1.27 BSC		0.50 BSC	
H	0.690	0.810	0.027	0.032
J	1.335	1.535	0.526	0.604
K	0.310	0.410	0.012	0.016

Dimensions for GTPAC

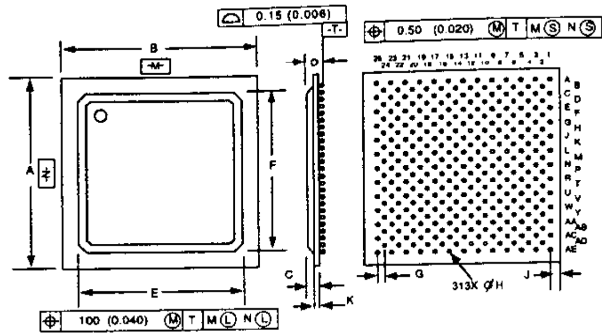
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	26.90	27.10	1.059	1.067
B	26.90	27.10	1.059	1.067
C	1.526	2.134	0.060	0.084
D	2.026	2.834	0.080	0.112
E	17.78	22.86	0.700	0.900
F	17.78	22.86	0.700	0.900
G	1.27 BSC		0.50 BSC	
H	0.690	0.810	0.027	0.032
J	1.335	1.535	0.526	0.604
K	0.510	0.610	0.020	0.024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: MILLIMETER

Figure A-4 256 OMPAC and GTPAC Mechanical Drawing

Preliminary

GTPAC (used for prototypes only)



Dimensions for OMPAC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	34.90	35.10	1.374	1.382
B	34.90	35.10	1.374	1.382
C	1.53	1.93	0.060	0.076
D	2.03	2.63	0.08	0.104
E	29.80	30.20	1.173	1.189
F	29.80	30.20	1.173	1.189
G	1.27 BSC		0.50 BSC	
H	0.690	0.810	0.027	0.032
J	2.260 REF		0.089 REF	

Dimensions for GTPAC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	34.90	35.10	1.374	1.382
B	34.90	35.10	1.374	1.382
C	1.53	2.134	0.060	0.084
D	2.026	2.834	0.080	0.112
E	25.50	29.50	1.004	1.161
F	25.50	29.50	1.004	1.161
G	1.27 BSC		0.50 BSC	
H	0.690	0.810	0.027	0.032
J	2.260 REF		0.089 REF	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: MILLIMETER

Figure A-5 313 OMPAC and GTPAC Mechanical Drawing

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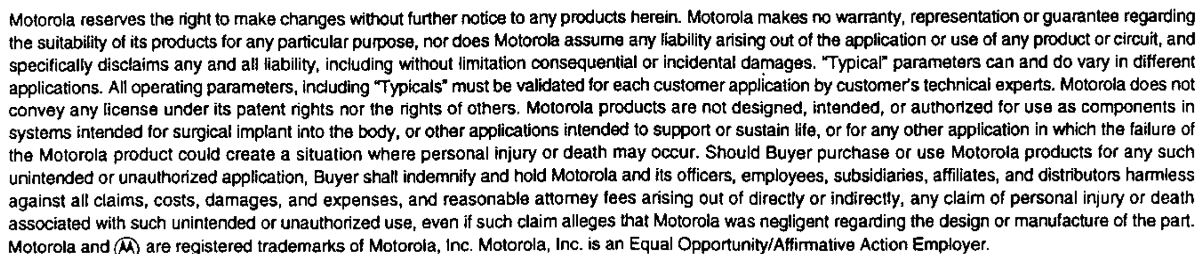
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