AN1545
Application Note

Thermal Data for MPC Clock Drivers

Prepared by
Todd Pearson
Applications Engineering

This application note provides general information on thermal and related reliability issues with respect to the MPC family of clock driver products. In addition, methods are presented to estimate power dissipation and junction temperatures for the MPC product family.

10/96

REV 0

MOTOROLA

Thermal Data for MPC Clock Drivers

Package Choice

The Motorola Timing Solutions products are offered in a variety of surface mount plastic packages. These packages include the 16 and 20 lead SOIC, 20 and 28 lead PLCC and the 32 and 52 lead TQFP packages. The bulk of the newer products are being introduced in the SOIC and TQFP packages with the PLCC being used for the older mature products.

The surface mount plastic packages were selected as the optimum combination of performance, physical size and thermal handling in a low cost standard package. While more exotic packages exist to improve the thermal and electrical performance the cost of these are prohibitive for many applications.

Long Term Failure Mechanisms in Plastic Packages

When analyzing a design for its long term reliability it is important that the dominant failure mechanisms are well understood. Although today's plastic packages are as reliable as ceramic packages under most environmental conditions, as the junction temperature increases a failure mode unique to plastic packages becomes a significant factor in the long term reliability of the device.

Modern plastic package assembly utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. Because plastic packages use injection molding the bond wires used must be extremely ductile to keep from breaking or being pulled from the bond pad during the injection process. Gold wire has far better ductility than aluminum wire and therefore is used in the process of plastic packaging. Aluminum is the metal used in the majority of low cost digital IC processes for transistor and bond wire interconnect. As the temperature of the silicon (junction temperature) increases an intermetallic forms between the gold and aluminum interface. This intermetallic formation results in a significant increase in the impedance of the wire bond and can lead to performance failure of the affected pin. With this relationship between intermetallic formation and junction temperature established, it is incumbent on the designer to ensure that the junction temperature for which a device will operate is consistent with the long term reliability goals of the system.

Reliability studies were performed at elevated ambient temperatures (125°C) from which an arrhenius equation relating junction temperature to bond failure was established. The application of the equation yields Table 1. This table relates the junction temperature of a device in a plastic package to the continuous operating time before 0.1% bond failure (1 failure per 1000 bonds). Note that this equation only holds for continuous elevated junction temperature levels, as the curve is quite steep if a system cycles through a temperature range but spends a relatively short amount of time at the extreme the numbers provided in this table will grossly underestimate the lifetime of the device based solely on the worst case junction temperature seen.

Table 1. Package Junction Temperatures

Junction Temperature (°C)	Time (Hours)	Time (Years)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.1
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

The Motorola Timing solutions products are designed with chip power levels that permit acceptable reliability levels, in most systems, under conventional 500lfpm (2.5m/s) airflow. However because of their flexibility and programmability there may be some situations where special thermal considerations may be required.

Thermal Management

In any system design proper thermal management is essential to establish the appropriate trade–off between performance, density, reliability and cost. In particular the designer should be aware of the reliability implication of continuously operating semiconductor devices at high junction temperatures.

The increasing popularity of plastic, small outline surface mount packages is putting a greater emphasis on the need for better thermal management of a system. This is due to the fact that the newer SMD packages generally require less board space than their first generation brethren. Thus designs incorporating the latest generation SMD packaging technologies have a higher thermal density. To optimize the thermal management of a system it is imperative that the user understand all of the variables which contribute to the junction temperature of the device.

The variables involved in determining the junction temperature of a device are both supplier and user defined. The supplier, through lead frame design, mold compounds, die size and die attach can positively impact the thermal resistance and thus, the junction temperature of a device. Motorola continually experiments with new package designs and assembly techniques in an attempt to further enhance the thermal performance of its products.

It can be argued that the user has the greatest control of the variables which commonly impact the thermal performance of a device. Ambient temperature, air flow and related cooling techniques are the obvious user controlled variables, however PCB substrate material, layout density, amount of exposed copper and weight of copper used in the power planes can all have significant impacts on the thermal performance of a system.

PCB substrates all have different thermal characteristics, these characteristics should be considered when exploring the PCB alternatives. Users should also account for the different power dissipation of the different devices in their systems and space them accordingly. In this way the heat

load is spread across a larger area and “hot spots” do not appear in the layout. Copper interconnect and power planes act as heat radiators, therefore significant thermal dissipation can be achieved by paying special attention to the copper elements of a PCB. The thermal resistance of copper (package leadframes are made from copper) is significantly lower than that of the epoxy used for the body of plastic packages. As a result the dominant mode of heat flow out of a package is through the leads. By employing techniques at the board level to enhance the transfer of this heat from the package leads to the PCB one can reduce the effective thermal resistance of the plastic package. Copper interconnect traces on the top layer of the PCB are excellent radiators for transferring heat to the ambient air, especially if these traces are exposed to even moderate air flow. In addition using thick copper power planes not only reduces the electrical resistance but also enhances their thermal carrying capabilities. The power planes can be thermally enhanced further by employing special edge connectors which draw the heat from the planes and again dissipate it into the ambient. Finally, the use of thermal conductive epoxies between the underneath of a device and thermal vias to a power plane can accelerate the transfer of heat from the device to the PCB where once again it can more easily be passed to the ambient.

The advent of small outline SMD packaging and the industry push towards smaller, denser designs makes it incumbent on the designer to provide for the removal of thermal energy from the system. Users should be aware that they control many of the variables which impact the junction temperatures and, thus, to some extent, the long term reliability of their designs.

Calculating Junction Temperature

Since the reliability of a device is directly related to junction temperature and that temperature cannot be measured directly there needs to be a means of calculating the approximate junction temperature from measurable parameters. There are two equations which can be used:

$$T_J = T_A + PD\Theta_{JA} \text{ or } T_J = T_C + PD\Theta_{JC}$$

where:

T_J = Junction Temperature
T_A = Ambient Temperature (°C)
T_C = Case Temperature (°C)
PD = Internal Power Dissipation of the Device (W)
Θ_{JA} = Avg Pkg Thermal Resistance (Junction – Ambient)
Θ_{JC} = Avg Pkg Thermal Resistance (Junction – Case)

The Θ_{JC} numbers are determined by submerging a device in a liquid bath and measuring the temperature rise of the bath, it therefore represents an average case temperature. The difficulty in using this method arises in the determination of the case temperature in an actual system The case temperature is a function of the location on the package at which the temperature is measured. Therefore, to use the Θ_{JC} method the case temperature would have to be measured at several different points and averaged to represent the T_C of the device. This in practice could prove difficult and relatively inaccurate. To alleviate this problem manufacturers will sometimes provide a Θ_{Jref} value for a package. This number represents the thermal resistance between the die and a specific spot on the package (usually the top dead center). This measure of thermal resistance typically has a much wider standard deviation than the standard resistance parameters and therefore is sometimes avoided, however it is the most easily measured parameter from which junction temperatures can be calculated.

The Θ_{JA} method of estimating junction temperature is the most widely used. To use this method one need only measure the ambient air temperature in the vicinity of the device in question and calculate the internal power dissipation of that device. The total power dissipation in a device is made up of two parts; the static power and the dynamic power. The two components can be calculated separately and then added together. Another source of power is the termination power as clock drivers are generally used to drive terminated transmission lines. For an ECL output this can be significant however for CMOS outputs the termination load current is pulled through very little voltage (the output HIGH and LOW voltages are very near the rail) so that most of the power is dissipated in the actual load. With this in mind we will address calculating power for ECL and CMOS/BiCMOS separately.

Because clock drivers generally drive transmission lines we will not assume any lumped capacitive load at the outputs. Lumped capacitive loads on outputs add significantly to the power dissipated on chip, when however the capacitive loads are at the the end of transmission lines they are buffered from the driving device and thus do not add to the power dissipation above that attributed to driving the transmission line. Note that for the purpose of power dissipation calculations it is not equivalent to calculate the distributed capacitance of a transmission line and treat it as a lumped load at the output of the device. This technique will significantly overestimate the calculated power of a device.

Calculating Power Dissipation in CMOS/BiCMOS Devices

The total power dissipated in a device can be represented as follows:

$$P_D = I_{CC}(\text{static})*V_{CC} + I_{CC}(\text{dynamic})*V_{CC} + n(I_{OH}*(V_{CC} - V_{OH}) + I_{OL}*(V_{OL}))/2$$

In general rather than using dynamic I_{CC} numbers the dynamic power is calculated using power dissipation capacitance numbers (C_{PD}). Using C_{PD} numbers the above equation becomes:

$$P_D = I_{CC}(\text{static})*V_{CC} + C_{PD}*V_{CC}^2*f + n(I_{OH}*(V_{CC} - V_{OH}) + I_{OL}*(V_{OL}))/2$$

As mentioned previously since the output logic levels are very nearly rail to rail, the third part of the above equation can be ignored. Note that although this assumption may be true for series terminated lines it may not be true for parallel termination where the relatively large DC currents will drive the output voltage levels away from the rails. If we assume series termination then the equation reduces to the following:

$$P_D = I_{CC}(\text{static})*V_{CC} + C_{PD}*V_{CC}^2*f$$

The dynamic dissipation may be a function of the number of outputs switching, if this is the case a CPD number may be provided for each output buffer. In this case the equation would expand to:

$P_D = I_{CC}(static)*V_{CC} + C_{PD}(internal)*V_{CC}^2*f + C_{PD}(output)*V_{CC}^2*f*n$

where n = number of outputs at the given frequency f.

Finally for a CMOS device the $I_{CC}(static) = 0$ and for a BiCMOS device which utilizes ECL gates internal the $C_{PD}(internal) = 0$ so that the equations reduce to:

CMOS $P_D = C_{PD}(internal)*V_{CC}^2*f + C_{PD}(output)*V_{CC}^2*f*n$

BiCMOS $P_D = I_{CC}(static)*V_{CC} + C_{PD}(output)*V_{CC}^2*f*n$

Calculating Power Dissipation in ECL Devices

Starting from the same basic equation:

$P_D = I_{CC}(static)*V_{CC} + I_{CC}(dynamic)*V_{CC} + n(I_{OH}*(V_{CC} – V_{OH}) + I_{OL}*(V_{CC} – V_{OL}))/2$

For ECL devices the the static current is equal to the dynamic current (I_{CC} is independent of frequency) therefore the equation reduces to:

$P_D = I_{CC}*V_{CC} + n(I_{OH}*(V_{CC} – V_{OH}) + I_{OL}*(V_{CC} – V_{OL}))/2$

The above equation assumes a 50% duty cycle on a single ended output and thus takes the average of the high state and low state power dissipation. For differential outputs it is simpler to calculate the power per output pairs. Since the pairs are always in complementary states the output power for the pair is simply the addition of the low state and high state power consumption. The only time one will see a difference between a single ended and differential output calculation is under worst case conditions. For say an 18 single ended output device the worst case condition would be for all 18 to be in the worst case logic state for power dissipation purposes. For a device on the other hand with 9 pairs of complimentary outputs (18 total) only 9 of the outputs can be in the worst case condition at a time so that the worst case power dissipation of a complimentary output device will be less than a device with an equivalent number of single ended outputs.

The only issue left is determining I_{OL} and I_{OH}. These values are a function of the termination technique and the pull down voltage used. The currents are easily calculated based on the V_{OH}/V_{OL} levels the pull down resistance and the pull down voltage used. For a standard termination of 50Ω to a voltage of 2.0V below V_{CC}:

$I_{OH} = (V_{CC} – 0.98) – (V_{CC} – 2.0)/50 = 20.4mA$

$I_{OL} = (V_{CC} – 1.7) – (V_{CC} – 2.0)/50 = 6.0mA$

Thermal Resistance of Plastic Packages

With the power estimates calculated the Θ_{JA} of the appropriate package is the only required parameter left to estimate the junction temperature of a device. The Θ_{JA} number for a package is expressed in °C per Watt (°C/W) and is used to determine the temperature elevation of the die (junction) over the external ambient temperature. Standard lab measurements of this parameter for the various timing solution packages are provided in the graphs of Figure 1 through Figure 3.

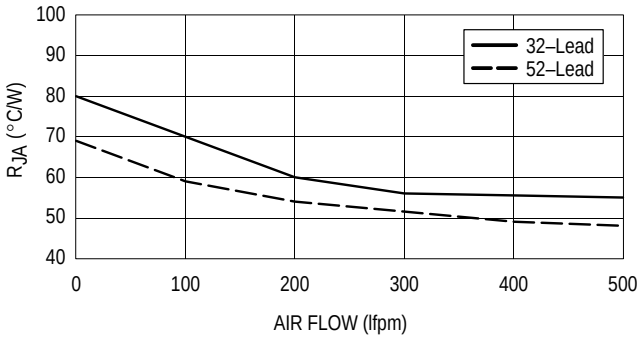

Figure 1. Thermal Resistance of the TQFP Packages

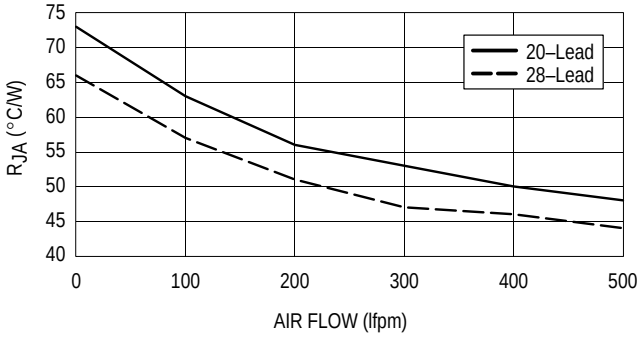

Figure 2. Thermal Resistance of the PLCC Packages

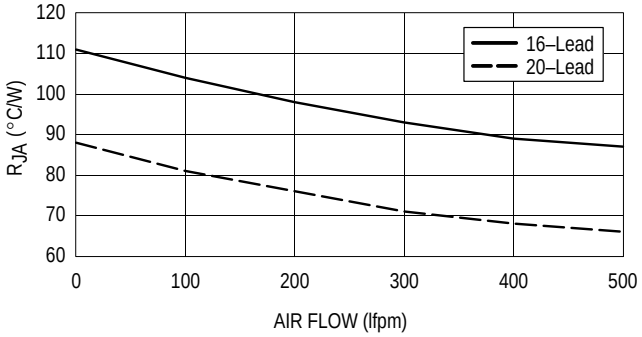

Figure 3. Thermal Resistance of the SOIC Packages

Junction Temperature Calculation Example

As an example the junction temperature of the MPC951 will be calculated. The static I_{CC} of the MPC951 is 95mA and the C_{PD} per output is 25pf. From these numbers the following results:

$P_D = 95mA*3.3V + 3.3V*3.3V*25pf*f*n = 315mW + 2.72e–10*f*n$

Assume we will configure all 9 outputs to the same frequency, the curve in Figure 4 shows the power dissipation vs frequency for the MPC951.

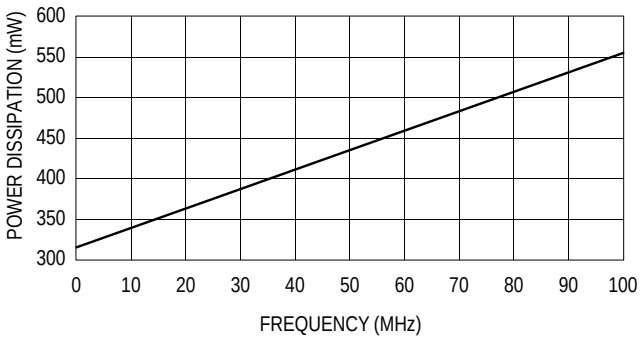

Figure 4. MPC951 Junction Temperature Calculation

Assume that one is building a design with all nine outputs operating at 66MHz. From the graph this corresponds to a power dissipation of 470mW. The MPC951 is packaged in the 32lead TQFP; from the Θ_{JA} chart (assume zero air flow) the thermal resistance of the package is 97°C/W. Plugging these into the T_J equation yields the following:

$T_J = T_A + 80°C/W*0.470W = T_A + 38°C.$

For a worst case ambient temperature of 70°C the resulting junction temperature would be 108°C. From the MTBF table this would correspond to a lifetime of greater than nine years, a lifetime which is well within the requirements of most systems. If however the user needed a little higher performance of 100MHz on the outputs the T_J would be:

$T_J = T_A + 80°C/W*0.555W = T_A + 44°C$

Under these conditions the worst case junction temperature would be 114°C and the worst case lifetime would be approaching 4 years. This may not be a satisfactory lifetime and the user would have to do some thermal management to reduce the junction temperature. Obvious enhancements would be providing airflow or perhaps reducing the maximum ambient specifications. If airflow was added (200lfpm) the junction temperature would reduce to:

$T_J = T_A + 60°C/W * 0.555W = T_A + 33°C$

This drops the junction temperature down into the same range as the 66MHz output case.

The second example will use an ECL output device; the MC100LVE111. The device has 9 differential output pairs and an I_{CC} of 65mA. Assume that the outputs are terminated 50Ω to 2.0V below V_{CC}.

$P_D = 65mA*3.3V + 9((0.98*1.02/50)+(1.7*0.3/50)) =$
$215mW + 270mW = 485mW$

The MC100LVE111 is packaged in the 28lead PLCC; from the Θ_{JA} tables the Θ_{JA} at 500lfpm is 45°C/W. This yield the following approximate junction temperature:

$T_J = T_A + 45°C/W*0.485W = T_A + 22°C$

For a maximum ambient of 70°C the LVE111 exhibits more than satisfactory long term reliability for most systems under standard operating conditions.

Note in both cases the most efficient way to lower the junction temperature is to reduce the ambient temperature of the system. Unit changes in ambient temperature result in unit changes in junction temperature no other parameter is this tightly coupled to junction temperature.

Limitations to Junction Temperature Calculations

The use of the previously described technique for estimating junction temperatures is intimately tied to the measured values of the Θ_{JA} of the package. Since this parameter is a function of not only the package, but also the test fixture the results may not be applicable for every environmental condition. As mentioned previously the Θ_{JA} of a package in a system could be somewhat higher or lower depending on the thermal design of the board.

In addition the reliability numbers derived for the intermetallic formation assumes constant usage at the specific conditions. In the real world devices will not be exposed to worst case conditions continuously but rather will cycle between the worst case and a lower junction temperature. The MTBF table does not take into account this cycling so that simply calculating the worst case junction temperature and applying it to the table directly will significantly underestimate the long term reliability of the device. Because reliability and environmental conditions are statistical in nature it is important that statistical analysis be applied to any long term reliability studies done on the clock driver products.

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center,
3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298