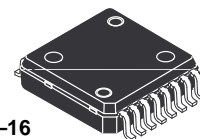


AN1580

Mounting and Soldering Recommendations for the Motorola Power Flat Pack Package

Prepared by: Jose Torres
Motorola Semiconductor Products Sector
Phoenix, AZ



PFP-16

INTRODUCTION

Motorola's Power Flat Pack-16 (PFP-16) is an overall superior package for high power surface mount applications. It is thin, space efficient, with a variety of processes to solder it to a printed circuit board (PC board). The PFP-16 is mounted and soldered like many other surface mount packages. Unlike most surface mount packages, it has a very high thermal conductivity, permitting die to dissipate up to 5 watts without consuming excessive board space. This document offers some considerations to help manufacturers using the Motorola PFP-16 take full advantage of the PFP-16 package.

WHY DOES MOTOROLA USE THE PFP-16?

Motorola uses the PFP-16 because it provides a convenient, economical and efficient way to package a high power (up to 5 watts) RF semiconductor device, all without compromising the high quality standards that Motorola's customers have come to expect. The PFP-16 is convenient as it can be assembled into PC boards using standard equipment. It is relatively simple to put on a board already populated with the common SOIC or TSSOP packages. The PFP-16 is also economical because it is compact, both in area and height, especially for high power applications. It is efficient because it has excellent thermal conductivity which allows the contained die to operate at higher power consumption levels.

The PFP-16 package has many advantages which manufacturers can pass on to their customers.

PACKAGE DESCRIPTION

The PFP-16 is essentially a thin, flat, rigid plastic case covering a silicon or GaAs chip. The package incorporates two rows of thin, gull wing metal leads that protrude from two opposing sides and a square solderable contact underneath. The plastic case is nominally 2.05 millimeters high by 7 mm long and 7 mm wide. The 16 leads extend the package width by 2 mm to 9 mm total. The solderable contact exposed on the bottom center of the plastic package is nominally 4.75 mm long by 4.75 mm wide. A 45° chamfer on one corner of the package designates pin 1 and makes its orientation easily distinguishable.

While the package dimensions are easy to describe in general terms, there are three important characteristics which merit detailed description: the contact surfaces of the leads are coplanar within a 0.10 mm tolerance; the heat sink surface stands off the mounting plane from 0.025 to 0.152 mm; and the feet of the leads have an angle tolerance between horizontal (flat) and 8° below horizontal (tipped down). These conditions are used by Motorola to ensure quality and make reflow processes easier for our customers. Each condition is defined in the following paragraphs.

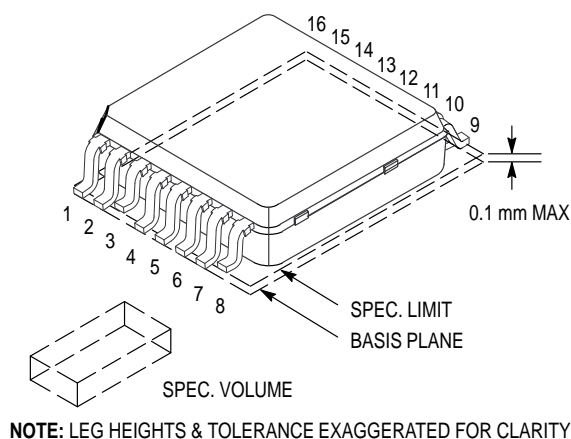


Figure 1. Coplanarity Specification

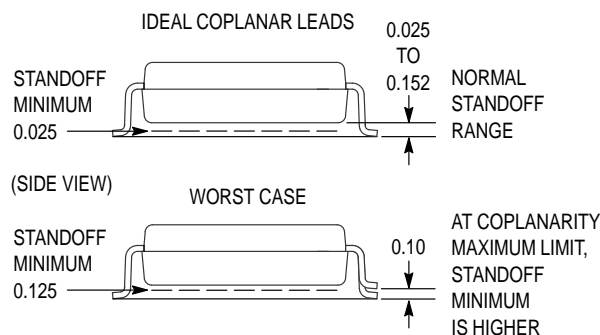


Figure 2. Standoff Specification

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The package's 16 leads are manufactured to be coplanar within a 0.10 mm (.004") tolerance (see Figure 1). The bottom surfaces of the 16 feet will be no more than 0.10 mm (.004") above the seating plane (see Datum C in Figure 4), defined as the plane furthest from the center of gravity, and common to three of the package feet that surround the center of gravity. Simply, when the package is placed feet first (down) on an ideally flat plane, no foot will be more than 0.10 mm above the plane.

Figure 1 uses exaggerated lead lengths to demonstrate more clearly acceptable tolerances. Leads 1, 2, 4, 5, 6, and 7 are all depicted ideally coplanar with the basis plane. Leads 3 and 8 are marginally acceptable at the extreme edge of the tolerance.

Figure 2 displays the standoff specification and how it controls height of the metallic heat sink above the seating plane. The bottom surface of the metallic heat sink must not be lower than 0.025 mm (0.001"), nor may it be lower than the bottom of the highest lead, (highest possible lead is limited by the coplanarity condition at 0.10 mm or 0.004") and it may not be higher than 0.152 mm (0.006") above the seating plane.

The foot angle specification requires the toe end of the foot of the lead to be lower than the heel end by 0 to 8°, as referenced from the seating plane. See Greek symbol Theta (θ) in the Package Outline Dimension table in Figure 4.

These three specifications ensure that the manufacturer receives reflow solderable products. The coplanarity specification ensures that all of the leads on the package will be solderable to a PC board with a proper solder reflow process. It also helps increase the repeatability and reliability of a manufacturer's reflow processes. The standoff restricts the solderable pad above the basis plane and places it no lower than the highest lead. It also creates space to clean off the residual flux resin. Finally, the foot angle specification allows for smoother solder fillets between the lead and the PC board. These specifications all make the package more solderable, reduce solder defects and rejects, and help

provide longer life solder joints, as well as provide a very durable product for the customer.

MOUNTING/SOLDERING CONSIDERATIONS

Soldering the PFP-16 to a PC board requires no more equipment than most other surface mount packages. However, due to the backside contact, some precautions about how the equipment is used to produce quality solder joints are necessary. The soldering recommendations that follow are provided solely for the convenience of the manufacturer and are not sufficient for actual manufacturing processes due to variations from process to process.

The PFP-16 package is intended to be placed onto solder paste that is 0.15 mm (0.006") high and on a PC board with an overstroke of 0.10 mm (0.004"). These values are to be considered as suggested values only.

An overstroke of 0.10 mm is created by setting the placement piston of a "pick and place" machine not only to push the part off of the vacuum head and onto the PC board but also to continue its quick motion and push the part an extra 0.10 mm into the PC board, and then release. This is an intended part of the package design so that the bottom surface of the metal heat sink will get pushed into contact with the solder paste that is already on the PC board. This process should leave solder clinging to the bottom surface of the backside contact, which, when reflowed, should result in a quality solder joint as shown in Figure 3.

The PFP-16 has been successfully soldered to a PC board using many different reflow techniques (infrared, hot stage, etc.). Specifications for soldering and reflowing the PFP-16 depend on many external factors such as board mass, component density, and reflow methodology. It is important to note that most solder liquidus temperatures are higher than the rated exposure temperatures of the package and semiconductor devices, and under such conditions, damage to the part may result. Consequently, customers are cautioned against exposing the package to high temperatures for extended periods of time. The following are suggested values.

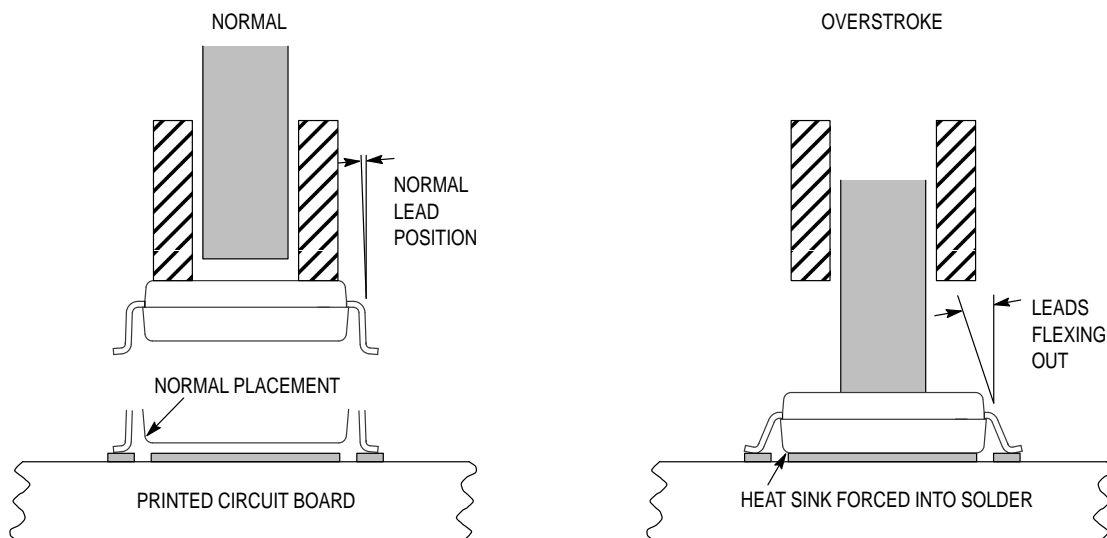


Figure 3. Effect of Overstroke

Maximum Ramp-up Rate	5°C/second
Pre-solder Dwell Temperature	125°C
Maximum Time above 185°C	120–180 seconds
Maximum Time at Max Temperature	10–40 seconds
Maximum Temperature	235°C
Maximum Ramp-down Rate	5°C/second

As stated in the Mounting/Soldering Considerations section, these values are not sufficient for actual manufacturing processes.

PFP-16 POWER DISSIPATION

The power dissipation of the Si or GaAs device through the heat sink can be quantitatively characterized by

$$P_D = (T_{Jmax} - T_{Ambient}) / R_{J-A}$$

where the maximum junction temperature of the device (T_{Jmax}) is 150°C. R_{J-A} is the gross thermal resistance from the junction(s) of the device to the ambient surroundings. R_{J-A} is the (more or less) linear sum of R_{J-C} , the thermal resistance from the device junction(s) to the case plus R_{C-A} , the thermal resistance from the case-to-PC board interface to ambient. R_{J-C} , commonly specified as θ_{JC} , is listed on the data sheet

of the device in question. R_{C-A} is application specific and includes the solder interface to the package, the PC board, heat sink, etc. For this reason, only θ_{JC} is specified for power devices since case to ambient system will vary from application to application.

PFP-16 devices should be mounted with holes or "via's" in the PC board under the device heat sink to promote thermal conductivity and RF grounding. A 3x3 pattern of 0.38 mm (0.015") via's has proven adequate. A hole as large as 9 mm (3/16") can be placed directly under the heat sink and will allow inspection of the solder fillet. To avoid solder runoff through the via's, they may be moved toward the device leads and isolated with solder masking.

Motorola does not provide suggestions for solder footprints on PFP-16 packages in RF applications because of the impact that solder quantities and layouts have on RF device performance characteristics. It is incumbent upon the manufacturer using the package to develop these application-specific guidelines.

Refer to Figure 4 for the mechanical outline of the PFP-16 package.

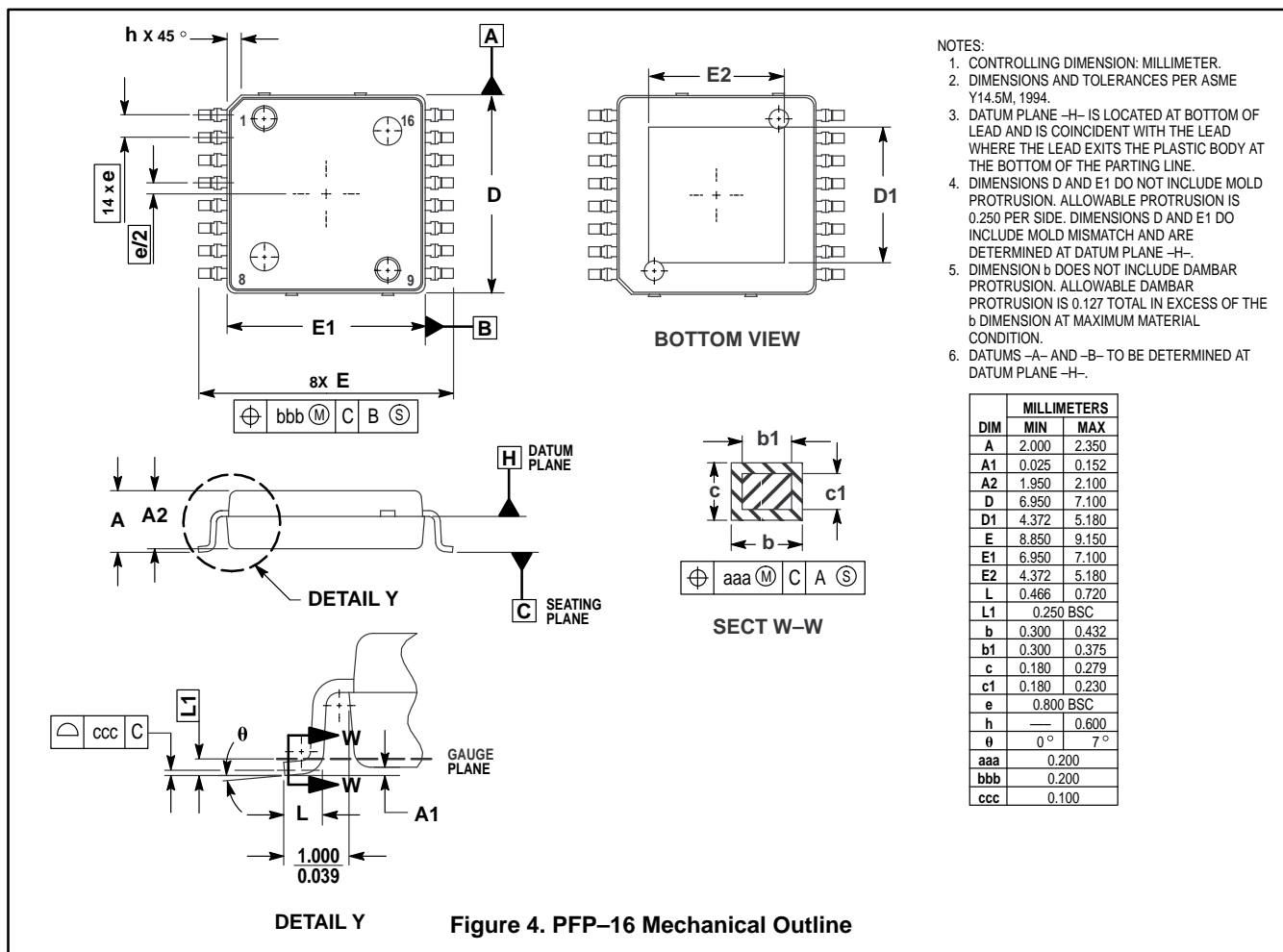


Figure 4. PFP-16 Mechanical Outline

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How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 303-675-2140 or 1-800-441-2447

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 4-32-1,
Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan. 81-3-5487-8488

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602-244-6609
– US & Canada ONLY 1-800-774-1848

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

INTERNET: <http://motorola.com/sps>

