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Power Control with the MRFIC0913 GaAs Integrated Power Amplifier and MC33169 Support IC

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INTRODUCTION

In modern multiple access radio systems, the transmitted RF power is programmable within a given range in order to optimize the propagation link budget. There are two resulting advantages; the interference level (for close receivers) is restricted and the power consumption of transmitter is reduced. In addition to this “static” output power control, the on and off switching (dynamic behavior) of the RF power must be tightly controlled to avoid the splattering of the signal into adjacent channels. This is accomplished by controlling the rise and fall time of the transmitter keying. The sharper the edges, the broader the occupied bandwidth. In TDMA systems, transmitter minimum turn on time must also be met.

This application note addresses the particulars of transmit waveform shaping and power control as applied to GSM TDMA systems using the MFRIC0913 GaAs integrated power amplifier (IPA) combined with the Motorola MC33169 GaAs power amplifier support IC.

CLOSED LOOP CONTROL APPROACH

RF output power control can be performed with a closed–loop approach. As shown in Figure 1, the RF power is sensed at the amplifier output using a directional coupler or capacitive divider and is detected across a fast Schottky diode. The resulting signal is a direct measurement of peak RF output voltage (knowing the coupling factor) and is compared to a reference voltage in an error amplifier. The loop controls the power amplifier gain via a control line to force the measured voltage and the reference voltage to be equal. Power control is accomplished by changing the reference voltage.

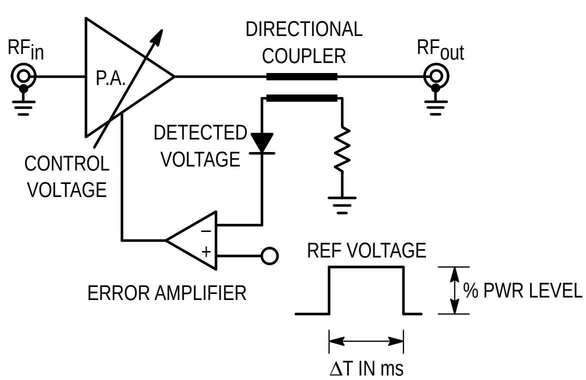


Figure 1. Closed Loop Control Technique

The main disadvantages of this approach are:

1. Output power is lost by the coupling device.
2. Dynamic range is limited to that of the detector diode, usually about 20 dB without compensation.
3. Loop gain can vary significantly over the dynamic range causing stability problems.
4. Switching transients are difficult to control if the loop bandwidth is not constant.

SUPPLY VOLTAGE CONTROL APPROACH

An alternative approach, particularly applicable to amplifiers utilizing square law devices such as FETs, uses supply voltage to control the output power of the amplifier. The RF output power from an FET amplifier is proportional to supply voltage. Reducing the drain voltage effectively limits the RF voltage swing and, hence, limits the output power. The response time is very fast and, as such, this technique, also known as high–level modulation, has been used for years in high–power AM transmitters.

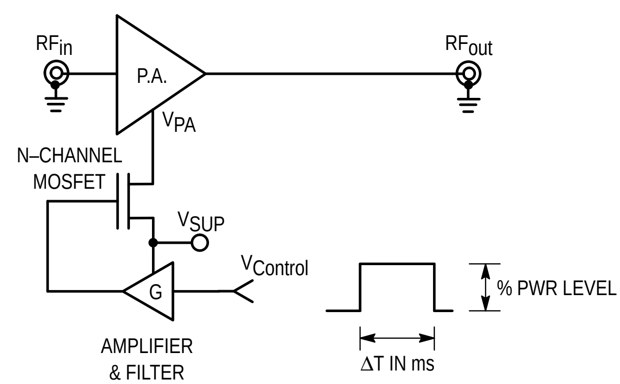


Figure 2. Supply Voltage Control Technique

An N channel MOSFET is used in Figure 2 as a follower to vary the supply voltage of the PA (V_{PA}) from 0 to V_{SUP}. The difference between the MOSFET’s gate voltage and the PA supply voltage is almost constant at the device threshold voltage, V_{TH}. A fixed gain amplifier drives the gate of the MOSFET. It’s maximum output voltage capability should be higher than $V_{SUP} + V_{th}$.

The analysis of this system is straightforward since every block has a nearly linear transfer function. The transfer characteristic of the system is shown in Figure 3.

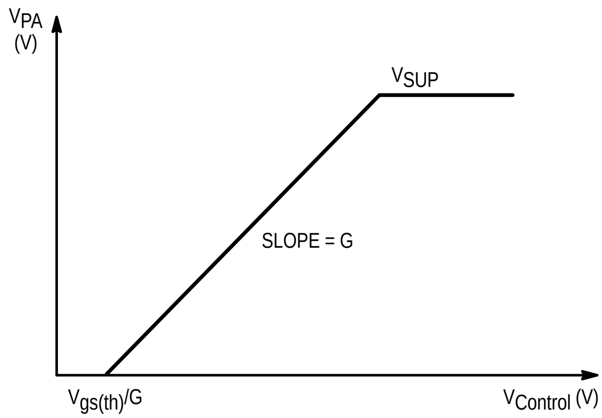


Figure 3. Supply Voltage Control Approach Transfer Characteristic

As mentioned above, RF output is proportional to V_{PA}, so we can substitute "RF output voltage" for V_{PA} in the transfer characteristics. Figure 4 shows the results of actual measurements made on such a system. A filter may be added with the control IC in order to control the transient behavior of the system as explained in the burst shaping section below.

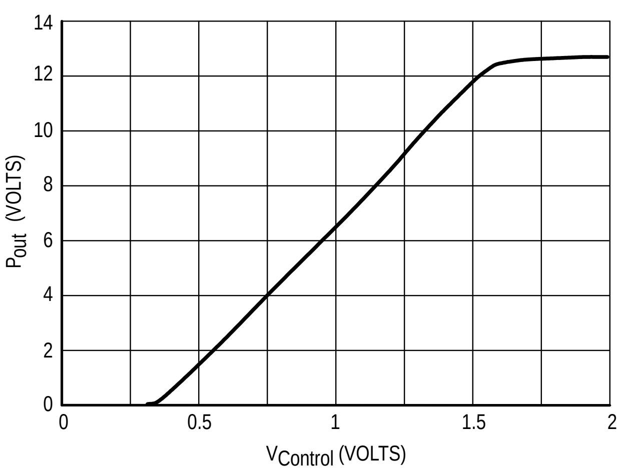


Figure 4. MESFET Amplifier RF Output Voltage versus $V_{Control}$

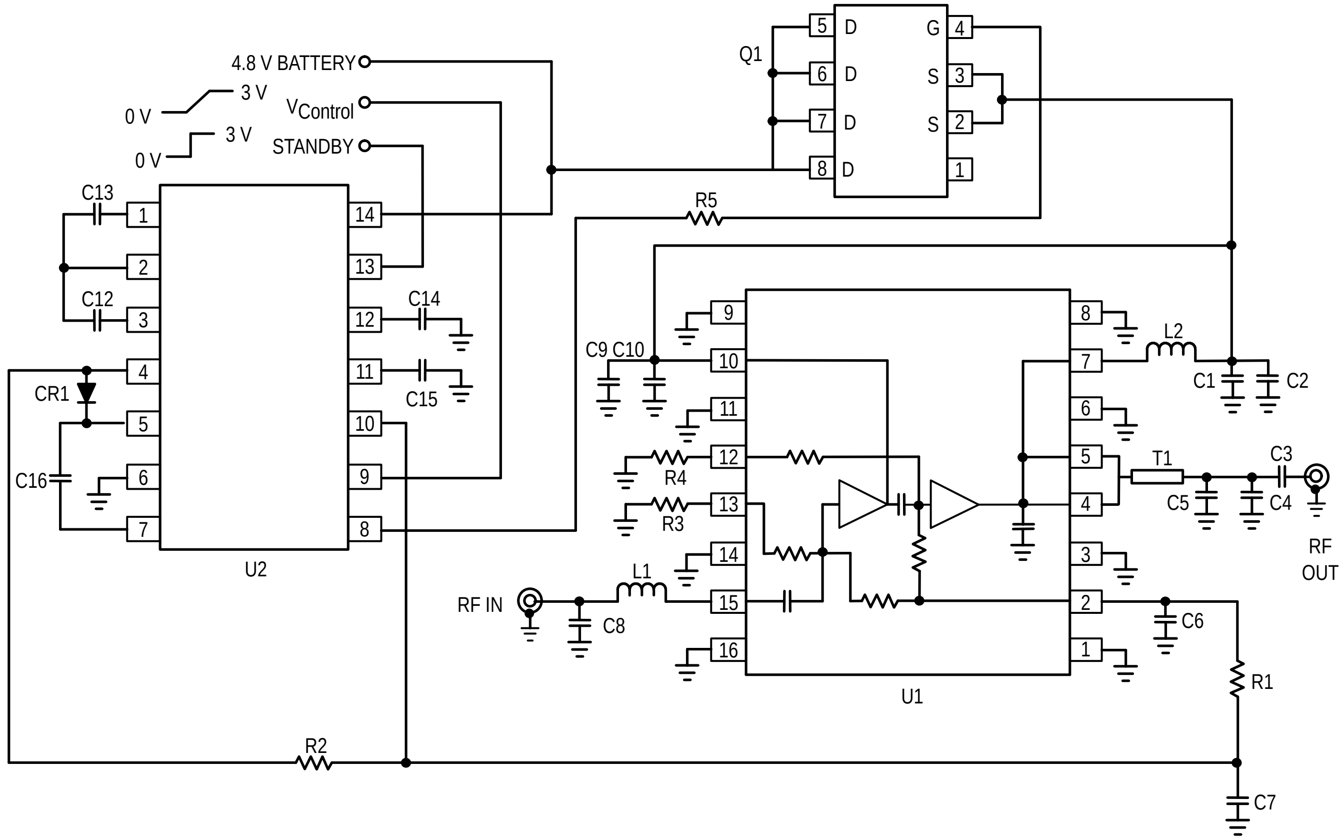
DUAL DEMONSTRATION BOARD

The results shown in Figure 4 were achieved with the Motorola MRFIC0913 GaAs MMIC Power Amplifier and GaAs PA support IC MC33169 configured in the supply voltage control approach previously described. Figure 5 shows the schematic for a 900 MHz GSM amplifier utilizing these two ICs. This amplifier is capable of producing 35 dBm output power at 50% power added efficiency from a single 4.8 V supply in the 880 to 915 GSM band.

MRFIC0913 INTEGRATED POWER AMPLIFIER

The MRFIC0913 is an integrated two–stage depletion mode GaAs MESFET power amplifier optimized for saturated operation in the 800 to 1000 MHz frequency range. It is packaged in the PFP–16 power surface mount RF package. This package is unique in its power handling capability. The GaAs die is mounted on a heatsink integrated into the lead frame which is exposed on the backside of the package. The package is soldered to the PCB just as any other surface mount package, however, the direct attach of the heatsink gives greatly improved thermal and electrical performance. Refer to Motorola application note AN1580, "Mounting and Soldering Recommendations for the Motorola Power Flat Pack Package," for more detail on the construction and soldering of the PFP–16 package.

The RF input match is a low–pass structure employing series inductor L1 and shunt capacitor C8. The interstage match between the driver and final amplifier is tunable through changes in value or position of the bypass capacitor C10. Moving this capacitor closer to the device or reducing the capacitance increases the frequency of resonance with the shunt inductor formed by the wirebonds and package lead frame. The output match is a two–stage low pass network which represents a compromise between bandwidth and harmonic rejection and presents a 3 Ω loadline to the output stage. Implementation is through transmission lines for the series inductors and shunt chip capacitors. High quality chip capacitors must be used to insure good harmonic termination. Harmonic suppression and optimized efficiency also require special care in power supply bypassing at pin 7. Refer to the MRFIC0913 data sheet for more details.



C1	33 pF, 0603 NPO/COG	CR1	MMBD701LT1	R2	100 Ω
C2, C9	33 nF	L1	8.2 nH, 0805 Toko	R3	1.8 kΩ
C3	47 pF, 0603 NPO/COG	L2	10 Turn MicroSpring,	R4	2.7 kΩ
C4, C5, C8	6.8 pF, 0603 NPO/COG		Coilcraft 1606–10 (for	R5	470 Ω
C6	33 nF		improved harmonic rejection	T1	5 mm 30 Ω Microstrip Line
C7	220 nF		only)	U1	MRFIC0913
C10	33 pF, 0603 NPO/COG	Q1	MMSF4N01HD	U2	MC33169 (–4 V Version)
C12 – C16	1 µF	R1	330 Ω	BOARD MATERIAL	Glass/Epoxy, ε_r = 4.45

Note: Use of a Schottky diode such as MMBD701LT1 for CR1 is mandatory below 3.6 V.
A general purpose silicon diode can be used above 3.6 V.

Figure 5. GSM Application Circuit Configuration with Drain Switch and MC33169 GaAs Power Amplifier Support IC

MC33169 SUPPORT IC

The MC33169 supplies the control functions described above. Additionally, it supplies the negative supply generator required by the depletion mode GaAs MESFETs of the MRFIC0913, an N–MOS switch interface for driving the drain switch and a power supply sequencer. Refer to the MC33169 data sheet for specifications and more detail on device operation.

The MC33169 negative voltage generator uses an internal 100 kHz oscillator that can produce spurious signals close to the carrier at the IPA RF output unless proper filtering is applied. There are two sensitive paths for these spurs. The negative voltage itself has transients which can modulate the bias point of the PA. In the demonstration circuit, two cascaded low pass RC sections (R1, R2, C6, and C7) are used to suppress these transients. The control voltage which drives the N–MOSFET gate, which cannot be filtered aggressively in order to keep fast control bandwidth, is the other source. In this case, only a series resistor, R5, is used. Spurious performance can be improved further if the supply voltage of MC33169 is kept below 4 Volts. This can be accomplished either by connecting it to a voltage regulator or with a series resistor which drops the battery voltage to a lower value. Along with the dropping resistor, a 1 µF capacitor should be placed near pin 14 for better decoupling and filtering. Figure 6 shows the spectrum of the amplifier output with proper filtering with GSM modulation applied (4 MHz span) at the lowest RF output level, 5 dBm. A spectral purity of more than 60 dBc at 400 kHz beside carrier can be noted. This is fully compliant with the phase 2 ETSI recommendations.

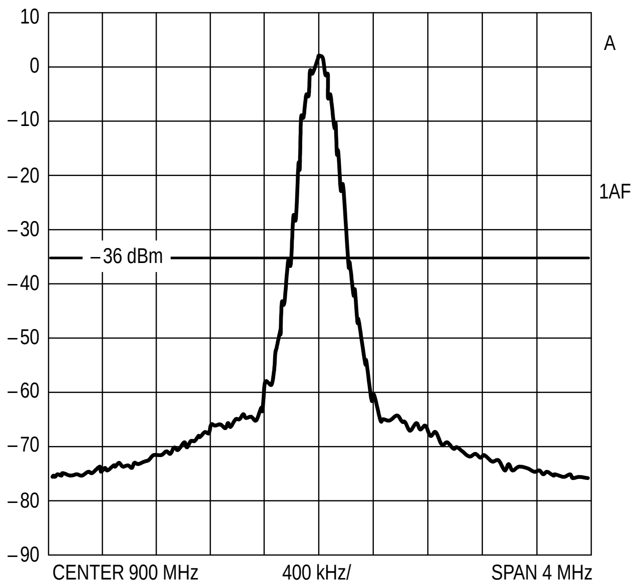


Figure 6. Modulation Spectrum of PA at 5 dBm Output

Double and triple voltages are available at pins 11 and 12 and can be used for external purposes provided that the current drain is only a few mA maximum. For example, these outputs can supply other components such as operational amplifiers, PLL charge pumps, switches, etc. Having higher voltages available than the battery itself is a key advantage in low battery systems.

ADVANTAGES OF SUPPLY VOLTAGE CONTROL

An important advantage to this approach for constant envelope modulation schemes such as GSM, is that the PA always operates in a saturated mode which improves its efficiency and reduces the AM to AM conversion. If the PA has several stages, they can be controlled in parallel, resulting in greater dynamic range. In GaAs MESFET amps, drain voltage control is preferable to gate voltage control since it changes the load line of the device and not its operating point. Changes in operating point may result in amplifier instability.

The fact that there is linear correspondence between control signal and RF output voltage has several benefits. In particular, there is better control of three key parameters of the power amplifier:

1. Output power is predictable after a simple calibration,
2. The burst template (power versus time) is easily shaped,
3. Spurious output due to the switching process is minimized.

In addition to the control advantages, the supply voltage control approach is also cost effective and efficient with respect to space and power. The coupler and associated losses required for the closed loop approach are eliminated, detector diode and temperature compensation circuitry is avoided, and the error amplifier with its potential stability problems is unnecessary.

POWER CALIBRATION

In order to predict accurately the output power of the PA versus control voltage, the transfer characteristics of the system must be known. The linear portion can be approximated after measuring two points and computing the linear equation y = ax + b where:

a = (y2–y1)/(x2–x1)	slope
b = y1–ax1	crossing with y axis
x0 = –b/a	crossing with x axis

This is shown graphically in Figure 7. Once these arguments are known, the control voltage needed for a given output power, expressed in RF volts across 50 Ω, can be calculated. Power output is then:

$$P_{out}\ (\mathrm{dBm}) = 10\mathrm{Log}\ (P_{out}\ (\mathrm{V})^2/50) + 30$$

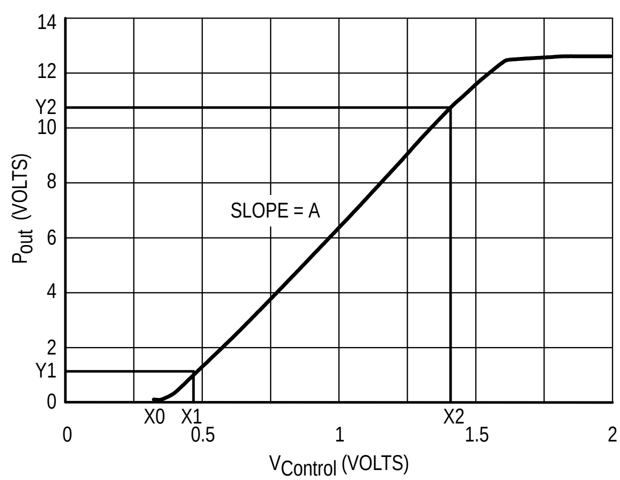


Figure 7. Control Loop Calibration

Table 1 shows the predicted versus actual output power for a typical MRFIC0913 with MC33169 support IC as described above. As can be seen, with a greater than 30 dB control range, there is a maximum absolute prediction error of only 1 dB.

Table 2 shows the calibration factors used in the equations above.

Table 1. Actual versus Predicted Power Output

Power Control Level (PCL)	Theoretical P_{out} (dBm)	Theoretical P_{out} (Volt)	Computed $V_{Control}$ (V)	Measured P_{out} (dBm)	P_{out} Error (dB)
5	34	11.21	1.620	34.15	–0.15
6	32	8.90	1.365	32.1	–0.10
7	30	7.07	1.163	30	0.00
8	28	5.62	1.002	27.65	0.35
9	26	4.46	0.875	25.6	0.40
10	24	3.54	0.773	23.6	0.40
11	22	2.82	0.693	21.8	0.20
12	20	2.24	0.629	20	0.00
13	18	1.78	0.578	18.3	–0.30
14	16	1.41	0.538	16.5	–0.50
15	14	1.12	0.506	14.5	–0.50
16	12	0.89	0.480	12.2	–0.20
17	10	0.71	0.460	10	0.00
18	8	0.56	0.444	7	1.00
19	6	0.45	0.431	5.3	0.70

NOTE1: P_{in} = 10 dB

NOTE2: Tx Path Insertion Loss = 1 dB

Table 2. Calibration Factors

PCL	$V_{Control}$ (V) x–axis	P_{out} (dBm)	P_{out} (V) y–axis
17	0.46	10	0.71
7	1.2	30.4	7.40

BURST SHAPING

As mentioned earlier, the rise and fall time of the burst signal must be controlled to meet turn on time requirements without splattering into adjacent channels. This burst shaping and associated switching transients control can be realized by adding a three–pole low–pass filter to the MC33169. The $V_{Control}$ pulse is precisely shaped and smoothed by the transfer function of the filter and the resulting voltage again has direct correspondence with the output power.

The system, including the three pole filter, is simplified in Figure 8.

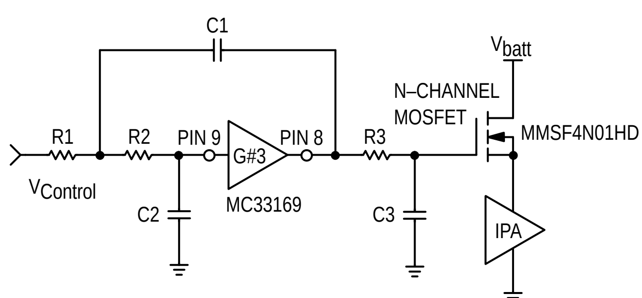


Figure 8. Control Loop with Burst Shaping Filter

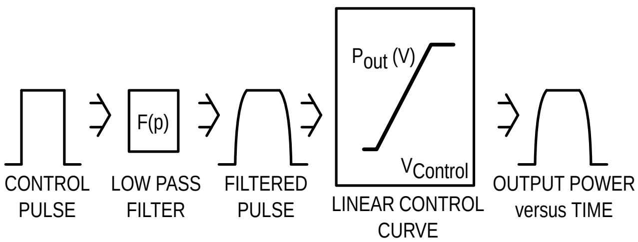
The transfer function of this arrangement is:

$$F(p) = \frac{G}{R1R2C1C2p^2 + (R1C2 + R2C1 + R1C1(1-G))p + 1} \times \frac{1}{R3C3p + 1}$$

Assume R1=R2=R. Then:

$$F(p) = \frac{G}{R^2C1C2p^2 + R(C2 + C1(2-G))p + 1} \times \frac{1}{R3C3p + 1}$$

The time response of the chain is:



The optimization of the filter and its time response can be achieved easily with simple CAD software such as SPICE. It is important that the pulse response have no overshoot, so a Bessel type filter with cutoff frequency of approximately 50 kHz is preferable.

It should be noted that input impedance on pin 9 of MC33169 is not particularly high (about 90 kΩ) so R1 and R2 must be low enough not to change the amplifier gain. The following values have proven to produce good results for a GSM–like time template and occupied bandwidth requirements.

R1 = R2 = 4.7 kΩ
C1 = 560 pF
C2 = 1.5 nF
R3 = 1 kΩ
C3 = 1 nF

Figure 9 shows the beginning and end of a TDMA burst shaped with the recommended filtering at various output power levels.

VARIATIONS OF THE TECHNIQUE

The "dead zone" corresponding to the threshold of the MOSFET can be compensated for by using a high gain differential amplifier such as an operational amplifier in the feedback loop as shown in Figure 10. The control curve is then independent of the MOSFET turn–on characteristics. The gain is set by external resistors according to available $V_{Control}$ range. The output voltage capability of the op amp should be greater than $V_{SUP} + V_{TH}$.

A P–channel MOSFET can also be used as shown in Figure 11. With this approach, the output capability of the op amp is reduced to V_{SUP}. The op amp is also used as an inverter.

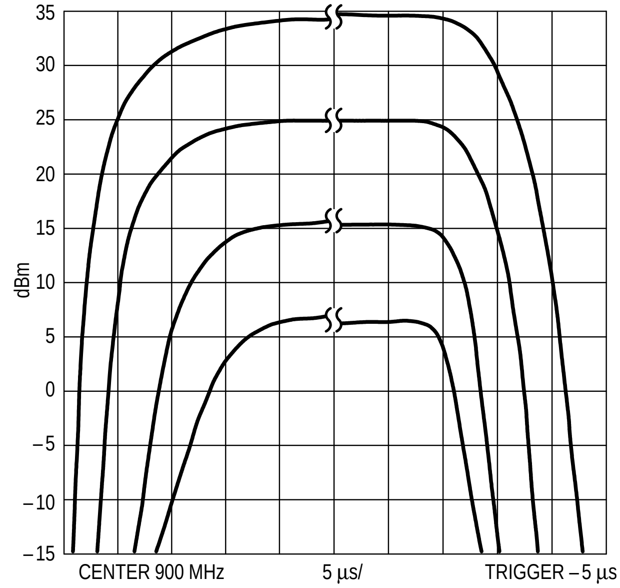


Figure 9. Burst Leading and Trailing Edges with Filtering

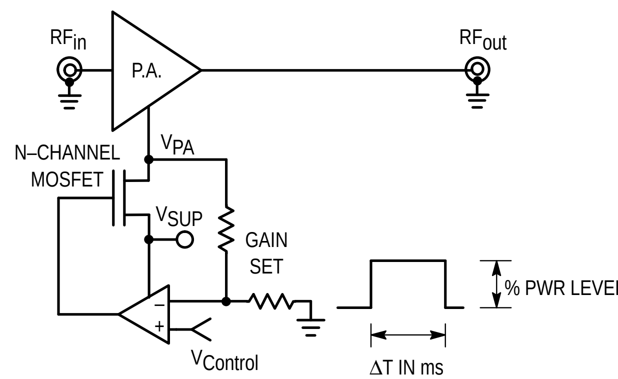


Figure 10. Control Loop with Differential Amplifier

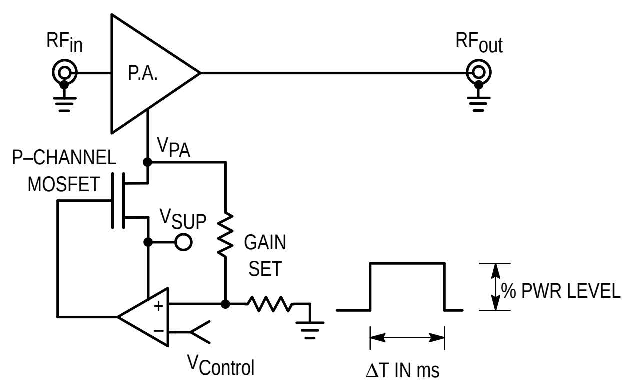


Figure 11. Control Loop with P–Channel MOSFET

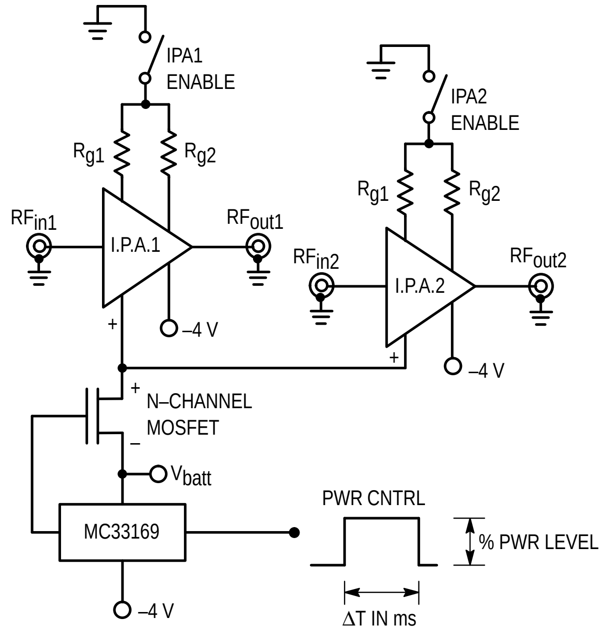


Figure 12. Dual Band Control

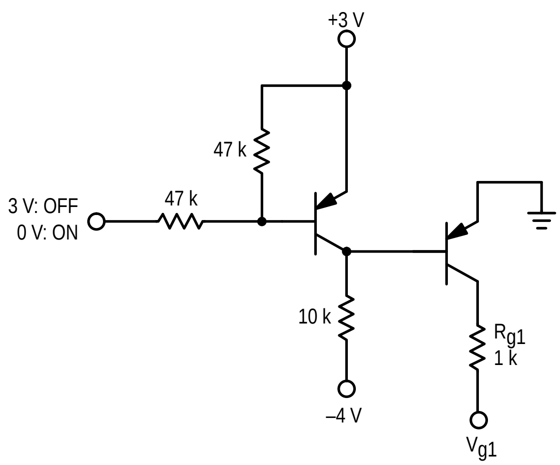


Figure 13. Negative Supply Current Reduction Circuitry

The control solution can be applied to two amplifiers in parallel with special enabling circuitry allowing optimized dual–band power amplifier control as shown in Figure 12.

With this technique, the same control circuitry can be shared by both amplifiers and the control curve is identical for both bands.

The interface circuitry shown in Figure 13 can be used to reduce the current consumption from the negative supply. As a result, the consumption of MC33169 is also reduced by a factor of three.

CLOSED LOOP USING SUPPLY VOLTAGE CONTROL

A hybrid of the two control techniques applies the supply voltage control technique within a closed loop architecture. Although this approach requires an RF voltage detector and has the additional losses from the output power coupler, compared with an open loop configuration, benefits like AM to AM reduction, high predictability, and ease of shaping still remain.

This is a major advantage since it is well known that PA control, in TDMA mode, is one of the biggest problems in high–volume manufacturing.

The behaviour of the complete loop is then much more stable and repeatable in production than for a gate controlled PA.

CONCLUSION

An amplifier control technique has been presented which is particularly well suited to power amplifiers in TDMA systems. It utilizes componentry already required for the high–efficiency depletion–mode GaAs MESFET PAs often used in such applications to perform burst shaping and power control. A demonstration circuit using a 900 MHz GSM Class IV subscriber terminal amplifier has been presented which gives greater than 1 dB power–setting accuracy over a 30 dB range without the complexity and instabilities of traditional power output sampling closed loop controls.

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