AN1610

Using Motorola's MRFIC1502 in Global Positioning System Receivers

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INTRODUCTION

The Global Positioning System is a Department of Defense operated system consisting of 24 satellites in orbit at an altitude of 20,183 km. The satellites continuously broadcast a navigation message on two L–band frequencies: Link 1 at 1574.42 MHz and Link 2 at 1227.6 MHz. The coarse acquisition(C/A) code and the precise (P) code are broadcast on L1 while the encrypted P(Y)–code is only broadcast on L2. The MRFIC1502 downconverter is targeted for the reception of the C/A code on L1, although it is potentially capable of receiving the P–code also. This application note focuses on the use of the Motorola MRFIC1502 as the downconverter in a GPS receiver.

SYSTEM ARCHITECTURE

The C/A code on L1 is broadcast at a power level that guarantees a minimum of –160 dBW at the user receiver equipment. The 1575.42 MHz carrier is modulated with both the C/A and P pseudo–random noise codes in quadrature. In addition, the navigation data stream is BPSK modulated on the carrier at a 50 bps data rate. The bandwidth of the C/A code is 2.046 MHz (1.023 MHz chip rate results in spreading the signal to ±1.023 MHz null to null) while the bandwidth of the P–code is 20.46 MHz (10.23 MHz chip rate). The content that follows is limited to the C/A code despreading and demodulation.

The power level received by the antenna is greater than –130 dBm as guaranteed by the system specifications in the GPS ICD–200, assuming that the receiver is in clear view of the sky. Any obstructions, such as foliage or vehicular structures, will degrade the signal substantially. Therefore, it is recommended that the system be designed with a sensitivity that is at least 5.0–7.0 dB lower than the guaranteed minimum signal level. This receive sensitivity will be discussed in the context of this application note with respect to the cascaded system noise figure and gain. Note that the demodulation scheme affects the overall sensitivity of the receiver and that the system designer has the ultimate control over the receiver performance.

A typical GPS receiver block diagram is shown in Figure 1. The receiver is shown with two amplifier and two filter stages preceding the MRFIC1502 downconverter. The specifications of these amplifiers and filters are left up to the system designer. Some of the tradeoffs and issues are discussed in the following section.

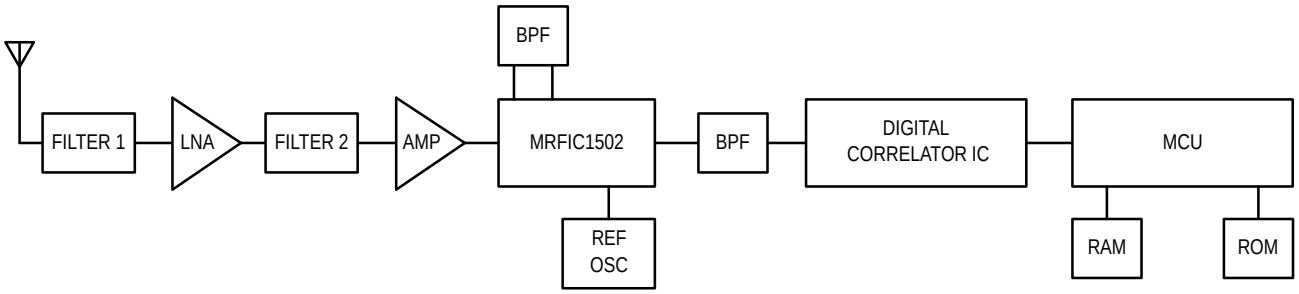


Figure 1. Typical GPS Receiver

LOW NOISE AMPLIFIER

The low noise amplifier is arguably the most critical component in the GPS RF receiver. This amplifier sets the overall system noise figure, thus contributing directly to the system sensitivity. The limits on the overall cascaded system noise figure should be determined by the system engineer, and the specifications for the LNA will be determined by this limit. One recommended LNA for use in the GPS system is the MRFIC1501. A data sheet is available for the MRFIC1501. This device provides 17 dB of gain with a 1.5 dB noise figure and consumes 7.0 mA off a 5.0 volt supply. The calculation of the system noise figure shown in Figure 1 is as follows:

$$NF(abs) = NF1 + \frac{NF2-1}{G1} + \frac{NF3-1}{G1 * G2} + \frac{NF4-1}{G1 * G2 * G3} + \frac{NF5-1}{G1 * G2 * G3 * G4} \text{ where :}$$

$$NF1 = 10^{filter1loss(dB)/10}$$

$$NF2 = 10^{NFLNA(dB)/10}$$

$$NF3 = 10^{filter2loss(dB)/10}$$

$$NF4 = 10^{NFAMP(dB)/10}$$

$$NF5 = 10^{NF1502(dB)/10}$$

$$G1 = 10^{filter1gain(dB)/10}$$

$$G2 = 10^{LNAgain(dB)/10}$$

$$G3 = 10^{filter2gain(dB)/10}$$

$$G4 = 10^{AMPgain(dB)/10}$$

The cascaded noise figure in dB is then:

$$NF(dB) = 10 * \log(NF(abs))$$

The second amplifier shown above is a general purpose amplifier with reasonably low noise figure (3.0 dB), and around 15 dB of gain. The system noise figure, calculated using the above formulas and the data from the part data sheets, is 3.0 dB. The two ceramic filters shown, part number KFF6338, are manufactured by Motorola's Ceramic Components Division. Since it can be shown that the receiver sensitivity decreases approximately 1.0 dB for every 1.0 dB increase in system noise figure, much care should be taken in the choice of the filters and low noise amplifier.

FILTERS

The choice of the ceramic filters has a direct impact on the performance of the GPS receiver in the presence of undesired jamming signals. There is not currently available an industry standard on the performance of the receiver in a hostile environment. There are several specifications that suggest the level of performance, one of which is RTCA–DO160B. The jamming signal can have one of two effects on the receiver. First, if the out–of–band filtering is not adequate, the jamming signal will cause the low noise amplifier or the downconverter to go non–linear, which could cause unwanted spurious output or an increase in the noise figure of the devices. The second effect is if the jam–to–signal ratio of the demodulator is violated, then the receiver will loose lock on the signal and will be unable to output position.

The 1.0 dB compression point of the MRFIC1502 is –40 dBm. Because of this low input compression point, the primary concern with a jamming signal is that the input of the MRFIC1502 will be driven into compression. Therefore, there needs to be enough filtering to ensure that the front end of the MRFIC1502 will not be subject to a signal that will be greater than the input 1.0 dB compression point.

The frequency plan of the MRFIC1502 is such that the first image is at 1575.42–2*47.7 MHz, or 1479 MHz. Any jamming signal present at this frequency will be mixed down to the IF frequency and be superimposed on the desired signal. There should be enough rejection at the image frequency so that the jamming signal will be no more than 30 dB greater than the desired signal when mixed down to the IF frequency.

DOWNCONVERTER DESIGN

See Figure 2 for the block diagram of the MRFIC1502 downconverter. The MRFIC1502 design is the standard dual downconversion configuration with an integrated fixed frequency phase–locked loop to generate the two local oscillators and the buffer to generate the sampling clock for the digital correlator and decimator. The active device for the L–band VCO is also integrated on the chip. This chip is designed in the third generation of Motorola's Oxide Self Aligned Integrated Circuits (MOSAIC 3) silicon bipolar process. See Figure 3 for a typical application circuit.

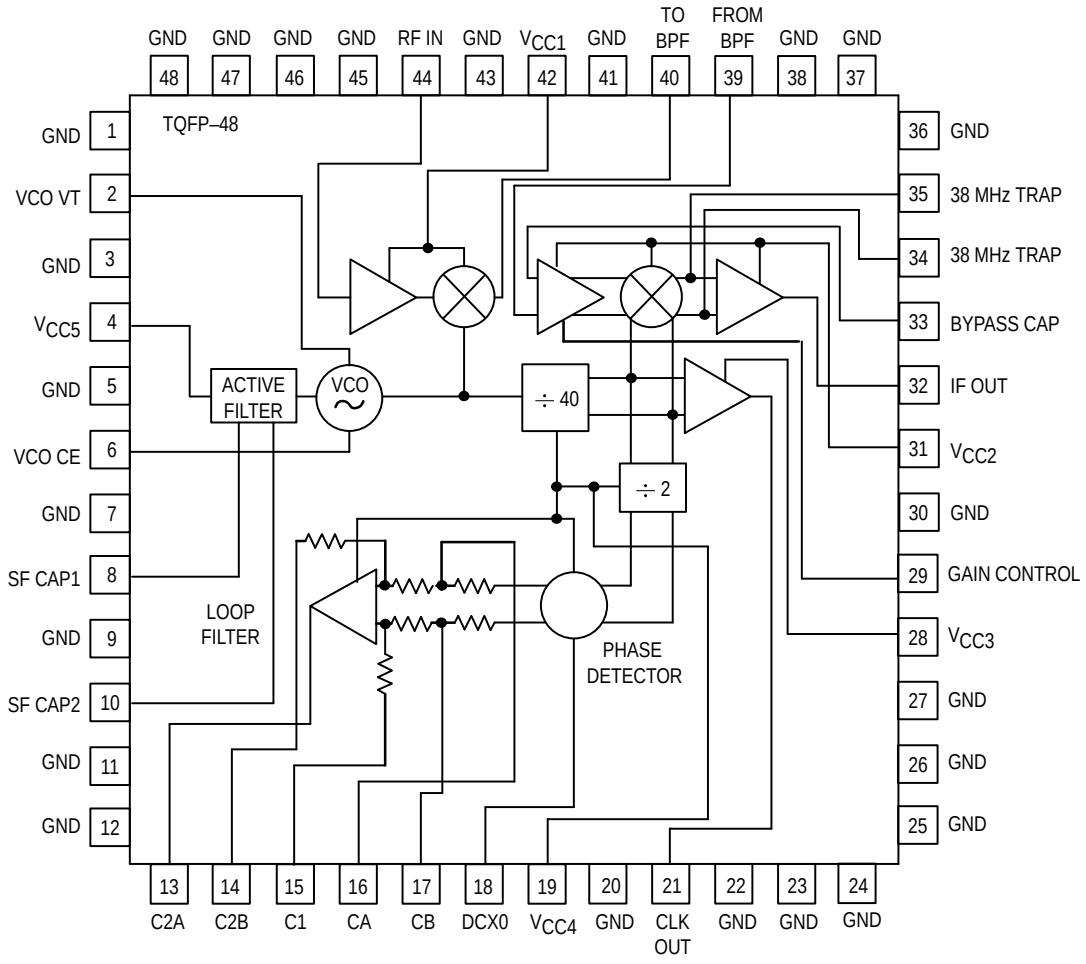
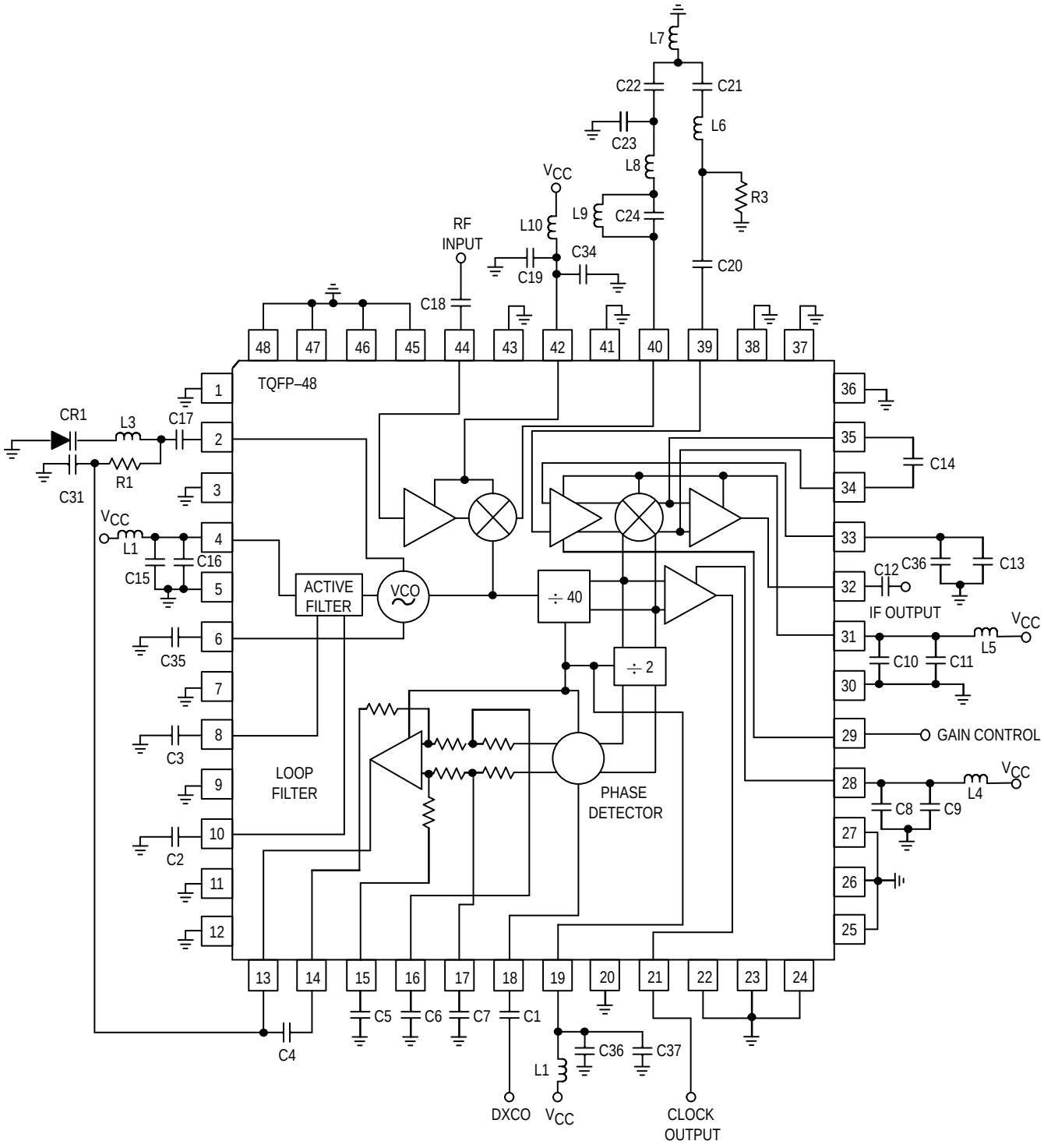


Figure 2. Pin Connections and Functional Block Diagram



C1, C8, C10, C12, C13, C15, C19, C20, C37	10,000 pF	C24	68 pF, ATC
		C35	0.4 pF, ATC
C4, C5	5600 pF	CR1	2.7 pF, MA45233–123, MACOM
C6, C7, C31	1000 pF	L1, L4, L5, L10	2.2 µH, 1008CS–222XKBC, COILCRAFT
C2, C3	1.0 µF	L3	2.2 nH, LL2012–F2N2S, TOKO
C14	3.9 pF, ATC	L6	2.2 µH
C16, C18, C36	27 pF, ATC	L7	220 nH
C17	15 pF, ATC	L8	0.56 µH
C21	5.6 pF, ATC	L9	0.27 µH
C9, C11, C34, C36	47 pF, ATC	R1	10 kΩ
C22, C23	120 pF, ATC	R3	220 Ω

Figure 3. Test Circuit Configuration

RF INPUT

The RF input to the MRFIC1502 is internally matched to 50 ohms. Therefore, only AC coupling is required on the input. The noise figure of the input amplifier is approximately 4.5 dB, and the gain is 13 dB. The output of the amplifier is not brought off–chip, but fed directly into the first mixer. This mixer is an active Gilbert Cell configuration, providing 7.0 dB of conversion gain. The output of the mixer is brought off–chip for the necessary filtering of the unwanted mixer products. The cascaded noise figure of the input amplifier and mixer is 9.5 dB.

The input amplifier and mixer have their own V_{CC} supply (pin 42) in order to reduce the amount of coupling to the other circuits. Therefore, in order to take advantage of this separate bias pin, the external circuitry must be designed properly and the layout must be done correctly. There are two bypass capacitors on this pin, one for the high frequency components and one for the lower frequency components. These two capacitors should be placed physically as close to the bias pin as possible to reduce the inductance in the path. The capacitors should also be grounded as close to the ground of the IC as possible, preferably through a ground plane. This will ensure that the gain of the stage is maximized and will reduce any chances of oscillation in the device. The amplifier is unconditionally stable as designed, but through poor grounding and bypassing strategies, the input can be made unstable.

FIRST IF FILTER

The first IF filter is designed primarily to filter out any undesired mixing products that may have been generated in the mixer. Secondly, this filter acts to suppress the image frequency of the second mixer at 28.6 MHz (47.74 – 2*9.54 MHz). The output impedance of the first mixer is 50 ohms, while the input impedance to the first IF amplifier is 1.0 kΩ. The IF filter that is shown in the application circuit is designed with a 50 ohm input and 200 ohm output, and has a bandwidth of 15 MHz. There is a trap (zero) designed in at the second LO frequency to limit the amount of LO leakage into the high gain first IF amplifier. Because there is a level translator on the chip that outputs a TTL level signal, there will always be a certain level of the 38 MHz signal floating on the chip. The designer must take the steps to prevent this from causing problems.

FIRST IF AMPLIFIER AND MIXER

The first IF amplifier is a variable gain amplifier with 25 dB of gain and 40 dB of gain control. The gain control pin can be grounded to provide the maximum gain out of the amplifier. If the baseband design utilizes a multi–bit A/D converter in the digital signal processing chip, this amplifier could be used to control the input to the A/D converter. As with any feedback system, much care needs to be taken so that the amount of amplitude modulation is kept to a minimum.

The amplifier has an external bypassing capacitor that is brought off the die due to the size of the capacitor. This capacitor should be on the order of 0.01 μF, and should be located near the package pin.

The second mixer design is also of the Gilbert Cell type. This mixer converts the 47.74 MHz signal to the final IF of 9.548 MHz. The interface between the mixer and the second IF amplifier is differential in order to increase noise immunity. This differential interface is also brought off–chip so that some additional filtering could be added in parallel between the output of the mixer and input to the amplifier. This filtering is primarily to reduce the amount of LO leakage into the final IF amplifier and is achieved using a single 3.9 pF capacitor across the differential ports. The value of the capacitor determines the high frequency of the low pass structure.

The supply pin for the IF circuits is on pin 33. This supply pin should be isolated form the other chip supplies in order to reduce the amount of coupling. The recommended capacitors are a 47 pF and 0.01 μF capacitor in parallel to bypass the supply to ground. The bypass capacitors should be placed physically as close to the pin as possible, preferably on the back side of the board directly under the MRFIC1502.

SECOND IF OUTPUT

The output of the second IF amplifier is 50 ohms with a bandwidth of ±5.0 MHz. This signal must be filtered before being digitized in order to limit the noise entering the A/D converter. The filter specifications are at the discretion of the system designer.

VCO RESONATOR DESIGN

The design and layout of the circuits around the voltage controlled oscillator (VCO) are the most sensitive of the entire layout. The active device and biasing resistors are integrated on the MRFIC1502. The external circuits consist of the power supply decoupling, the capacitors for the integrated supply superfilter, the resonator and frequency adjusting elements, and the bypassing capacitor on the emitter of the active device.

The VCO supply is isolated from the rest of the PLL circuits in order to reduce the amount of noise that could possibly cause frequency/phase noise in the VCO. The supply should be filtered using a 22 μH inductor in series and two capacitors in parallel. The two capacitors are a 27 pF and 0.01 μF. The 27 pF capacitor should be series resonant at least as high as the VCO frequency to get the most L–band bypassing as possible. The on–chip supply filter requires two capacitors off–chip to filter the supply. The active filter is basically a pass transistor with feedback circuitry to filter out any noise present at the input. The capacitors on the input (pin 8) and output (pin 10) of the filter are 1.0 μF, and the output also has a high frequency bypass capacitor in parallel. The input capacitor should not be smaller than a 1.0 μF to ensure stability of the supply filter.

The VCO design is the standard negative resistance cell with a buffer amplifier. The off–chip frequency determining components are required because the chosen semiconductor process does not have a high Q tuning diode as a standard component. The resonating structure is connected to the base of the active device and consists of a coupling capacitor, a hyper–abrupt varactor diode, and an inductive device, which in this case is a wire wound chip inductor. With the values shown on the application circuit, the VCO is centered at 1527.7 MHz, and the gain of the VCO is approximately 20 MHz/volt.

The above performance is heavily dependent on the capacitive structure that is used as the emitter bypass on pin 6. Because there is not a high Q capacitor on–chip, the RF bypassing of the emitter to ground is done off–chip. The total capacitance should be around 1.0 pF, and this can be achieved using either a discrete element or a microstrip open circuited stub. The evaluation circuit shown uses a 0.4 pF capacitor.

PHASE–LOCKED LOOP DESIGN

The VCO signal at 1527.68 MHz is divided by 40 to the second LO frequency of 38.19 MHz. In addition to providing the LO to the second mixer, the 38 MHz signal is output through a translator and used as the sampling clock for the digital correlator and decimator circuits. There is an additional divide by two so that the signal used by the phase detector is at 19.096 MHz. The reference input to the phase detector is normally provided by a high stability temperature compensated crystal oscillator. The reference input to the phase detector (pin 18) has an input sensitivity of 400 mV_{pp} minimum and 2.5 V_{pp} maximum. The phase detector in the MRFIC1502 is based on the Motorola MC12040 design with some modifications to reduce power consumption and complexity.

The loop filter design is the standard op–amp loop filter, resulting in a type II second order loop. The detailed configuration of the loop filter is shown in Figure 4.

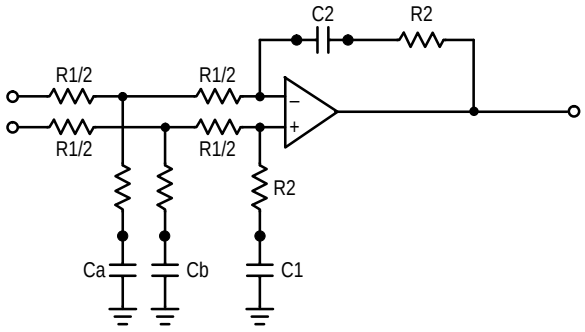


Figure 4. Loop Filter

The parameters required to calculate the external capacitor values for the loop filter are as follows.

K_ϕ = 0.16 volt/radian
K_V = 20 MHz/volt
R1 = 890 ohms
R2 = 1020 ohms
N = 80

Given the above information, the calculation of the capacitors Ca, Cb, C1 and C2 is straight forward. The loop natural frequency, ω_n, and the damping factor, ς, are usually chosen given the requirements of the synthesizer for phase noise, loop–lock time, and transient response.

Because R1 and R2 are given, the only variable is the capacitor value for C1 and C2, which are identical. This capacitor value is:

$$C1 = C2 = \frac{K_\phi K_V}{N\omega_n^2 R1}$$

With the calculated value of the capacitors C1 and C2, the damping factor should be re–calculated to ensure that the loop will be stable. The damping factor is calculated with the following equation.

$$\varsigma = \frac{R2\omega_n C1}{2}$$

The choice for the value of the capacitor Ca and Cb is dependent on how much additional rejection of the reference spurs is required. The cut–off frequency of this additional pole should be placed at least five to ten times the loop natural frequency. The calculation of the capacitor values Ca and Cb is as follows.

$$Ca = Cb = \frac{4}{R1\omega_c}$$

The layout of the discrete components around the loop filter and VCO is very critical to the performance of the phase–locked loop. Much care should be taken in routing the VCO control voltage line from the output of the loop filter to the varactor diode. If this line picks up any noise, it will appear as a deviation in the frequency of the VCO and will reduce the sensitivity of the receiver.

SAMPLING CLOCK OUTPUT

The output of the divide by 40 is buffered by a clock translator that converts the low level sine wave into a TTL level square wave. This TTL level signal is used by the digital correlator and decimator as a sampling clock and to generate all the necessary internal clocks. Because this translator is operating at 38 MHz and the output is a square wave with very sharp edges, the loading on the supply to the buffer is very high. The peak currents can reach as high as 50 mA with the maximum load of 1.0 kΩ in parallel with 40 pF on the output. Therefore, the translator has a dedicated V_{CC} supply, pin 28, which requires external bypassing and isolation. The recommended bypassing uses two capacitors in parallel, a 47 pF and a 0.01 μF capacitor.

GENERAL LAYOUT RULES

The physical location of the bypass capacitors should be replicated as closely as possible. The signal flow is such that the part layout is very simple and straight forward. The layout is such that some of the critical components are placed on the back side of the MRFIC1502 in order for the physical path from the MRFIC1502 to these parts is as short as possible.

The resistance to jamming can also be affected by the location of the VCO resonating structure. If a distributed element is chosen rather than the lumped inductor, there is a chance that some coupling between the L–band input and the resonator will occur due to the close proximity of the pins on the package. If there is coupling, the receiver will be very sensitive to any jammers at the VCO frequency due to the energy from the jamming signal coupling into the VCO and pulling it off frequency. In order to minimize this coupling, a stripline structure should be used rather than microstrip.

DIGITAL CORRELATOR

Information on the correlator chip is available by contacting the Motorola RF Semiconductor Marketing organization.

CONCLUSION

This application note decribes one way the MRFIC1502 can be used in GPS receivers. The external circuitry described in this application note can be optimized to satisfy a variety of specific design requirements. For additional technical information about the MRFIC1502 or other devices descibed in this application note, contact Motorola RF Semiconductor Marketing or your local Motorola Sales office.

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