AN1672

The ECL Translator Guide

ECL • TTL • PECL • LVECL • LVPECL • CMOS • LVTTL
How To Make Them Talk To Each Other

Are You Designing with Different I/O Levels?

This document guides you to the appropriate interface.

For interfacing between ECL devices and the TTL / CMOS world discrete interfaces could be used. But the switching points are usually not controlled and may vary with temperature, device variation, or supply voltage. This results in duty cycle variation. To avoid this signal quality uncertainty translating devices with controlled switching levels and specified propagation delays and skews are available.

Translation between ECL signals off different power supplies might be done by capacitive coupling. But this is only possible for clock signals or RZ coded signals. For this reason special translators are available.

If you are looking for interfaces between LVDS and ECL, please see the application note AN1568 "Interfacing Between LVDS and ECL".

You will find the right device for your application in the translator matrix on page 3. The tables give you additional information on the bit–width and the databook location.

Translators from TTL–World to ECL–World

TTL to ECL Translators (Dual Supply +5 V, −5 V)

Width	Device	Function	Databook
1	MC10/100ELT24	TTL to Differential ECL	DL140
4	MC10124	Quad TTL to MECL	DL122
4	MC10H124	Quad TTL to MECL with TTL Strobe	DL122
4	MC10H424	Quad TTL to PECL with ECL Strobe	DL122
6	MC10/100H604	Registered Hex TTL/ECL	DL122
9	MC10/100H600	9 Bit TTL/ECL	DL122
9	MC10/100H602	9 Bit Latch TTL/ECL	DL122

TTL/ECL Transceiver (Dual Supply +5 V, −5 V)

Width	Device	Function	Databook
4	MC10/100H680	4 Bit Differential ECL Bus/TTL Bus Transceiver with Latches	DL122

TTL to PECL (Single Supply +5 V)

Width	Device	Function	Databook
1	MC10/100ELT20	TTL to Differential PECL	DL140
2	MC10/100ELT22	Dual TTL to Differential PECL	DL140
4	MC10H351	Quad TTL/NMOS to PECL	DL122
6	MC10/100H606	Registered Hex TTL/PECL	DL122

LVTTL to LVPECL (Single Supply +3.3 V)

Width	Device	Function	Databook
2	MC100LVELT22	Dual LVPECL to LVTTL	WWW

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Translators from ECL–World to TTL–World

ECL to TTL (Dual Supply +5 V, −5 V)

Width	Device	Function	Databook
1	MC10/100ELT25	Differential ECL to TTL	DL140
4	MC10125	Quad MECL to TTL	DL122
4	MC10H125	Quad MECL to TTL	DL122
4	MC10/100H660	4 Bit ECL TTL Load Reducing DRAM Driver	DL122
6	MC10/100H605	Registered Hex ECL/TTL	DL122
9	MC10/100H601	9 Bit ECL/TTL	DL122
9	MC10/100H603	9 Bit Latch ECL/TTL	DL122

PECL to TTL (Single Supply +5 V)

Width	Device	Function	Databook
1	MC10/100ELT21	Differential PECL to TTL	DL140
2	MC100ELT23	Dual Differential PECL to TTL	DL140
4	MC10H350	Differential PECL to TTL	DL122
6	MC10/100H607	Registered Hex PECL/TTL	DL122

LVPECL to LVTT (Single Supply +3.3 V)

Width	Device	Function	Databook
2	MC100EPT23	Dual Differential LVPECL to LVTTL	WWW

PECL–TTL and TTL–PECL (Single Supply +5 V)

Width	Device	Function	Databook
1+1	MC10/100ELT28*	TTL to Differential PECL + Differential PECL to TTL	DL140

CMOS to PECL Interfacing

	Width	Device	Function	Databook
CMOS to PECL (Single +5 V)	4	MC10H352	Quad CMOS to PECL	DL122

Different Supplied ECL

	Width	Device	Function	Databook
LVECL to PECL (−3.3 V to +5 V)	3	MC100EL90	Triple ECL to PECL	DL140
LVECL to LVPECL (−3.3 V to +3.3 V)	3	MC100LVEL90	Triple ECL to LVPECL	DL140
LVPECL to ECL (−3.3 V to MECL)	3	MC100EL91	Triple LVPECL to ECL	DL140
LVPECL to LVECL (+3.3 V to −3.3 V)	3	MC100EL91	Triple LVPECL to LVECL	DL140
PECL to ECL (+5 V to MECL)	3	MC100EL91	Triple PECL to LVECL	DL140
PECL to LVECL (5 V to −3.3 V)	3	MC100LVEL91	Triple PECL to LVPECL	DL140
PECL to LVPECL (5 V to +3.3 V)	3	MC100LVEL92	Triple PECL to LVPECL	DL140
ECL to PECL (MECL to +5 V)	3	MC100EL90	Triple ECL to LVPECL	DL140
ECL to LVPECL	3	MC100LVEL90	Triple ECL to LVPECL	DL140

Translator Matrix

From/To	TTL VCC = +5 V	ECL VEE: −4.5/−5.2 V	PECL VCC = +5 V	LVTTL VCC = 3.3 V	LV–ECL VEE = −3.3 V	LVPECL VCC = +3.3 V	CMOS VDD = +5 V
TTL VCC = +5 V	—	MC10124 MC10H124 MC10H424 MC10/100H600 MC10/100H602 MC10/100H604 MC10/100H680* MC10/100H681* MC10/100ELT24	MC10H351 MC10/100H606 MC10/100ELT20 MC10/100ELT22 MC10/100ELT28*	Use of devices with 5 V tolerant inputs or clamped VIH to 3.3 V	MC100LVEL91 interface (+3.3 V required; VIH clamped to 3.3 V)	MC100LVELT22 With VIH limited to VCC = 3.3 V	Pull up resistor
ECL VEE =−4.5/ −5.2 V	MC10125 MC10H125 MC10/100H601 MC10/100H603 MC10/100H605 MC10/100H660 MC10/100H680* MC10/100H681* MC10/100ELT25	—	MC100EL90	—	MC100EL91	MC100LVEL90	ECL/TTL Translator to HCT or ACT input
PECL VCC = +5 V	MC10H350 MC10H607 MC10/100ELT21 MC100ELT23 MC10/100ELT28*	MC100EL91	—	MC100LVEL92 + MC100LVELT23	MC100EL91	MC100LVEL92	PECL/TTL Translator to HCT or ACT input
LV–TTL VCC = 3.3 V	Direct connection, as DC levels are identical	MC100EL91	MC100LVELT22 +5 V PECL line receiver	—	MC100LVEL91 + MC100LVELT22	MC100LVELT22	Pull up resistor
LVECL VEE = −3.3 V	—	Direct connection, as DC levels are identical	MC100EL90	—	—	MC100LVEL90	ECL/TTL Translator to HCT or ACT input (−5 V required)
LVPECL VCC = +3.3 V	—	MC100EL91	ECL line receiver, e.g. MC100EL17	MC100EPT23	MC100EL91	—	—
CMOS VDD = 5 V	Direct connection	MC10H352 + MC100EL90	MC10H352	Via LCX	MC10H352 + MC100EL90	LCX + MC100LVELT22	—

*Bidirectional

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