AN1675

A Low Noise Amplifier with High IP3 for the 900 MHz Band Using the MRF1057T1 Low Noise Transistor

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INTRODUCTION

This Application Note describes the performance of the Motorola MRF1057T1 low noise bipolar transistor in a LNA circuit.

The Motorola MRF1057T1 is a low noise bipolar junction transistor, which, along with the MRF1027T1 and MRF1047T1 comprise a family of sub–micron geometry devices. The main difference between these devices is their current carrying capabilities.

The MRF1057T1 has a 12 GHz peak transition frequency, f_τ, 1.0 dB minimum noise figure, NF_{min}, and a maximum of 28 dBm for the output third order intercept, OIP3. This transistor is housed in the industry standard SC–70 package and is well suited for the new generation of low voltage, high frequency wireless applications.

DESIGN REQUIREMENTS

The requirements of this design are typical of the most recent cellular communication technologies such as CDMA and TDMA. The design demonstrates 11 dBm input IP3 performance with 1.3 dB noise figure and a power consumption of less than 40 mW.

The requirements are as follows:

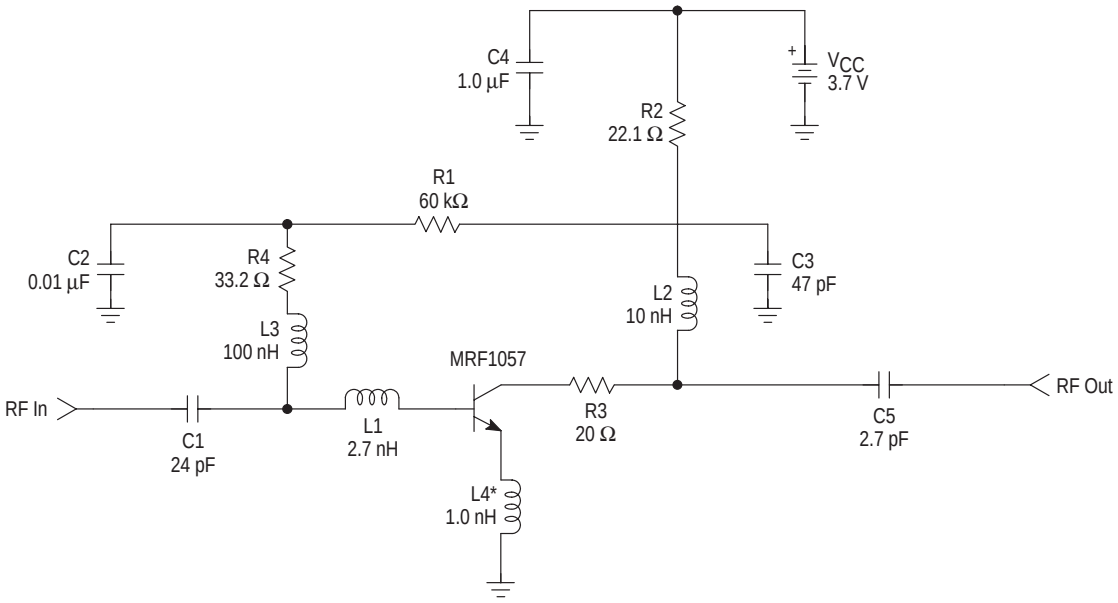
Supply Voltage:	3.7 V
Current:	10 mA
Frequency Range:	870 to 900 MHz
Bias level:	3.7 V
Noise figure:	1.3 dB
Gain:	11 dB
Input Return Loss:	–12 dB
Output Return Loss:	–15 dB
Input IP3:	11 dBm
Stability:	Unconditional stability

The MRF1057T1 is chosen for this application because of its high linearity at the required bias and its low noise resistance, which makes the impedance match easier and simpler.

CIRCUIT DESIGN

The LNA circuit is designed using the MRF1057T1 Spice Gummel–Poon model, which includes the package parasitics of the SC–70. Model details are given on the data sheet.

Figure 1. LNA Using the MRF1057TI

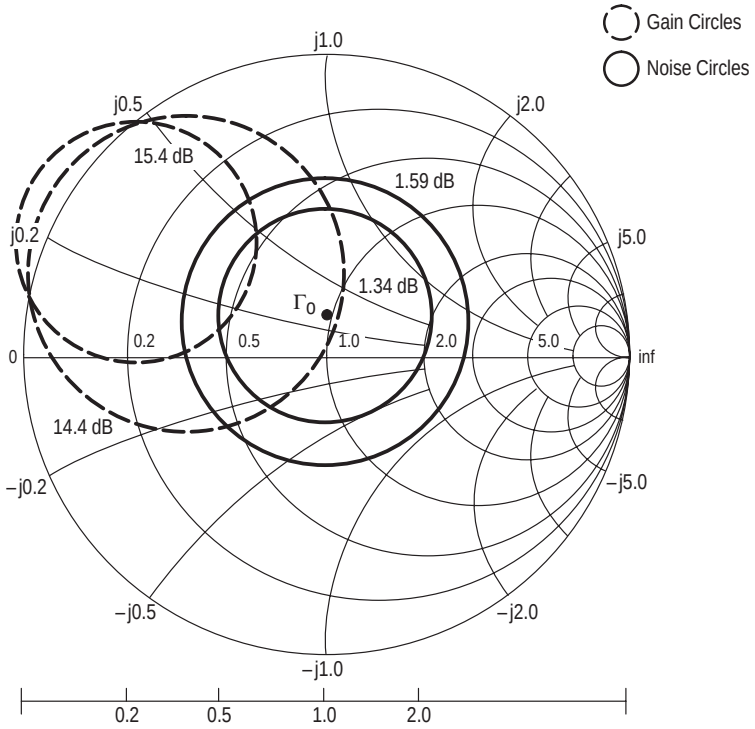


The bias network is designed using passive components. This circuit is not designed to provide bias stability over temperature. Improved stability over temperature and reduced variation in amplifier performance due to the variation in device current gain, h_{FE}, can be achieved by using active bias circuitry. Motorola's MDC5001 is a single chip bias stabilizer that can provide the desired stabilization over temperature. The bias scheme for this LNA uses a single collector resistor of 22 Ω and a base resistor of 60 kΩ fed through the collector resistance. This stabilizes the collector current to 10 mA, ±20% for h_{FE} ranges of 100 to 200.

The emitter is tied to ground through a 1.0 nH inductor to bring the optimum reflection coefficient, gamma optimum (Γ_O), closer to S_{11}*. This results in an improvement in the NF and input return loss tradeoff. It also improves IP3 by 1.5 dB, as observed in simulations. Figure 2 shows the noise and gain circles without emitter inductance, and Figure 3 includes the emitter inductance.

The amount of inductance must be carefully weighed against its negative effect on other parameters such as gain and stability. Higher emitter inductance can cause out of band oscillation.

Figure 2. Noise and Gain Circles



V_{CE} = 3.0 V
I_C = 10 mA

f (MHz)	NF_{min} (dB)	Γ_O	G_{amax} (dB)
900	1.09	0.146 ∠ 89.9°	16.4

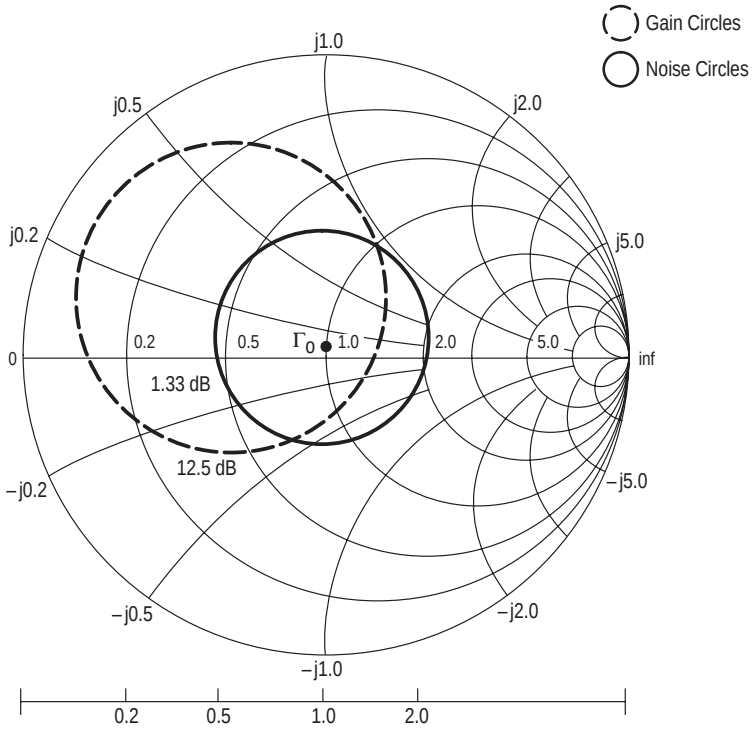
The input is matched to provide the lowest noise figure for at least –12 dB input return loss (IRL). The optimum source impedance, Γ_O, to achieve minimum noise figure is very close to 50 Ω. It has a magnitude of 0.09 and an angle of 93.1°. This is one of the advantages of the MRF1057T1 — its input can be terminated in 50 Ω and still have excellent performance. The noise figure is 1.2 dB for an unconditionally stable design and for an IRL better than –12 dB.

The input match consists of a 2.7 nH series inductor, but as noted, the input can be terminated to 50 Ω and still have comparable performance. A blocking capacitor is in series with the inductor to prevent the dc from affecting adjacent circuitry. The base dc is fed through a 100 nH shunt inductor, which enhances the IP3 performance of the LNA.

The output is matched to achieve the best IP3 while maintaining low noise performance and at least –15 dB output return loss (ORL). Using the circuit simulator a load pull test was done to plot the IP3 contours. The best IP3 is 24.8 dBm, with a magnitude of 0.52 and an angle of 30°.

The output match consists of a 10 nH parallel inductor, which serves as a bias feed, followed by a 2.7 pF series capacitor, which blocks dc from affecting adjacent circuitry. This match yields the best IP3 for the required ORL, gain and noise figure.

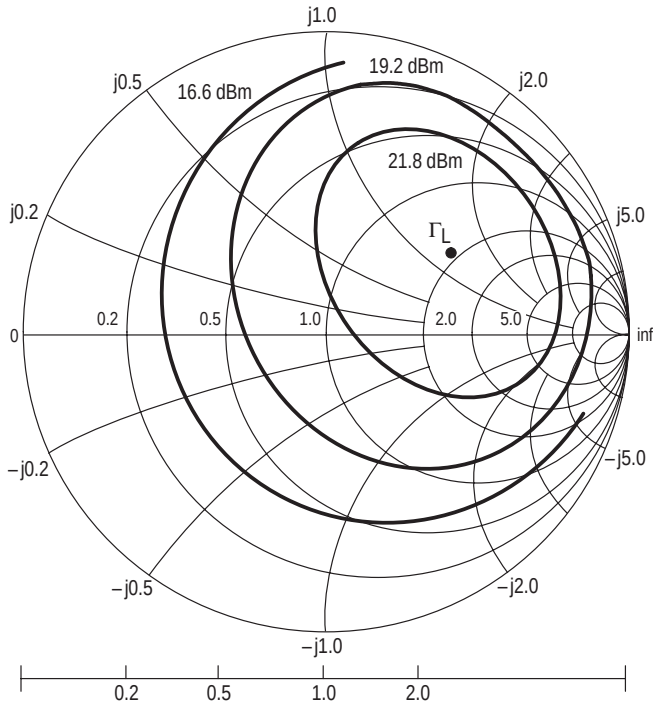
Figure 3. Noise and Gain Circles with 1.0 nH Emitter Inductance



V_{CE} = 3.0 V
I_C = 10 mA
with 1.0 nH Emitter Inductance

f (MHz)	NF_{min} (dB)	Γ_o	G_{amax} (dB)
900	1.08	0.09 ∠ 93.1°	13.5

Figure 4. IP3 Contours



V_{CE} = 3.0 V
I_C = 10 mA

f (MHz)	$IP3_{max}$ (dB)	Γ_L
900	24.8	0.52 ∠ 30°

An important requirement of the design is stability. As mentioned, increasing the emitter inductance affects stability as do the parasitics of the components and the board. Stability could be improved by making the device more unilateral, that is by decreasing the feedback through the collector–to–base capacitance and/or adding resistance to the input or output of the device. The major disadvantage of using a resistor in the output of the device is degradation in gain and IP3. Use of a resistor affects noise figure as well, with the degree of degradation dependent on the reverse transmission insertion gain. Another option is to place a series resistor in the input at the expense of noise figure. Since the LNA was intended to provide gain while adding minimum noise, a 20 Ω series resistor is inserted in series at the output of the device and no resistor is placed in the input. This helps prevent oscillation, especially at higher frequencies.

An amplifier with high gain at low frequencies, that may be unconditionally stable according to the simulator, may oscillate if the output can radiate back to the input. Therefore, a resistor, R4 (Figure 1), is used to provide circuit stability at low frequencies. If the proper value is chosen it will not affect the performance of the LNA. Another option to improve the stability of the LNA is inserting a shunt capacitor in the base and/or in the collector that will result in a RF short at the frequency where oscillation is occurring.

BOARD LAYOUT AND LIST OF COMPONENTS

Component selection plays an important role in the design. Characteristics such as tolerance, Q, and resonant frequency must be carefully chosen. Improper selection of components or board material may cause the design to fall short of meeting the required performance and may increase the possibility of oscillation. Figure 5 shows the printed circuit board layout and parts placement and Table 1 shows the list of components used on the LNA demo board.

Figure 5. PCB Layout and Parts Placement

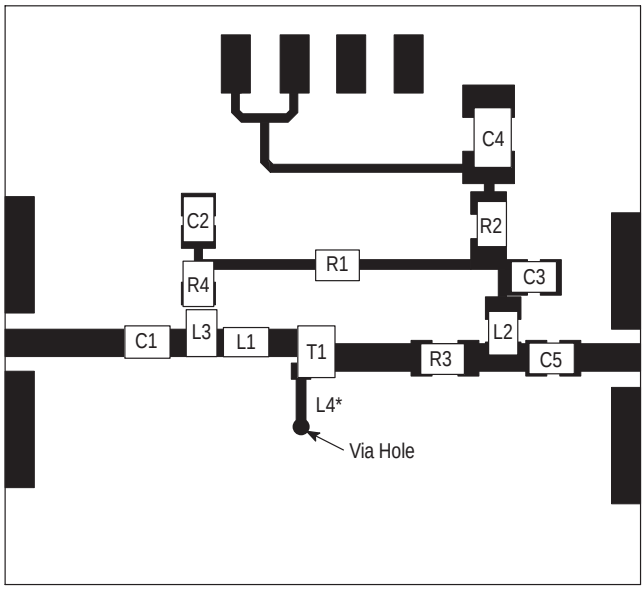


Table 1. List of Components

Component	Value	Comments
C1*	24 pF	DC Block
C2*	0.01 μF	Improve IP3
C3*	47 pF	900 MHz Short
C4*	1.0 μF	RF Short
C5*	2.7 pF	Output Match and DC Block
L1**	2.7 nH	Input Match
L2**	10 nH	Output Match
L3**	100 nH	DC Feed and Improve IP3
L4	1.0 nH	100 mil x 15 mil (Printed Inductor)
R1***	60 kΩ	Bias
R2***	22.1 Ω	Bias
R3***	20 Ω	Stability
R4***	33.2 Ω	Stability
Via		D = 15 mil, H = 25 mil
Substrate	FR4	ε_r = 4.5, H = 25 mil, T = 1.5 mil

* ATC chip caps: 100 A series, case size: 0.055″ x 0.055″, Q: >10000 @ 1.0 MHz.
** Toko chip inductors: LL2012 series, 0805 package.
*** KOA Speer flat chip resistors, Part#: RK73H2A–F, 1% tolerance, 0805 package.

LNA PERFORMANCE

This LNA design offers excellent linearity, very low noise figure with good input and output return loss. It exhibits an input VSWR of 1:1.33 and an output VSWR of 1:1.12. It has a noise figure of only 1.2 dB and is extremely linear, with more than 23 dBm of output IP3, which translates to over 11 dBm input IP3. This surpasses the input IP3 requirement of the majority of the applications, such as CDMA, which requires about 8.0 dBm input IP3. Another way to understand the linearity of this LNA is by using the 1.0 dB compression point (P_{1dB}) parameter, which specifies the output power where the linear gain is 1.0 dB below its projected value. As a general rule of thumb the P_{1dB} of a LNA is 10 dB below the output IP3. This LNA has a 13 dBm output power when gain is compressed by 1.0 dB, which is much better than most wireless application requirements at 900 MHz.

The measured gain of this LNA is 11.9 dB, which is excellent for cellular, paging and cordless applications. Excessive gain in the LNA can cause intermodulation problems in the mixer stage and might increase the difficulties in meeting the mixer design requirements. It will also degrade the input third order intercept for a given output third order intercept.

This LNA was designed using the Spice Gummel–Poon model for the MRF1057T1. The simulated results compare favorably with the measured values. None of the matching networks needed to be fine tuned in the circuit, demonstrating the accuracy and reliability of the MRF1057T1 model.

Figure 6. Simulated IRL and ORL

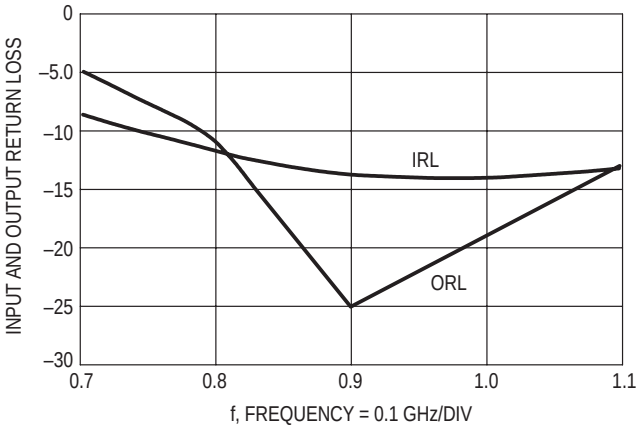
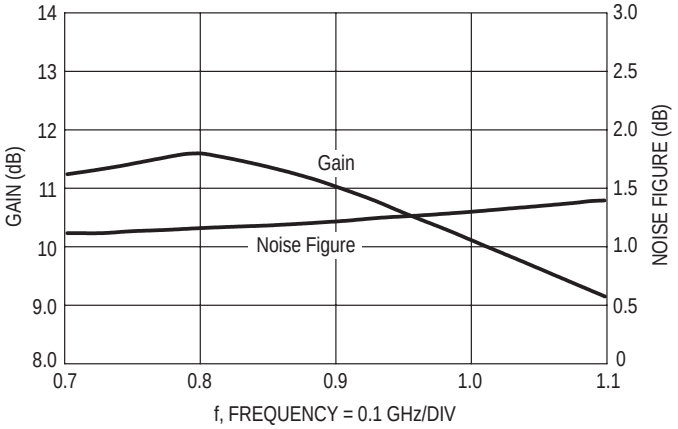


Figure 7. Simulated Gain and Noise



Detailed simulated RF performance is shown in Table 2.

Table 2. Simulated RF Performance

Frequency (MHz)	S[1,1] (dB)	S[2,1] (dB)	S[2,2] (dB)	NF (dB)	OIP3 (dBm)
870	–12.7	11.4	–18.3	1.2	23.3
900	–13.2	11.2	–25	1.21	23.9

The results obtained from the characterization of the circuit are shown in Table 3.

Table 3. Measured RF Performance

Frequency (MHz)	S[1,1] (dB)	S[2,1] (dB)	S[2,2] (dB)	NF (dB)	OIP3 (dBm)
900	–17	11.9	–25	1.35	23.4

CONCLUSION

This high performance LNA circuit was designed using the Motorola MRF1057T1 device. The LNA circuit demonstrated the performance of the MRF1057T1 for an unconditionally stable, low power consumption, low noise, high IP3 design. The Motorola MRF1057T1 is well suited for the new generation of low voltage, high frequency wireless applications.

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