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Get Your Best From Your LDO Designs

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Introduction

Thanks to their weak insertion losses, Low DropOut regulators (LDOs) occupy a place of choice in battery operated systems. If the dropout was of main concern over the past years, increasing marketing requirements for new generation devices have highlighted other LDO parameters. In this area, output noise, ripple rejection and quiescent current are among the designers most wanted numbers. Unfortunately, obtaining the essence on these parameters implies that you fully understood the way an LDO is built and how it will accommodate to your application. This article details the nitty–gritty of these new high performance regulators thus giving you the ability to predict their behaviors when dropped into the final circuit. This learning stage is essential when design cycles could be as low as 6 months.

The LDO is a series regulator

A linear regulator will always deliver an output voltage lower than its input's. Several possibilities are offered to the designer to implement this kind of device. The most common solution uses an element working as a variable resistor. The resistor could be connected in series with the input source (**Figure 1a**, series regulator) or across the load (**Figure 1b**, shunt regulator).

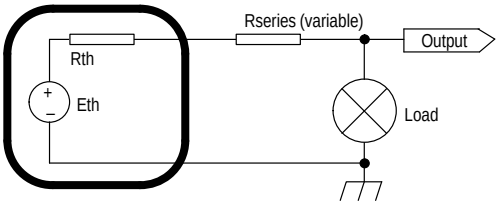


Figure 1a

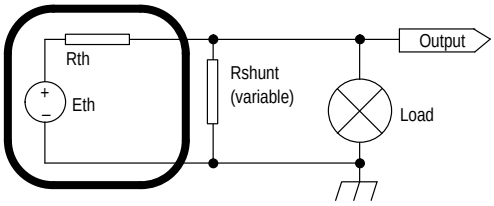


Figure 1b

Figure 1. Two concepts in regulator designs: series or shunt

Since the shunt version is not very popular, except with current sources like solar arrays, we will concentrate our study on series regulators.

As one can see from **Figure 1a**, the series element, also called a ballast, has to permanently sustain the difference between the input and the output voltage. Since the load current runs through this resistor, you can easily define the power it dissipates in heat: $P_{loss} = (Vin - Vout).Iout$. The voltage difference is called the dropping voltage and will condition the maximum power the LDO's package will be able to safely dissipate.

A variable resistor can be implemented by using a transistor either bipolar or MOSFET. For the sake of clarity, we will stick to the bipolar solution. **Figure 2** details a classical ballast stage made around an NPN transistor driven by a PNP element, e.g. the output stage of an error amplifier.

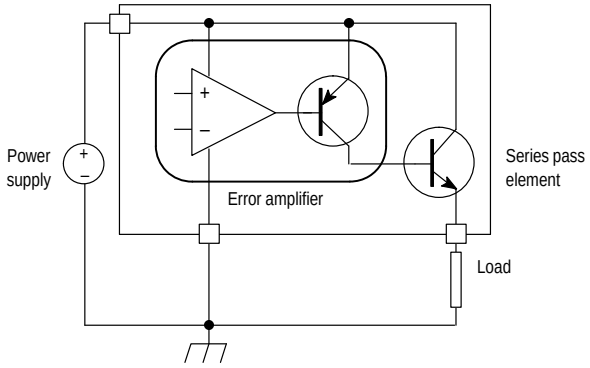


Figure 2. A classical bipolar regulator architecture

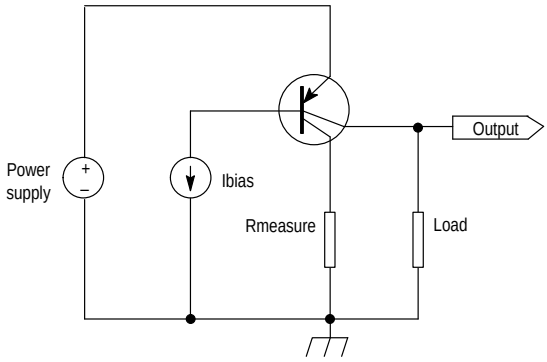


Figure 3. A PNP overcomes the floating emitter issue

The NPN receives its bias current from the input rail through the PNP transistor. This bias current is then evacuated via the emitter and contributes to the output current. To ensure a proper operation, the biasing circuit shall keep the base potential always above the emitter's. When the input to output differential is high, there is obviously no problem. But if we now decrease the input voltage close to the output value, the control circuit pushes the series pass element toward saturation to ensure a proper operation of the regulator: the transistor equivalent resistor diminishes. Unfortunately, this equivalent resistor cannot decrease indefinitely simply because it is now harder to maintain the transistor's Vbe. As a result, the component is unable to keep the regulation and the output voltage drops. Actually, we are in the configuration of a high–side switch where the emitter or source (with an N–channel MOSFET) requires the addition of a separate floating power–supply. This can be done with the bootstrap technique, like in half–bridge based applications, but it would be difficult to implement it in a low–noise linear regulator. With figure 2's drawing, the minimum differential voltage within regulation will not go lower than VCE_{SAT}(PNP) + VBE(NPN). If we take 200 mV for the PNP and nearly 600 mV for the NPN, we reach a dropout of 800 mV, an unacceptable value for battery operated systems. In 78XX series, a resistive shunt was offering a current protection to the circuit but, again, contributed to degrade the overall voltage drop.

Use PNPs as high–side switches

Since the NPN's emitter is floating in figure 2's sketch, why not reversing the bipolar and securing its emitter to the supply rail? In that case, a floating supply is no longer needed and the bias path via the ground is immediate. **Figure 3** describes this last solution implementing a PNP transistor. The control toward saturation is now easier since all the input supply dynamic is available. Compared to the NPN solution, the dropout is the PNP's saturation voltage VCE_{SAT} or $RDS_{(ON)}$. Id with a MOSFET. By selecting a high–gain series transistor, dropouts as low as 60 mV @ 100 mA can be obtained. If you look at figure 3, you will note that the bias current is now evacuated through the ground and does no longer contribute to the output current. This is a typical characteristic of bipolar LDOs called the *ground current*, as highlighted in the data–sheets. The value of this ground current is directly dependent on the series transistor gain.

Now that we achieved a small dropping voltage, it would be a pity to degrade it with a shunt element. For that purpose, a multi–collector transistor will provide the necessary cells to sense a fraction of the output current and feed it back to a protection loop.

Analysing the LDO stability

Figure 4 details the internal structure of an LDO like the MC33264 from MOTOROLA (Phoenix, AZ). The series element is physically disconnected from the error amplifier for sake of clarity, but it is actually part of the error amplifier output stage.

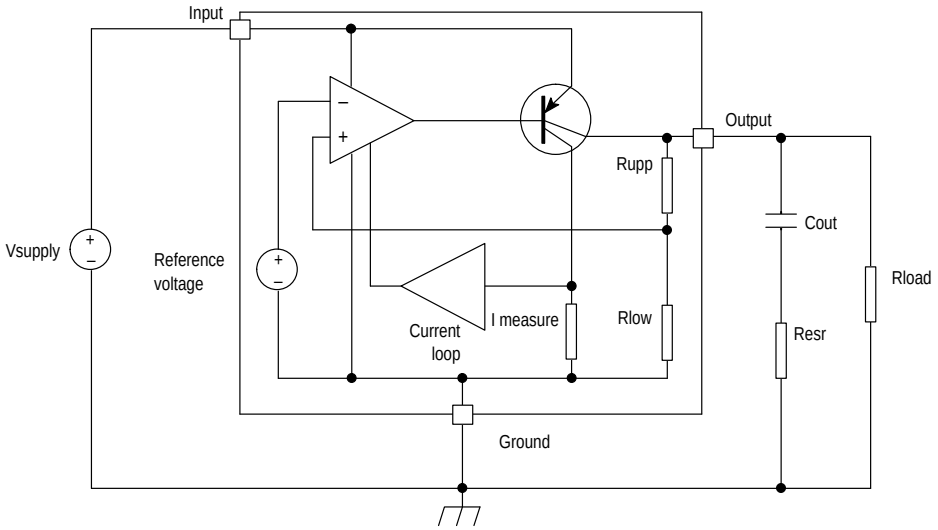
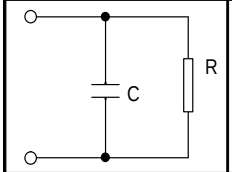
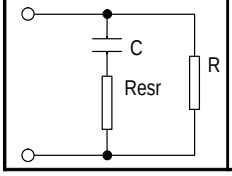


Figure 4. A simplified version of a bipolar LDO

The closed–loop output voltage calculation is straightforward and equals: $Vref \times \left(1 + \frac{Rupp}{Rlow}\right)$. The trimming of the output voltage can be done at the final test before assembly by fusing some calibrated resistors. The influence of the resistors stability on the output voltage is evaluated by summing the partial derivatives of the above expression to the feedback elements, $\frac{\partial Vout}{\partial Rupp} + \frac{\partial Vout}{\partial Rlow}$, which leads to a maximum error of: $\frac{Vref}{50} \times \frac{Rupp}{Rlow}$ V/%.

The voltage and current loops stability analysis requires the determination of the overall loop gain whose pole/zeroes will depend, among other parameters, on the nature of the charge. The following table details their location for two different load combinations:

Load nature	Pole location	Zero location
	$\frac{1}{2 \times \pi \times R \times C}$	–
	$\frac{1}{2 \times \pi \times (R + Resr) \times C}$	$\frac{1}{2 \times \pi \times (Resr) \times C}$

The series pass element can be seen as a transconductance generator where $gm = \frac{\partial Ic}{\partial V_{BE}}$. In that case, the following transfer function for the voltage loop, excluding the error amplifier, can be derived from figure 4, where the capacitor's Equivalent Series Resistor (ESR) is clearly indicated:

$$\frac{Vout}{V(pin+)} = \frac{gm \times Rload \times (1 + sz1)}{1 + sp1} \times \left(\frac{Rupp}{Rupp + Rlow}\right)$$

$z1 = Resr \cdot Cout$

$p1 = (Rload + Resr) \cdot Cout$

The series pass bipolar transistor also exhibits a high frequency pole F_P who links its static low–frequency β to the transition frequency f_T by: $F_P = \frac{F_T}{\beta}$. This pole finds its origin from several phenomena but in well designed high–frequency transistors, the emitter time constant and the base transit time are the most important factors to account for [1]. Depending on the output current, one term is stronger than the other. For instance, at low current, the dynamic emitter resistance r_e is rather high and dominates the frequency response of the component. When you now increase the collector current, the r_e effect starts to be negligible until the second term takes the lead. When the current is further increased, the base widens and consequently makes f_T decrease. **Figure 5** shows how f_T typically varies with the collector current of a small–signal PNP transistor.

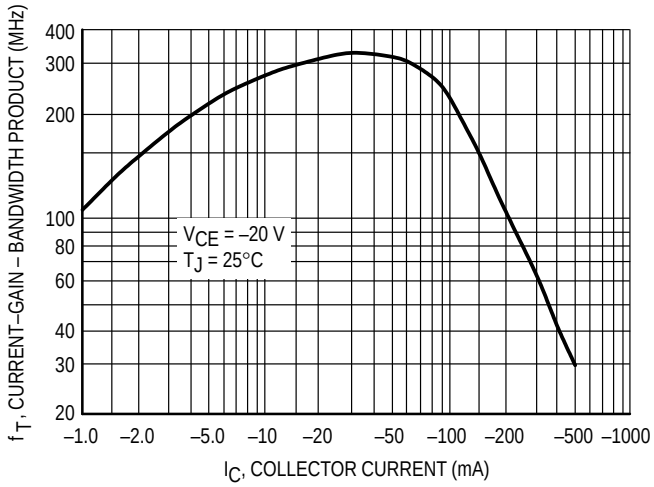


Figure 5. Typical f_t variations of the MPS2907

High–current LDOs make use of large output transistors where the added pole needs to be accounted in the stability analysis. Fortunately, small transistors used in low current devices naturally push the pole toward high frequencies and thus exclude it from the bandwidth of study.

As you can see from the transfer equation, there is no inherent pole except the one introduced from the output capacitor. This last element is fundamental in the LDO stability point of view. Without it, there would be no element to roll–off the gain to 0dB at reasonable frequencies thus jeopardizing the regulator stability in the upper portion of the spectrum. Please note that figure 4 is an oversimplified LDO schematic for explanation purposes. Final designs include complex compensation networks put at strategic places to ensure the device stays stable whatever load it sees.

Too much of ESR degrades stability

Drawing the Bode plot of an LDO could be undertaken with a network analyzer. However, studying the impact of external elements upon the phase margin or the open–loop gain can rapidly become tedious and lead to prohibitive analysis times. In this aspect, a SPICE simulator, like INTUSOFT's IsSpice4 (San–Pedro, CA) offers the required flexibility to quickly assess how an electrical parameter will evolve in function of various influences. **Figure 6a** depicts a simplified model of an LDO.

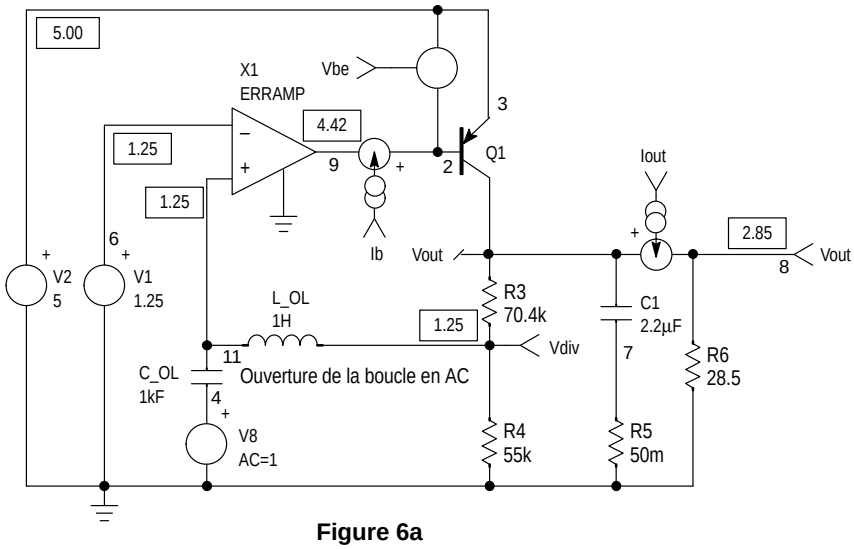


Figure 6a

Figure 6. IsSpice4 LDO simulation schematic

As with any closed–loop systems, the Bode plot depends on the operating point and shall be kept before any frequency sweep. This is the purpose of the L_OL and C_OL elements which open the loop in AC but let the DC current circulate, thus closing the loop. **Figure 6b** shows the result of the sweep where the instability is

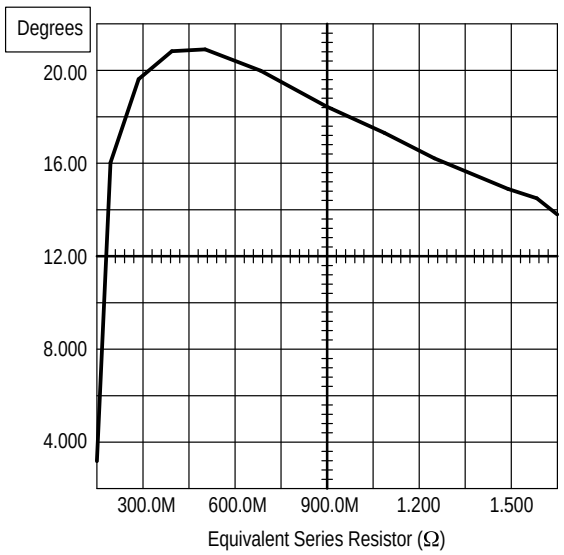


Figure 6b The Bode plot of figure 6's example reveals a null phase margin

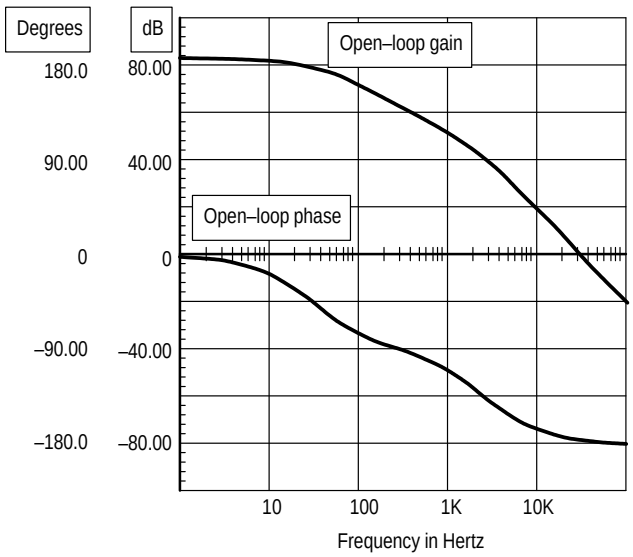


Figure 6c Adding some ESR provides the system with phase margin

obvious: the phase margin is null! If we now introduce a zero with the help of the capacitor's ESR, we will brake the –2 slope to a –1 somewhere, depending on the zero location. Crossing the 0dB axis with a –1 slope ensures an adequate phase margin. However, pushing the zero location toward low frequencies eases its action and it no longer acts as it should. **Figure 6c** shows how the ESR improves the system stability but at a certain point, it tends to degrade it. For this reason, MOTOROLA always specifies an ESR range within which his regulator is stable. A well designed regulator accepts ESR between a few tens of mΩ and 5Ω.

My regulator acts like a coil

It is a little known that the output impedance of an LDO exhibits an inductive part when the excitation frequency goes beyond the regulator bandwidth. The output impedance of a closed loop device Z_{Ocl} depends on its open–loop gain, A_{OL}, following the formula: $Z_{Ocl} = \frac{Z_{Ool}}{1 + A_{OL}}$. At low frequency, where the gain is high, the output impedance stays low and resistive. If the gain starts to decrease, Z_O correspondingly increases as **Figure 7** depicts from an IsSpice4 simulation.

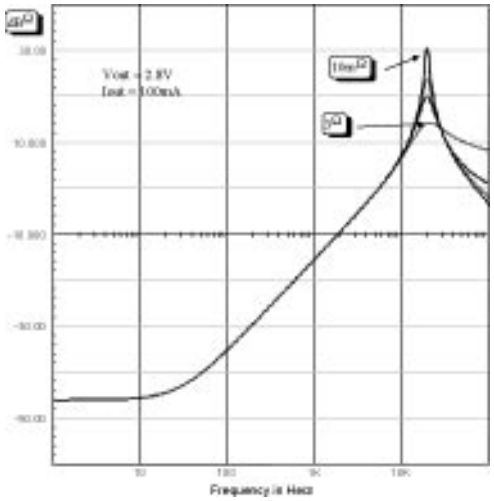


Figure 7. The LDO's output impedance is reactive at high frequencies

In the example, the equivalent inductive part reaches 26µH at an output current of 100 mA. If no precautions are taken, the combination of the output capacitor and this equivalent coil can naturally lead to resonance problems. As expected, the ESR affects the quality coefficient of the resulting tank. Do not be surprised if you observe some noise peaks in certain portion of the spectrum, as well shown by Erroll DIETZ in Robert PEASE's book [2].

Dropout and ripple rejection

The ripple rejection is a very important parameter for battery operated systems. If the regulator excels in this particular point, it will offer a natural shield to the downstream electronics against choppy DC rails. As for the output impedance, the audiosusceptibility (AS) is affected by the open–loop gain by: $AS_{cl} = \frac{AS_{ol}}{1 + A_{OL}}$. This explains the good behavior of regulators in the lower portion of the spectrum while it tends to degrade when operating at higher frequencies. Another parameter which is rarely taken into account is the dropping voltage used during this ripple measurement. As we previously said, the series pass element works as a variable resistor. When the differential Vin–Vout is high, the transistor equivalent resistor is large. You can thus imagine that the regulator has little difficulty to isolate the output from the input perturbations and the ripple rejection is good. If you now decrease the dropout, you move the transistor operating point toward low VCEs at higher base current where its conductance $(\frac{\partial Ic}{\partial V_{CE}})$ tends to degrade seriously. As a matter of fact, the LDO can no longer maintain the required ripple rejection, as **Figure 8** portraits for a typical LDO excited at 100 kHz.

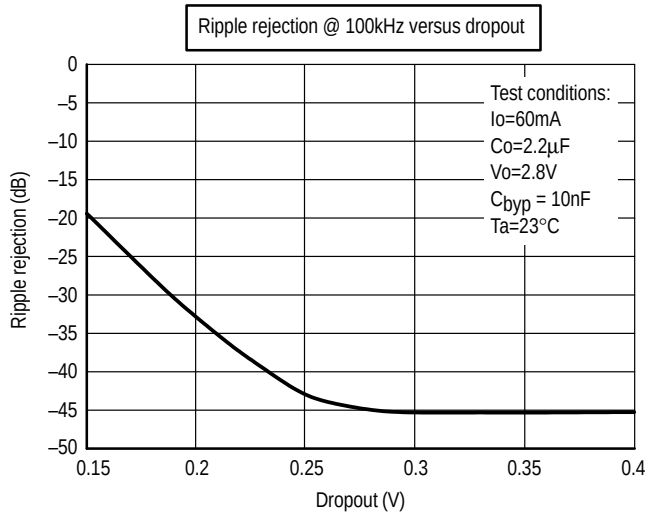


Figure 8. At very low dropouts, the ripple rejection is degraded

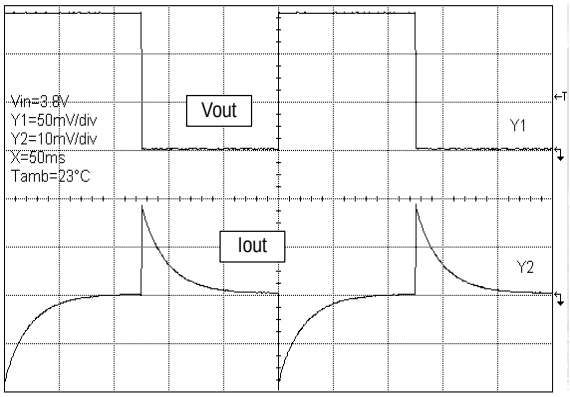


Figure 9. Transient response of an LDO (I_O=3mA to I=150mA)

When doing these measurements, you must avoid any input to output parasitic couplings, for instance via the differential voltmeter.

Don't slip on the slope!

The quality of the response time is related to many parameters, among which the closed–loop bandwidth with the corresponding phase margin play an important role. However, other characteristics also come into play like the series pass transistor saturation. When a current perturbation suddenly appears on the output, e.g. a load increase, the error amplifier reacts and actively biases the PNP transistor. During this reaction time, the LDO is in open–loop and the output impedance is rather high. As a result, the voltage brutally drops until the error amplifier effectively closes the loop and corrects the output error. When the load disappears, the opposite phenomenon takes place. **Figure 9a** depicts the classical response waveform.

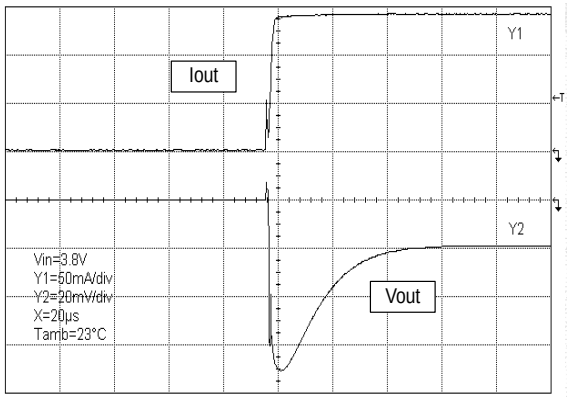


Figure 9b Reaction to a current slope of 2mA/µs

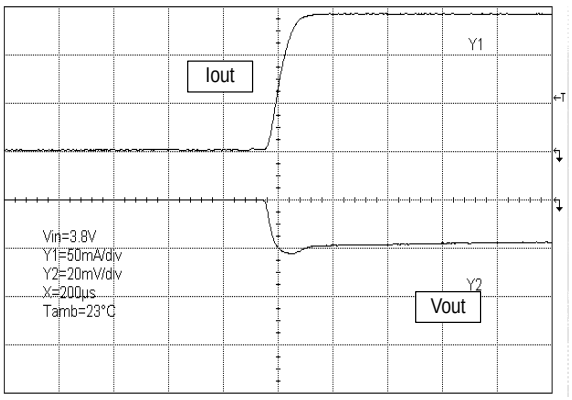


Figure 9c Reaction to a current slope of 100mA/µs

The slope of the output excitation is a key parameter when specifying the LDO transient response. The steeper the slope, the richest the harmonic content of the pulse. A rich harmonic content means frequencies well above the LDO bandwidth which cannot obviously combat the corresponding aggression: the negative undershoot takes place and is well pronounced. To cure this problem, you need to act on your final load in order to brake the establishment of the current. **Figure 9b** and **9c** respectively show the results for a low and a high current slopes.

In figure 9a shot, the current is pulsed from 3 mA to 150 mA. This situation is rather comfortable for the LDO. When the load is suddenly removed, it gives birth to a positive overshoot. Thanks to the 3 mA current, a discharge path takes place for the output capacitor and allows the internal circuit to immediately go back to its steady–state level with a series pass element slightly biased: the LDO is ready for the next shot and the negative undershoot stays within the specs (**Figure 9d**). If you now pulse the output from e.g. 150 mA down to zero, the discharge path no longer exists, except trough the internal feedback network: the discharge time is long. If unfortunately you bang the output while being in this discharge slope, the negative undershoot is

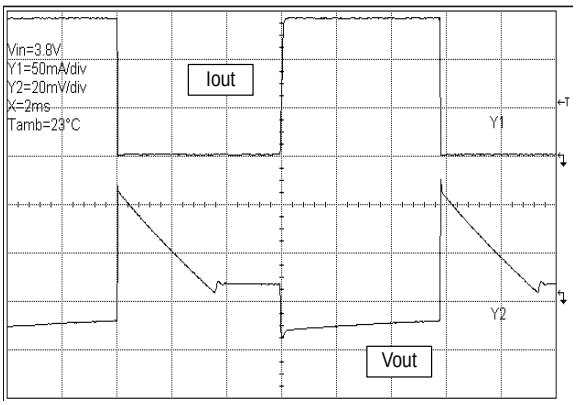


Figure 9d Transient response without any output rest current

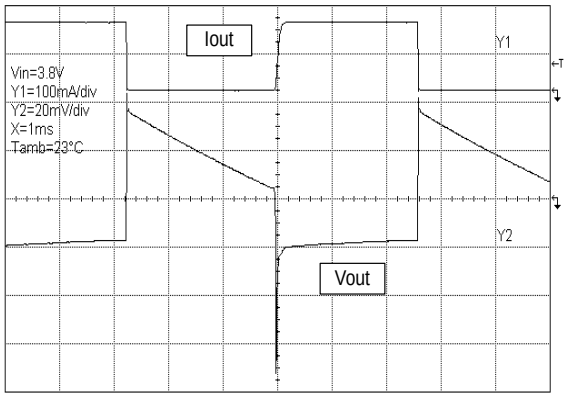


Figure 9e If you re–fire during the discharge, a negative pulse appears

much deeper, as **Figure 9e** portraits. In the discharge phase, the output level is above the nominal value and the circuit is asleep: the error amplifier's output is pushed to its upper level to block the PNP. This situation dramatically lengthen the response time to a perturbation and produces an exaggerated undershoot. Reducing the frequency of the output perturbation allows some time to recover as in figure 9d and avoids the negative undershoot.

Power–on phase

When the voltage starts to rise at the LDO input, the regulator crosses several stages. At the very beginning, when Vinput is low, the LDO is down and does not deliver any power to the load (stage 1). When the LDO starts to be active, it becomes a voltage follower and its output copies the input (stage 2). Finally, stage 3 is reached when Vout nominal is delivered. **Figure 9f** depicts this typical behavior for the MOTOROLA MC33263.

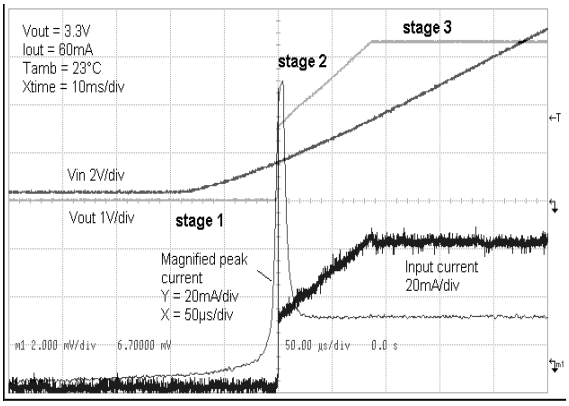


Figure 9f Typical LDO start–up curves

As one can see from the oscilloscope graph, a current glitch takes place just when the LDO enters stage 2. This glitch finds its seat in the voltage slope suddenly applied to the output capacitor which creates a current peak (C.dV/dt).

Waking–up the LDO

As we previously said, the bandgap needs an external bypass capacitor to reduce the output noise. When the LDO is in shut-down mode, the bandgap is cut and the bypass capacitor is discharged. If the logic control sends a wake–up signal, the bandgap circuit is enabled and the bypass capacitor starts to charge toward its nominal voltage. This naturally slows down the settling time of the voltage reference, as well as the output voltage. **Figure 10a** details the typical start–up phase of the low–noise MC33263.

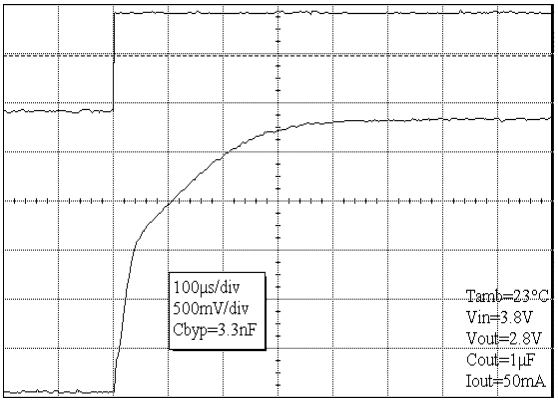


Figure 10. Start–up phase of an LDO by its OFF/ON pin

Waking up the LDO in a short time is particularly important in portable handset applications where the device timely checks for the presence of an incoming call. For instance, the Voltage Controlled Oscillator (VCO) in GSM phones is regularly switched on and off for the previous purpose. If you remove the bypass capacitor on the MC33263, the LDO reacts in less than 30 µs but its output noise reaches 65µVRMS 100 Hz–100 kHz.

Bipolar technology boasts low noise

The vast majority of LDOs are built around a bandgap reference and an error amplifier whose output stages integrates the series pass PNP. When you supply a noise sensitive circuit, e.g. a Radio Frequency (RF) VCO, the noise superimposed on the supply line is a key parameter to not degrade the overall noise floor. There are several types of noise, as pedagogically detailed in [4]: *Johnson noise* finds its origin in the thermal agitation of electrons in resistive portions of the circuit (transistor base, bias resistors etc.). Also called *white noise*, its power spectrum is flat up to a certain frequency cutoff. That is to say, each harmonic theoretically transports an equal level of energy over the considered spectrum. The *flicker noise* is dependent on the quality of the process and exhibits an 1/f envelope, whence his second name, *1/f noise*. This so–called *pink noise* transports the same level of energy integrated over each decade of frequency. *Shot noise* describes the fluctuations of a current flowing in a junction around its steady–state value. It also produces a flat power spectrum: it is a white noise.

By mixing the previous sources into a circuit, you can imagine they will combine to shape the overall spectrum response. In the low frequency range of the LDO noise, 1/f noise is prevalent until you reach a technology dependent frequency corner f_c where white noise takes over.

An LDO is made of two separate blocks whose individual noise performances condition the component final specs in this domain. If we split a regulator into a bandgap reference and an error amplifier/output stage, their DC noise characteristics are the main contributors to the LDO noise. However, since internal poles and zeroes are positioned for stability compensation purposes, the AC behavior of these stages also impacts the global performances.

Figure 11a describes a typical noise spectrum of a bandgap reference. As we previously saw, the noise decreases with an 1/f slope until the technology dependent corner f_c is reached. A second pole appears, f_{p1}, due to the bandgap bandwidth. The designer internally fixes it but offers the possibility to reduce it by the mean of an external bypass capacitor: if the bypass capacitor value is high, its rolls off the bandwidth and accordingly dwindles the noise. The most important part of the noise spectrum is the bandgap noise floor.

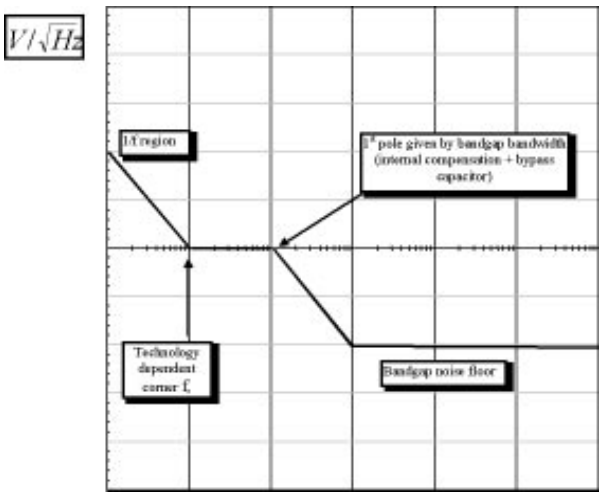


Figure 11. A typical bandgap noise spectrum

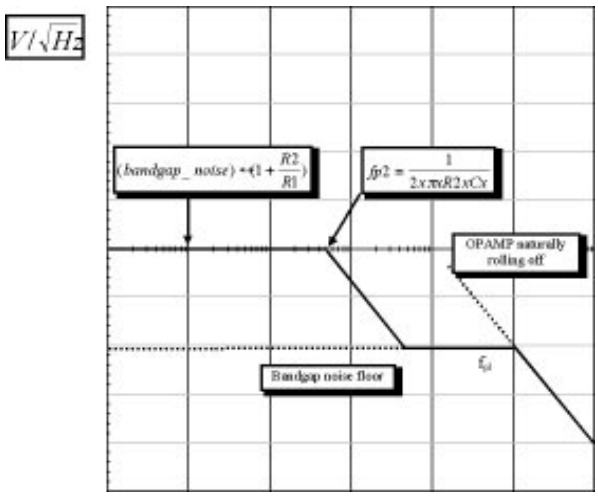


Figure 11c A typical output stage noise spectrum

Let's connect our reference voltage to the output stage according to **Figure 11b**. The error amplifier is connected in a non–inverter configuration with a gain of (1+R2/R1) which, of course, amplifies the bandgap noise. Since the LDO is a rather low frequency device, there is no need for gain in the upper portion of the spectrum. Capacitor Cx with R2 will thus introduce a pole at f_{p2} to tailor this gain. It then makes the output stage act as a simple follower when Cx shorts R2. The error amplifier naturally rolls–off at pole f_{p3}, as **Figure 11c** depicts. Once you gather the two spectrum plots upon the same graphic, it gives birth to **Figure 11d**. Looking at this noise curve gives some clues on the options you have to act on the total RMS noise:

1. Decrease the frequency of f_c. Impossible since the silicon material dictates its performance!
2. Diminish the bandgap noise floor. The noise level is kept low by good design rules, clever transistor architecture and selection, low base resistance and high enough collector current for critical transistors [3] (in the bandgap but also in the output stage).
3. Roll–off the bandgap bandwidth by internal frequency compensation or via the bypass capacitor.
4. Move f_{p2} toward low frequencies by increasing Cx.R2 time constant. Well, the flexibility is not obvious since high values for R2 will engender more thermal noise and bigger Cx eats silicon die size. It is usually difficult to decrease f_{p2} below several tens of kHz in common designs.
5. Using low bandwidth operational amplifiers is a solution when noise density above 500 kHz is critical. Otherwise, when the noise target stays within 100 kHz, this last contribution is less important.

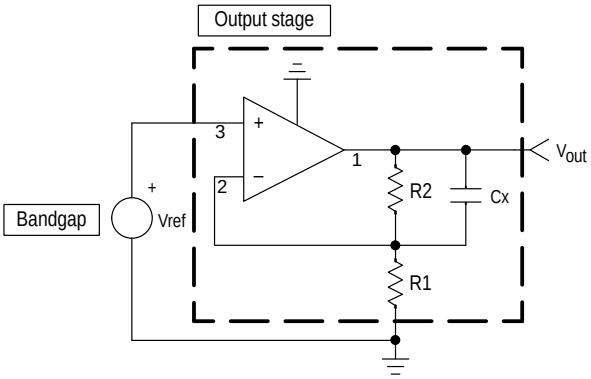


Figure 11b The complete LDO noise chain

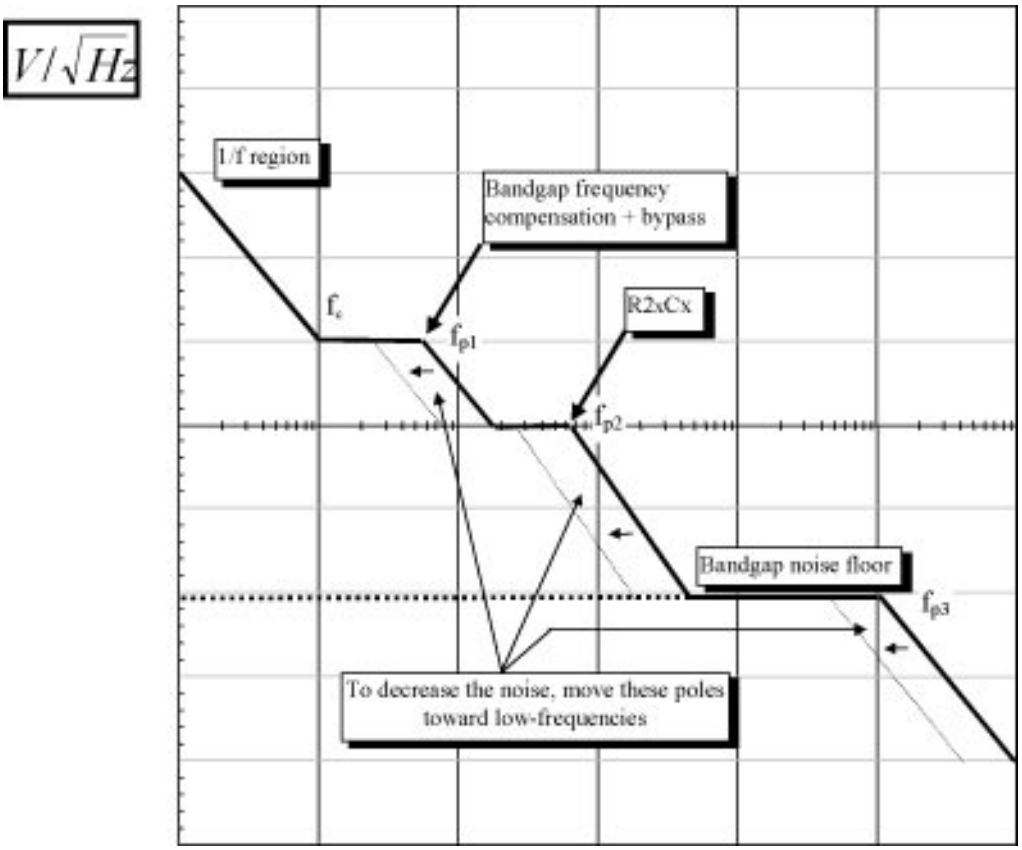


Figure 11d Total LDO noise behavior

Watch out for noise specs!

The definition of the white noise states that the power or the energy content it transports is equally distributed over the spectrum of interest: if you take a measure with a powermeter at any frequency you should theoretically always find the same value. If the noise is not white, or is actually a mix–up of white and 1/f components, its power content is no longer equally distributed over the considered spectrum. You are then obliged to define a bandwidth B in which you measure your noise power: it becomes a power noise density expressed in Watt/Hertz. Power can be evaluated by its **m**ean **s**quare **v**alue (*msv*) with the formula: $msv = \frac{1}{T}\int_0^T [f(t)]^2 dt$ also equal to $\sum_{n=-\infty}^{\infty} |C_n|^2$ if we relate *msv* to the energy transported by each harmonic (Cn being the Fourier coefficients). Since we want to deal with voltages, simply extract the square root of the *msv* and you obtain … RMS voltage: $\sqrt{W/Hz} \Rightarrow V_{RMS}/\sqrt{Hz}$. This explanation teaches us three things: a) since LDOs power density is not equally distributed over the spectrum of interest, expressions of this density without a frequency reference is a non–sense. The correct information should be for instance: $200nV/\sqrt{Hz}@1kHz$ b) any total RMS noise level given in lack of bandwidth and minimum operating conditions cheats you about the real noise level. This last sentence is particularly pregnant if the given bandwidth is short! An adequate statement could be: 100µVRMS <100Hz–1MHz> @Iout = 50mA c) spectral noise density over frequency plots are fundamental to assess the noise of an LDO. A designer cares of the noise density level over his operating spectrum, e.g. in or out his PLL bandwidth. A simple amplitude/frequency plot nor a total RMS level (integration smoothes ungraceful peaks or resonance!) cannot give him such insight. That is why MOTOROLA provides you with spectral density plots to clearly show how his LDOs perform in term of noise. As an example, **Figure 12** depicts the ultra–low noise level of the new MC33263, specifically designed for telecommunication applications where noise is at premium.

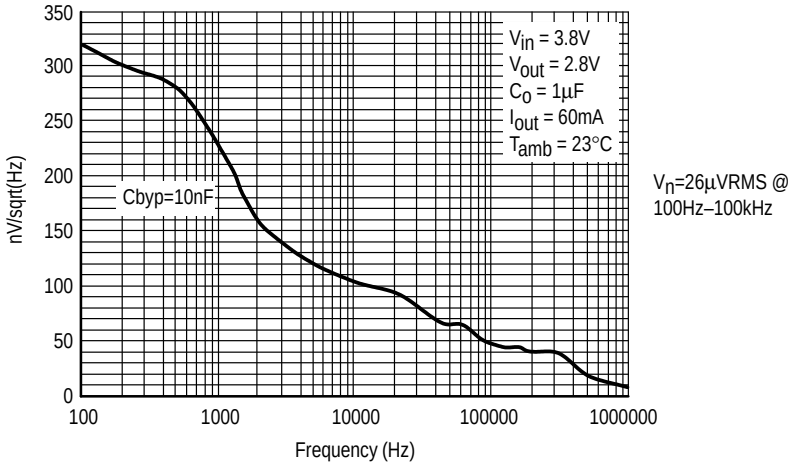


Figure 12. Noise density plots give insight about the noise performance of the device

Noise and RF specifications

It is today widely understood that the Voltage Controlled Oscillator (VCO) and its associated loop circuitry is one of the critical section in a radio. Its overall behavior but specifically its noise performance condition the radio most important specifications: spectral purity of the transmitter, selectivity of the receiver, noise and hum in analog transceivers, phase error in digital systems etc.

VCOs are extremely sensitive to external perturbations. This property has been even used to design low cost receivers (regenerative and super–regenerative receivers). The purpose of this article is not to present a comprehensive theory of noise in oscillators (which would probably require entire books!) but it is important to feel how the noise can plague your radio designs.

What is phase noise?

Both *phase* and *amplitude* characteristics of an oscillator can be affected by noise. With some simplifications, pure phase noise can be considered as phase or frequency modulation of a carrier, by a kind of random signal. **Figure 13a** depicts how the carrier will move around its nominal frequency because of noise modulation. You could take a frequency counter and save pictures of the display along the time to obtain this drawing.

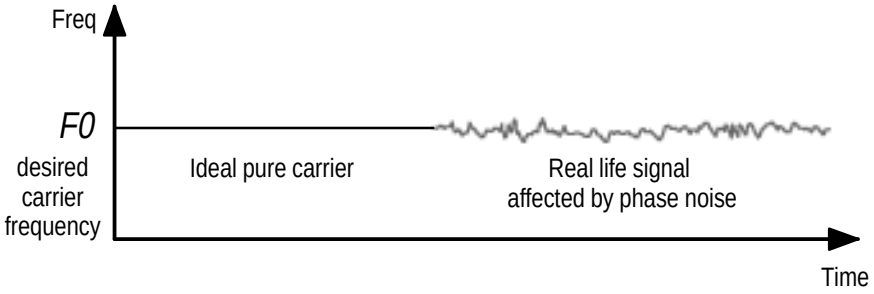


Figure 13. The time domain representation of phase noise

Figure 13b portraits the same phase noise but translated into the frequency domain, like when observed with a spectrum analyzer. Without phase noise, the spectrum screen would simply display a single ray at the nominal frequency. But the phase noise makes sidebands appear, as shown on the picture.

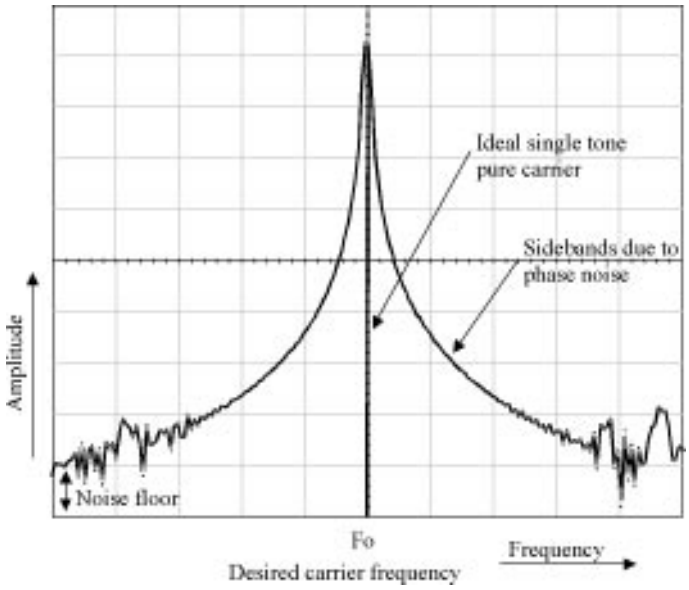


Figure 13b Frequency domain representation of phase noise

VCO and noise

A VCO is the seat of four well identified phase noise sources on which a lot of studies have been carried. The two first are:

Thermal noise:

Amplified within the oscillator loop and consequently modulating the carrier. The linear approach is usually used in this case, leading to some equations like the well–known Leeson's model [5].

Flicker noise:

It depends on active elements and even passive components, which usually require a non–linear approach, because of its "up–converted" nature. Nevertheless, some simple models, like the enhanced Leeson's model proposed by Parker or others, can still be used :

$$S_\phi(fm) = \left[\alpha_r \times F_0^4 + \alpha_E \times (F_0/(2 \times Q_L))^2\right]/fm^3 + \left[(2 \times G \times F \times K \times T/P_0) \times (F_0/(2 \times Q_L))^2\right]/fm^2$$
$$+ (2 \times \alpha_R \times Q_L \times F_0^3)/fm^2 + \alpha_E/fm + 2 \times G \times F \times K \times T/P_0$$

Where: G is the compressed power gain of the loop amplifier
F is the noise factor of the loop amplifier
K is the Boltzmann's constant
T is the temperature in Kelvins
Po is the carrier frequency in Hz
fm is the offset from the carrier Fo, in Hz
Q_L is the loaded Q of the resonator in the feedback loop
α_R is the flicker noise constant of the resonator
α_L is the flicker noise constant of the loop amplifier

This equation reveals so–called terms "$1/f$, $1/f^2$, and $1/f^3$" noise and also the tremendous importance of Q_L and output power Po.

The remaining two noise sources are probably more important, despite what can be read in books focused on state–of–the–art devices. Actually, the design of VCOs in large volume products (e.g. cellular or cordless phones) requires a lot of trade–off in order to account for cost targets etc. One of the most common tradeoff is accomplished on the tuning part where tuning slopes of 100 MHz/V are not uncommon. This large quantity allows a comfortable modulation dynamic even on low battery voltages where the cost of DC–DC converters would have hampered the final product price.

Varactor noise:

The varactor diode can be considered as an equivalent resistor R, (usually few tens of Kohms) generating thermal noise. Please note that the resistance usually biasing the diode can also have some influence if not properly optimized. The Single Side Band (SSB) noise N generated at an offset fm from the carrier, can be expressed in dBc (dBs bellow carrier) [6] :

$$N(fm) = 20\log_{10}\left[\frac{Ko\sqrt{4 \times K \times T_0 \times R}}{\sqrt{2} \times fm}\right]$$

Where Ko is the VCO gain in Hz / V
K is the Boltzmann's constant
To is the temperature in Kelvins

As an example, let's assume R=10 kΩ, fm=100 kHz, and Ko=20 MHz / V. We obtain $N_{(100\ KHz)} = -115$ dBc / Hz which is not negligible in GSM for instance. Partly for this reason, the tuning range shall be kept as small as possible.

Pushing noise:

As you can easily imagine, a noisy supply voltage will induce amplitude noise on the VCO output. However, it does not represent a big issue since the signal is further limited by downstream buffers and mixers. The real trouble is located in the conversion of this amplitude modulation into phase noise. This effect is called the *pushing*. If we call P the pushing gain of the VCO (Hz/V) and Sfm the supply voltage noise at fo (nV/√Hz) (measured at an offset fm (Hz) from the carrier), we can evaluate the frequency ripple generated according to the formula: $\Delta frms = P \times Sfm$ in Hertz. We can also relate it to a peak phase noise deviation by: $\theta fm = \frac{\sqrt{2} \cdot P \cdot Sfm}{fm}$ in radians, for 1Hz bandwidth. Finally, the phase noise calculated at an offset fm from the carrier will be found using: $N_{(fm)} = 20 \cdot \log_{10} \cdot \left(\frac{P \cdot Sfm}{\sqrt{2} \cdot fm}\right)$

You could try to reduce the supply noise by additional filtering using RC networks, but you would degrade the dropout of the overall device and the turn–on speed would obviously suffer from this integration. The only solution lies in using ultra low–noise LDOs.

Influence of the supply in Phase Locked Loops (PLL)

With some simplifications, we can attribute the noise present within the PLL bandwidth to the time reference (usually very clean) multiplied by the division ratio. This level cannot drop lower than the minimum noise floor imposed by the surrounding noisy circuits (e.g. switching charge pumps etc.). Outside the loop bandwidth, illustrated by a transition zone, the free running VCO noise (or short term VCO drift) is always predominant. This is pretty well observed on **Figure 14**'s spectrum shot obtained on a DECT synthesizer supplied by LDOs differing in noise specs.

The VCO we implemented in the measurement offered a pushing gain of 40 MHz/V associated with a tuning gain of 80 MHz/V. If we select an equivalent diode resistance of 10kΩ and a noise density of 50 nV/√Hz@100 kHz for the MC33263, we come up to −95 dBc/Hz and −103 dBc/Hz respectively for the DC supply noise contribution and varactor noise contribution at 100 kHz from the carrier. It thus gives us a total phase noise of −92 dBc/Hz@100 kHz or −55 dBc/Hz within our 5 kHz window of study. As you can see, it nicely agrees with the −53 dBc/Hz observed on figure 14's plot.

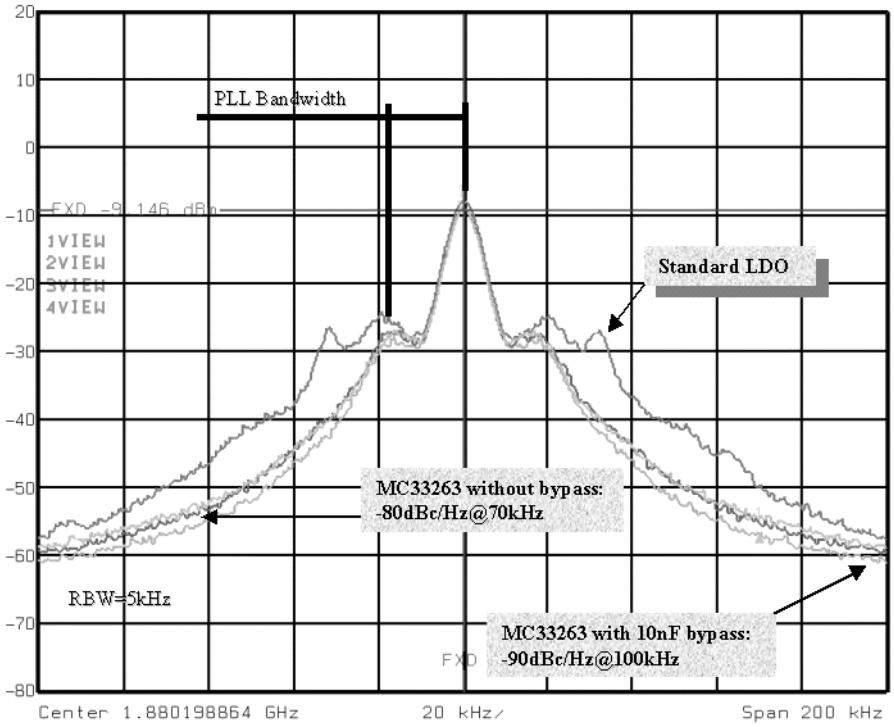


Figure 14. Comparison of a PLL behavior depending on the regulator's noise quality (RBW=5kHz)

A loaded Q and flicker noise calculation (using enhanced Leeson model) would have lead us to a much lower contribution, thus negligible.

For cellular or cordless systems, like in the above example, attention must be paid to the quality of VCO's supply and optimized LDOs like the MC33263 or MC33765 (5 output LDO) should be selected.

Conclusion

New low dropout regulators take benefit of the miniaturization trend associated with a decreasing operating voltage of portable products. Despite an ease of implementation, it is necessary to fully understand the way LDOs are built in order to design optimum performance systems.

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