AN1691

PRACTICAL SOLUTIONS FOR MEDIUM DATA RATE WIRELESS COMMUNICATIONS

Paul Sofianos
Motorola, Inc., WSSG RF/IF Applications Engineering

INTRODUCTION

This application note examines various practical solutions for an inexpensive, medium data rate (5.0 kbit/S to 100 kbit/S), wireless point–to–point link. The 902–928 MHz Industrial, Scientific and Medical (ISM) band was chosen as an ideal radio frequency (RF) medium for the wireless link for its low implementation cost as well as unlicensed (i.e., FCC Part 15) operation. FCC regulations permit continuous low power (approximately 0 dBm) or higher power (approximately 30 dBm) spread spectrum transmissions within the band. Only low power operation will be considered to reduce complexity and cost.

Successful wireless digital communications require a designer to consider a host of problems not usually encountered with a wired solution. This note will discuss these problems and examine some solutions for both the digital and RF portions of the link.

THE SYSTEM LINK – AN OVERVIEW

One of the first questions which must be resolved to implement a wireless, point–to–point link is whether to adopt a simplex (one–way) or duplex (two–way) architecture. If full duplex operation is a system requirement, the choice is obvious. However, if one–way transmission operation is all that is required (such as in a garage door opener), the choice may not be so obvious.

Simplex has the advantage of reduced complexity and cost, requiring only one transmitter and one receiver. Since there is no possibility of remote confirmation of received data, simplex usually relies on redundancy, typically re–transmitting the data several times in the hope that the remote receiver will be able to ascertain correct information. This strategy greatly reduces effective bandwidth and is extremely susceptible to other external transmissions which might overpower the desired transmitted signal.

Duplex communication affords the designer the capability to verify received data. As a result, data need only be transmitted once unless the remote indicates a reception problem. Furthermore, if the reception problem persists (possibly caused by external interference), the possibility exists to select a new, clearer frequency, communicate this to the remote, and adaptively change channels. This results in a very efficient use of bandwidth, with the effective bandwidth being determined by the bit error rate of the communication link.

Duplex operation need not be restricted to a talk then listen (half duplex) approach. It is possible for the host and remote to communicate with each other at the same time in both directions (simultaneously). This full duplex approach maximizes the effective bandwidth of the communications link, although there is a corresponding increase in complexity.

Once the question of simplex versus duplex communications has been resolved, it becomes necessary to define the nature of the RF link. Digital information must be modulated/demodulated on a RF carrier in order to establish the wireless portion of the link. Many modulation schemes exist, but the two most common are Amplitude Modulation (AM) and Frequency Modulation (FM).

Since digital information can take on one of two discrete values (zero or one), AM modulating a carrier with digital information is referred to as Amplitude Shift Keying (ASK). In ASK modulation, the carrier amplitude (i.e. transmitted power) becomes one of two pre–defined power levels. A special case of ASK modulation is On/Off Keying (OOK), whereby a logic zero is represented by no carrier power and a logic one is represented by full carrier power. In any event, ASK communications are a very poor quality RF communications link since they are extremely susceptible to external interference. ASK is generally used for very low data rate, short distance, redundant simplex communications. The availability of inexpensive, highly integrated FM RF devices has made ASK communications all but obsolete.

FM offers the designer improved noise immunity (and therefore lower bit errors) than AM. There are a number of ways to implement a FM wireless link, but the most cost effective and commonly used approach is Frequency Shift Keying (FSK). In FSK, digital zeros represent one unique frequency while digital ones represent another unique frequency. Obviously, it is possible to transmit more than just two discrete frequencies, thereby affording the possibility of an even higher effective bandwidth.

This application note will focus on implementing a full duplex, FM wireless communications link as the most practical solution for most systems in the medium data rate arena.

THE WIRELESS LINK – OVERVIEW

At this point, it is prudent to investigate the architecture of the wireless portion of the link. Thus far, we have determined that each half of the link will require a FM transmitter and FM receiver (full duplex) capable of operation in the 902–928MHz ISM band. Additional requirements are low RF power output and medium data rate compatible. To implement this portion of the link, the MC13146 Low Power Transmitter, the MC13145 Low Power Receiver and MC33411 Baseband IC were chosen.

The MC13146 will fulfill the role as the FM transmitter for the link. It is capable of direct conversion or up converted FM transmission and RF output power which meets FCC requirements. The device consumes very low DC power and is capable of operation from 2.7 to 6.5 V, ideal for both 3 and 5.0 V logic.

The MC13145 will implement the FM receiver portion of the link. The device has excellent sensitivity, selectivity and an integrated coilless demodulator as the detector for the recovered FM. It too consumes very low DC power and can operate from 2.7 to 6.5 V.

The MC33411 Baseband contains two complete synthesizers for the transmitter and receiver local oscillators (LOs), an additional phase–locked–loop (PLL) to generate a second LO for the receiver IC, and complete analog audio processing sections for received and transmitted signals. This device also consumes very low DC power, has a number of power saving features, and can operate from 2.7 to 5.5 V.

DIRECT CONVERSION OR UP CONVERSION?

Direct conversion FM transmission implies that the carrier frequency, or LO, is directly modulated with desired source. Direct conversion is extremely easy to implement and produces no unwanted mixing products. Unfortunately, in order to generate accurate frequencies above a few hundred megahertz, it is necessary to synthesize the desired frequency from some other stable source (such as a crystal oscillator) by the use of a PLL.

As we noted above, FSK transmissions take the form of two or more discrete transmitted frequencies. If we attempt to FM modulate the carrier directly, the PLL will eventually “see” the desired modulated frequency as a deviation from the carrier frequency (derived from a stable source), and attempt to correct the actual transmitted frequency back to the original carrier frequency. This phenomena is referred to as “tracking out” the modulation and can present a great deal of frustration to the designer.

Up conversion FM transmission techniques get around this problem by synthesizing a carrier frequency from a stable source (LO), and then mixing a FM modulated intermediate signal (or frequency, thus IF) to generate the desired frequency (referred to as the radio frequency or RF).

Generating the IF can also become a problem. If a PLL is used to generate the IF, the same “tracking out” problems will occur as with direct conversion. However, since the IF frequency can be significantly lower than the desired carrier, it is possible to generate a reasonably accurate IF without a PLL, thus eliminating the “tracking out” problem.

This approach adds complexity, cost and unwanted mixing products, but has the advantage of being capable of transmitting static (DC) levels. Also, in order to filter out unwanted mixer products, the IF should be as high as possible – thus making it more difficult to accurately create without the use of a PLL.

Although up conversion may appear attractive at first glance, it is necessary to study the receiver portion of the link. The MC13145 coilless demodulator uses, in effect, a PLL to recapture the modulated carrier. Therefore, this PLL will “track out” any DC from the transmitted signal, making the benefit of up conversion a moot point.

It now becomes obvious that our RF link will use direct conversion FM transmission and reception, and we will not be capable of transmitting or receiving static FSK signals.

DEFINING REQUIRED RF BANDWIDTH

Many designers are unfamiliar with required RF bandwidth as a function of digital bandwidth. To make matters even worse, there really is no “good” formula to calculate required RF bandwidth for a given digital transmission rate. Since this application note is supposed to give practical solutions to the problem at hand, I’ll try to give some general guidelines based upon my experience with the subject.

The first parameter which should be defined is peak deviation. Simply put, peak deviation is the delta frequency from the carrier which will be transmitted for either a logic zero or one. In general, a good starting point for peak deviation is:

peak deviation = (2 x Frequency Error) + Bit Rate

For example, if a system is based upon a crystal reference of 10 MHz specified as ±10 ppm and a 57.6 kbits/S data rate is desired at a RF frequency of 900 MHz, then:

Frequency Error = 900 MHz x 10e–6 = 9000 Hz

and,

peak deviation = (2 x 9000 Hz) + 57600 = 75600 Hz

Once peak deviation is defined, Carson’s rule can be used to approximate the required RF bandwidth as:

RF bandwidth = 2 x ((peak deviation + (Bit Rate / 2))

Again, as a practical matter, this only reflects the required bandwidth to transmit a sinusoidal waveform (not a true square wave), and represents a –3dB power point where the recovered voltage will be only 1/2 the expected value! The presence of a sine wave will mean energy is lost for a bit and this translates to higher bit errors. Realistically, a better approximation is

RF bandwidth = 2 x ((peak deviation +(3 x Bit Rate / 2))

For the example above, the RF bandwidth would be about 325 kHz. A 330 to 350 kHz RF bandwidth will allow for recapture of the transmitted signal to the third harmonic, at the loss of overall system sensitivity. Additionally, the higher the RF bandwidth, the higher the probability of unwanted interference from other transmission sources – a very real problem in all of the unlicensed bands.

As can be seen above, if only the fundamental frequency is to be recovered, the same 325 kHz bandwidth could be used for bit rates of about 175 kbits/S. Although this may seem attractive, the designer will most likely discover that the bit error rate is so high as to make reliable communications almost impossible, increasing re–transmission rates or redundancy and thereby reducing the effective data rate to that of a 57.6 kbits/S system or less.

As a general rule for medium data rate communications within the ISM band, peak deviations of 25 to 100 kHz and bandwidths of 150 to 380 kHz result in the best overall system performance.

DEFINING MINIMUM DATA RATES

So far, we have only been concerned with the maximum data rates which can be transmitted and received through the RF link. Equally important is the minimum data rate, or more appropriately the minimum fundamental frequency which will be transceived.

As we discovered above, direct conversion FM does not allow for static transmission of DC levels. The PLL loop filter will tend to “track out” very slow frequencies, or more precisely, those frequencies which are not significantly above the low–pass loop corner frequency. Lowering this corner frequency extends channel lock time and can add significant phase noise to the transmitter, again impacting bit error rate. This is perhaps the most frustrating dilemma of the system

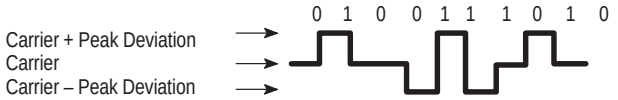
design, as most of the burden to solve the problem lies in the digital domain.

Several techniques have been developed to overcome this problem. They include, but are not limited to:

1. Manchester encode the data. The minimum fundamental frequency will be one half of the bit rate. Although very easy to implement from a transmit point of view, a receiver requires a preamble of bits in order to determine the center of the bit stream. This preamble must occur from time to time, as a missing bit or bit error can cause all other bits within the stream to be misinterpreted.
2. Use intelligent encoding schemes. Many of these abound, all at a cost of complexity. See AN1687 for an example.
3. Use a multi–phase encoding scheme such as Alternate–Mark–Inversion (AMI). See Figure 1. AMI is a three phase, synchronous encoding technique which uses bipolar pulses to represent logical ones and no signal to represent logical zeros. It has the advantage of being inexpensive to implement at the cost of noise immunity (hence higher bit errors), but is well suited for many applications.

The prototypes for this application note were designed around AMI coding and will be discussed in further detail.

Figure 1. AMI Encoding



MINIMIZE DC COMPONENTS

Before we proceed, a few words should be stated about DC components.

Suppose we wish to transmit a continuous waveform represented by Figure 2. As can be seen, both the maximum and minimum fundamental frequency components are defined, satisfying the requirements which have been discussed so far. This waveform, however, contains a time–varying DC component which can play extreme havoc on the RF receiver.

The coilless demodulator of the receiver senses the presence of a DC component as a shift in frequency from the carrier. Again, this PLL–like circuit will essentially assume that the received frequency is “off” and adjust itself to a point where no DC component is present. This is referred to as Automatic Fine Tuning (AFT) and necessitates that the decoded output from the receiver is AC coupled a processing section.

The DC component of the signal will cause an excursion from the ideal signal center, and this in turn impacts noise immunity. Therefore, it is essential that the DC component of the transmitted signal remain as close to zero as possible at all times. As can be seen, AMI coded signals have no overall DC component, again making AMI encoding a very attractive method for RF transmission.

Figure 2. DC Components

Figure 3. RF Transceiver Block Diagram

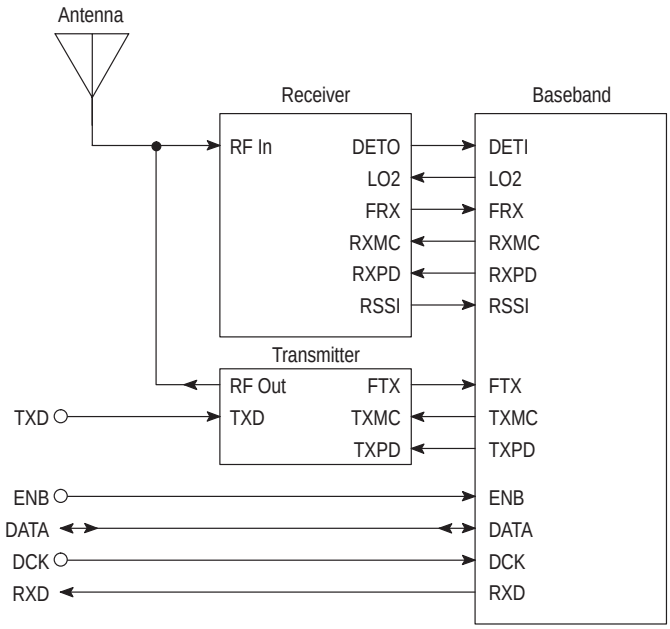
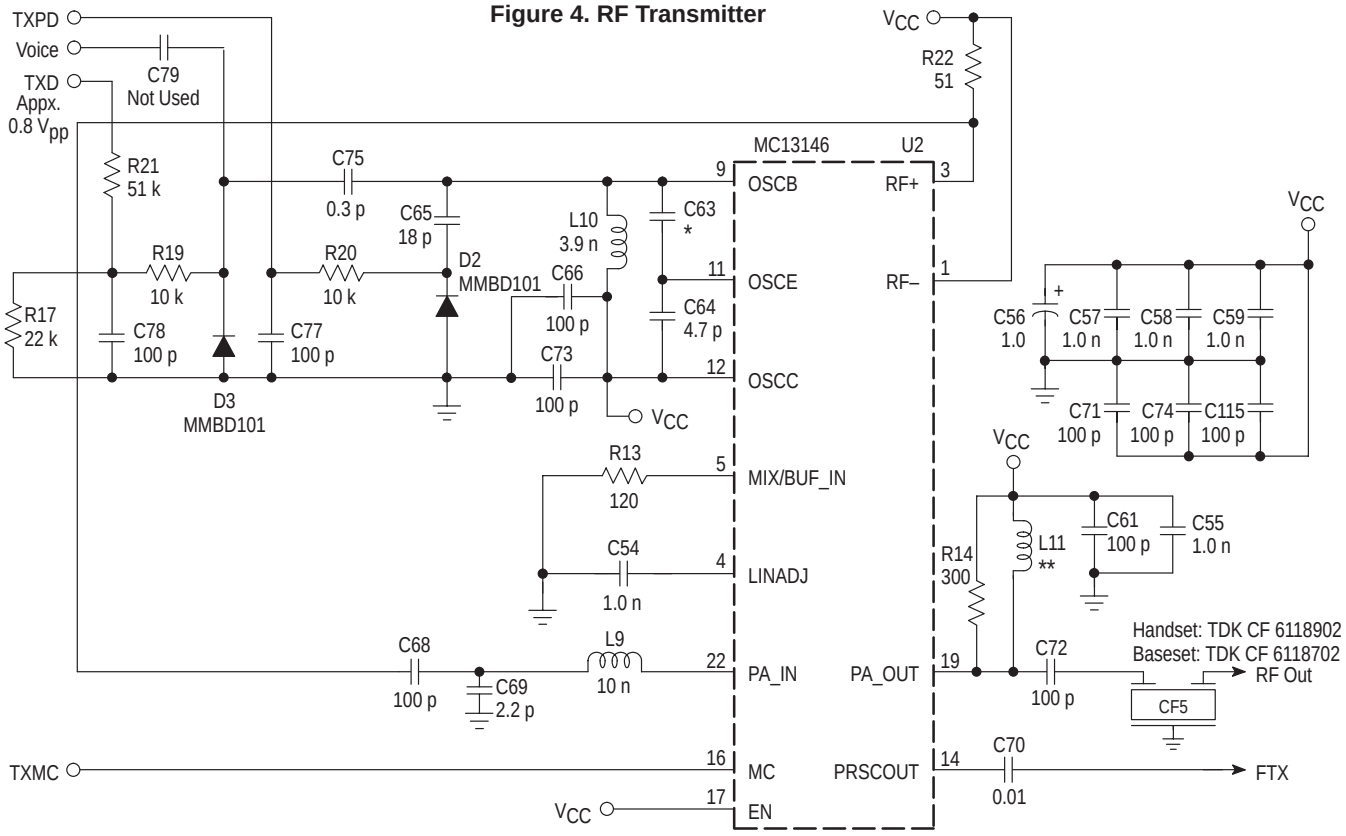


Figure 4. RF Transmitter



Default Units: Ohms, Microfarads and Microhenries
*C63: Handset 3.9 p **L11: See Text
Baseset 4.7 p

DESIGN THE RF TRANSCEIVER – GENERAL

Refer to Figure 3 for a block diagram of the RF transceiver.

For an example, we'll settle on a system with the requirements outlined below:

1. Frequency band 902 to 928 MHz, low power (<0 dBm) transmission, direct conversion FM.
2. Data rate 57.6 kbits/S, full duplex.
3. Data encoding/decoding – AMI.
4. Peak deviation – 80 kHz.
5. RF bandwidth – 330 kHz.
6. Number of channels – 5.
7. Channel spacing – 500 kHz.
8. Receiver first IF frequency – 73.7 MHz.
9. Receiver second IF frequency – 10.7 MHz.
10. Reference frequency – 11.2 MHz, ±10 ppm, 100 kHz internal.
11. Transmit/Receive channel delta – 21.9 MHz.
12. System power = +5.0 V.

Items 6 through 11 were chosen for the prototype after an analysis of possible image frequencies, cost and availability of external components. Arbitrarily, units are referred to as handset or master and baseset or slave. The handset transmits at 925.9 MHz for channel 2 and the baseset transmits at 904 MHz for channel 2. Channels are identified as 0–4, inclusive.

DESIGN THE RF TRANSCEIVER – TRANSMITTER

Please refer to Figure 4 for the transmitter schematic.

The MC13146 is configured as an oscillator/buffer with a parallel–resonant, Colpitts oscillator. C63/C64 provide feedback to the transistor and L10 is a tuning element. Diode D2, through R20, is used to tune the center frequency of the oscillator while D3, through R19, is used to direct conversion modulate the carrier. C65/C75 provide DC block to the diodes, set the diode tuning range, and are a factor in the overall resonance of the oscillator. C77 and C78 decouple the voltages from the PLL phase detector and transmit data source, respectively. R21 and R17 comprise a voltage divider for the transmit data source.

As tested, the VCO tuning range is approximately 8.0 MHz/V and the modulation tuning range (at TXD) about 200 kHz/V. The transmitter was designed to accept a nominal 800 mVpp signal at TXD for a nominal ±80 kHz peak deviation. Capacitor C63 was chosen to yield a tuning voltage of approximately 1.0 V for channel 2 operation. The actual values used are very close to the calculated, theoretical values, indicating a minimum of parasitic stray capacitance and inductance on the PCB.

The RF output of the oscillator/buffer is fed into the conjugately matched PA input by blocking capacitor C68 and matching components C69/L9. The PA output is biased by R14 and DC blocked by C72 prior to the RF filter. Output

power adjustment is by R13, and was a nominal –2.0 dBm after the filter.

L11/C72 were provided for conjugately matching the PA output to the load, and as a DC block. The actual values used are not for a 50 Ω conjugate match, as large variations in the load impedance (antenna) could cause the amplifier to go unstable. The values shown provided a good tradeoff between power transfer to the load and the PA remained stable for all tested conditions.

As this unit was a prototype, the VCO tuning range was considered adequate. Larger tuning ranges can make the design more robust from a mass production standpoint, but will result in poorer transmitted phase noise. It is also possible to construct L10 from wound wire, adjusting the inductance by “spreading” the coils, if desired.

DESIGN THE RF TRANSCEIVER – RECEIVER

Please refer to Figure 5 for the receiver schematic.

The receiver uses dual ceramic filters (CF4/CF3) for image rejection prior to mixing. Additionally, transmitter filter CF5 and receiver filter CF4 are used with controlled impedance traces on the PCB to form an improved duplexer to the antenna.

C6 is a DC block for the LNA input. L5 conjugately matches the LNA input, while C9/L4/R2 match and bias the LNA output. C10 is a DC block for the mixer input.

The mixer LO is again a parallel resonant, Colpitts type with diode D1, through R9, being used for tuning. C12 was chosen to yield a tuning voltage of about 1.5 V for channel 2 operation. As tested, the VCO had a tuning range of approximately 15 MHz/V, ideal for most applications. The calculated theoretical values vary a bit from the actual values shown, indicating some parasitic board inductance and capacitance in the tuning circuitry.

T1, C13, C14 and C40 match the output of the first mixer to 50 Ω, provide for selectivity and perform a balanced–to–unbalanced operation. The DC blocked signal from C14 is fed to the second mixer, as well as a LO signal derived from the MC33411 baseband.

C15, L7, L8 and C16 also match the output of the second mixer, provide for selectivity and perform a balanced–to–unbalanced operation for the IF amplifier. CF1 and CF2 are 10.7 MHz, 330 kHz bandwidth IF filters.

R3 is used to scale the ±80 kHz deviation signal to approximately 800mVpp. C25, in conjunction with R3, sets the high frequency corner and was chosen to be high enough not to bandwidth limit the recovered signal up to 300KHz. C43/R11 filter and current–to–voltage scale the RSSI output.

R4, R5, R6 and C32 set the frequency response of the coilless demodulator and were chosen for maximum bandwidth at 10.7 MHz IF and a low corner frequency for the AFT to accommodate slower bit rates (down to 9600 bits/S).

DESIGN THE RF TRANSCEIVER – BASEBAND

Please refer to Figure 6 for the baseband schematic.

The prototype wireless link did not utilize any of the audio transmit and receive paths available in the MC33411. It may be desirable, however, to design these paths into a production transceiver for the following reasons:

1. The compander circuitry may give improved bit error performance. If not, it can be internally bypassed by setting the corresponding register bits of the baseband IC.
2. If an EEPROM is available, the Rx and Tx gain adjust settings can be used to set desired signal amplitude instead of external adjustments. The EEPROM can also be used to adjust the internal capacitor for the local oscillator.
3. The Rx and Tx low–pass filters can be adjusted by setting the switched capacitor filter (SCF) counter to provide a very steep rolloff for unwanted frequencies. Take care to note the limitations of the anti–aliasing low–pass filter (AALPF) for the receive path for data rates above about 100 kbits/S.

All components shown for the audio transmit and receive paths are “default” values and were placed on the prototype PCB for other evaluation purposes. C79, C106 and C107 were not required for AMI digital data.

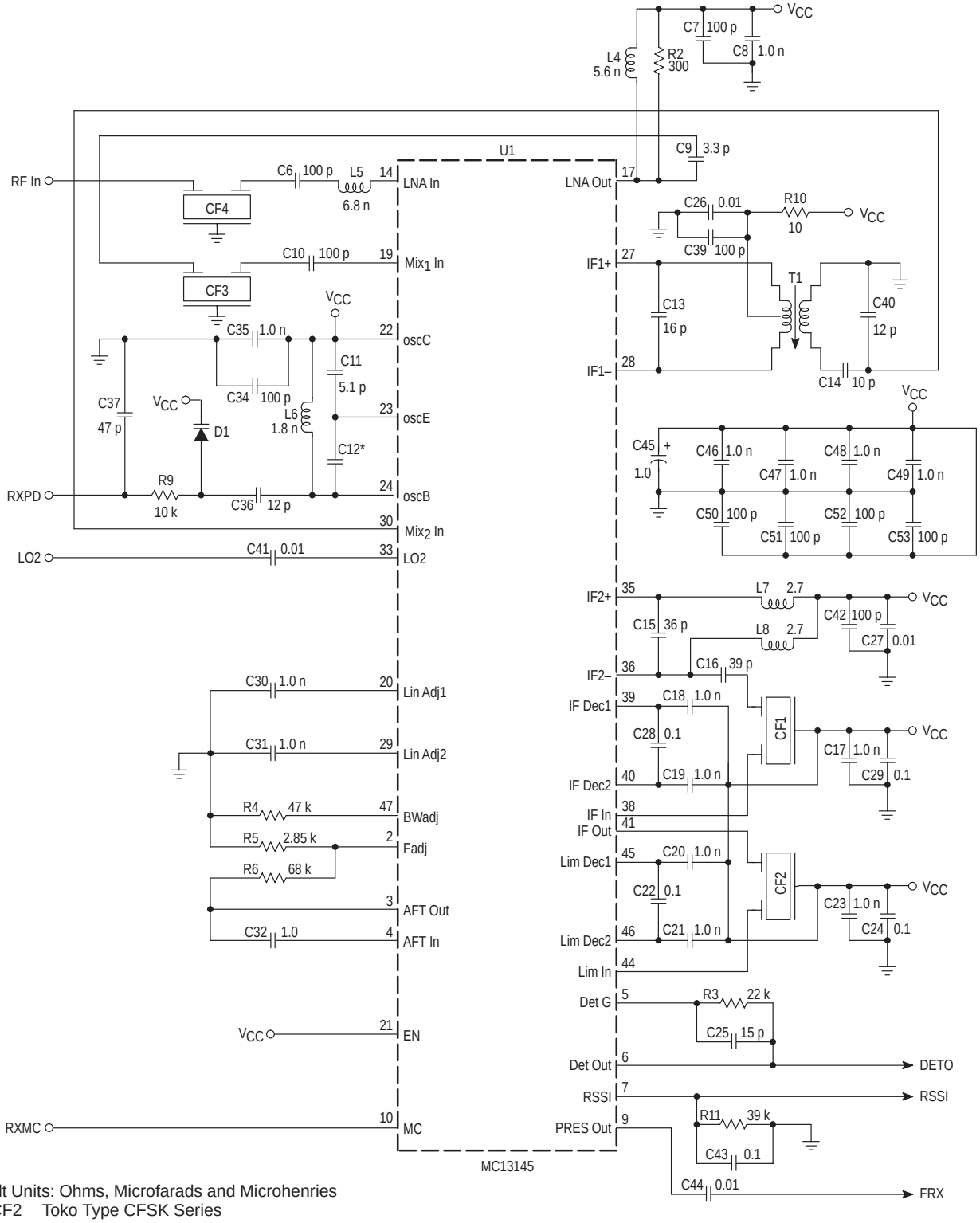
Y1, C83 and C84 are used to set and adjust the Pierce oscillator reference frequency. The internal reference frequency is set to 100KHz.

L12 and C92, along with an adjustable, internally selected capacitor, set the LO frequency at 63MHz. C91/C105/C104/R28/R29 comprise the PLL low–pass filter found in the MC33411 data sheet.

The Rx PLL and Tx PLL low–pass filters were calculated using the formulas provided in the MC33411 data sheet. For the Rx PLL, Qp was chosen to be 45 degrees, the K–factor was 6, and Wp was 6280 radians. For the Tx PLL, Qp was chosen to be 55 degrees, the K–factor was 12, and Wp was 314 radians. R2 was adjusted for the best experimental results.

The DATA, DCK, and ENB pins of the baseband comprise a three–wire, SPI compatible interface to the device. Programming of all baseband registers is accomplished through this port. The status of the battery (VCC) and RSSI voltage level can be read back through this bi–directional port. It is recommended that the SPI pins remain static during transfer of RF data to reduce digital interference to the transmitter and receiver. For the prototype, the baseband was programmed with a MC68HC705C8A MCU.

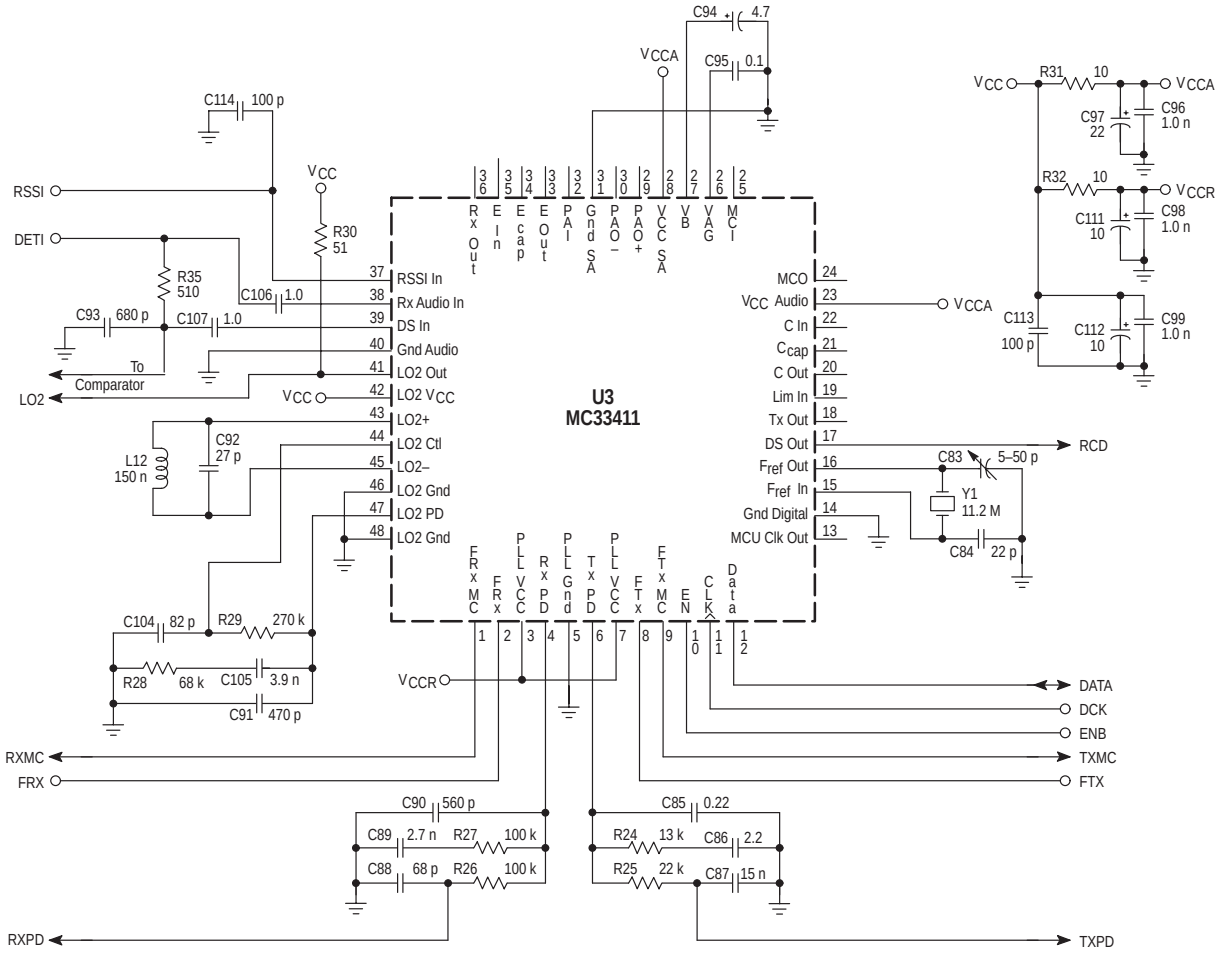
Figure 5. RF Receiver



Default Units: Ohms, Microfarads and Microhenries

CF1,CF2	Toko Type CFSK Series SK107MX–AE–XXX, 330 kHz BW
CF3,CF4	Handset: TDK CF6118702 Baseset: TDK CF6118902
*C12	Handset 5.1 p Baseset 4.7 p
D1	MMBV809LT1
T1	Toko A638AN–A099YWN

Figure 6. Baseband



Default Units: Ohms, Microfarads and Microhenries

RF TRANSCEIVER – GENERAL COMMENTS

As can be seen, designing the RF transceiver can be a relatively trivial task thanks to the highly integrated and tightly coupled nature of this chip set. For data rates other than the example, it is generally necessary to only recalculate:

1. The transmitted peak deviation required. This can be modified by R21/R17 voltage divider or C75 capacitor.
2. The received peak deviation. R3 can be adjusted for a nominal 800 mVpp swing and C25 recalculated for an appropriate high frequency corner frequency.
3. The receiver bandwidth required. R4, CF1 and CF2 can be changed.
4. Minimum frequency. Recalculate the AFT low–corner frequency by R6/C32.
5. PLL Tx low–pass filter.

For data rates in the range of about 5 to 100 kbits/S, this topology works well. Below 5 kbits/S, the transmit PLL loop filter begins to introduce a substantial amount of phase noise into the system. For data rates above 100 kbits/S, the receiver coilless demodulator becomes bandwidth limited, introducing high bit errors.

Obviously, the designer may wish to alter the channel spacing, first IF frequency, channel frequencies, etc. A thorough analysis of image frequencies and spurs should be performed to insure a solid RF link.

For the prototype communications link, the RF transceiver was implemented as a “dumb” medium. Channels were manually set, and the baseband processor was idle at all times except for initialization.

Lastly, the RF link was evaluated with “rubber duck” antennas to get a feel for open field (i.e. line–of–sight) communication distances. For the example above, the prototype units performed well to distances of about 1200 ft. when interference was a minimum. Indoor, home operation was reasonably reliable for distances up to about 300 ft. Clearly, these data rates can be realized for most consumer applications without the need to implement higher power (spread spectrum) transmissions.

THE DIGITAL INTERFACE – OVERVIEW

The basic hardware required to interface a digital communications port to the RF section can take on many architectures with a varying degree of complexity. In the least, the digital data stream to and from the digital–to–RF interface must be serial in nature, have a in–phase clock for transmitted data, and a recovered clock for received data. Also, some facility must be made to program the baseband

IC, and if desired, “intelligence” can be built into the system for purposes such as clear channel detection, bit error monitoring, etc. For the prototype unit, an unused RS–232 serial communications port from a PC was used for data stimulus and retrieval. The MC68HC705C8A MCU was used to initialize the baseband registers, monitor external switches and display basic information such as channel number and received signal strength.

THE DIGITAL INTERFACE – RS–232 TRANSMITTER

The serial, asynchronous data stream from the RS–232 port (i.e. TXD) cannot be directly AMI encoded without recovering the in–phase data clock. Although several methods exists to recover this clock, a simple rising/falling edge detector was used in conjunction with a 16X baud rate system clock oversample to re–time and regenerate the data and clock. Figure 7 is a block diagram of this circuit.

Once the re–timed data and in–phase clock are available, a toggle (T) flip–flop and three–state driver can be used to generate AMI encoded data. The T flip–flop is responsible for the alternating portion of the encoding, while the three–state driver converts logic zeros to a high–impedance state and simply buffers logic ones from the output of the T flop.

By using a simple pull–up/pull–down resistor arrangement on the output of the three–state buffer, three discrete levels will appear (for our purposes, about 0 V, 0.4 V, and 0.8 V). Additionally, a filter capacitor shunted to ground in parallel with the divider can provide a low–pass filter corner to attenuate high frequency, odd harmonics from the fundamental data stream.

A word of caution is in order at this point. Thus far we have assumed that the direct conversion modulation properties of the transmitter are linear. Our prototype was distinctly non–linear in this region, this being caused by reverse biasing the schottky diode referenced to ground. A quick look at schottky reverse bias versus capacitance characteristics indicates a very non–linear region of operation. This, however can be easily overcome by either reverse biasing the schottky at larger voltages or modifying the actual transmission voltages. For our purposes, we modified the transmit signal to assume three levels of 0 V, 0.3 V, and 0.8 V. Failure to take this into account produces a DC component in the recovered FM signal from the receiver.

THE DIGITAL INTERFACE – RS–232 RECEIVER

The recovered FM signal from the detector output of the RF receiver will have an undefined DC voltage with a well defined AMI encoded signal riding on it. It is necessary, therefore, to recover the digital (two–state) signal from the detector an eliminate the DC component (AC coupled).

As the AMI signal can assume three distinct levels, a window comparator is used to identify logic zeros as voltages less than an arbitrary high level voltage, VH and also greater than an arbitrary low level voltage, VL. The center or bias voltage, VB, represents a perfect logic zero (i.e., carrier) level. The detected FM signal is AC coupled to this bias voltage. The bias voltage should be very stable for both power supply and temperature variations. If desired, it can be derived from the VB pin of the baseband IC.

Although the choice for the VB voltage is not critical, VH and VL are. In theory, for best noise immunity, the bit energy for a logic zero should equal that for a logic one. For a perfect recovered square wave of 0.8 V_{pp}, this would suggest VH–VL = 0.267 V (one–third of the signal swing). However, for a perfect recovered sine wave of 0.8Vpp, this would mean VH–VL = 0.4 V (one–half of the signal swing). In practice, something between these two voltages will usually be ideal since the recovered signal will contain harmonics other than the fundamental.

The comparator output will contain “glitches” for received alternating ones. This is due to the fact that the recovered FM signal transitions are not instantaneous, nor is the comparator response. Therefore, transitions from one alternating state to the other must pass through the low state (in between VL and VH). These “glitches” can be used as part of a clock recovery circuit or “de–glitched” and ignored.

The first option affords the opportunity to re–synchronize to the incoming data more often (long strings of ones) at the expense of a loss of predictability. This is due to the fact that the glitch width is, among other factors, a function of the harmonics recovered from the received FM signal. The second option is more predictable but the recovered clock can only be re–synchronized when the data stream changes. Data streams such as RS–232 will always contain at least one positive and one negative edge for each transmitted data byte, and this is usually sufficient to recover a good clock. However, during the idle state, no data transitions will be available for clock re–synchronization. If this presents a problem, the first option above is probably the best approach. Lastly, the data can be further encoded by techniques such as High Density Bipolar 3 (HDB3) to ensure a constant stream of data bit transitions, if desired.

Once the embedded clock has been recovered, it can be used to extract the data from the comparator output. If the system permits, a digital oversample filter should be used to reduce bit errors caused from external interference. Figure 8 is a block diagram of the digital receiver.

Figure 7. RS–232 Transmitter

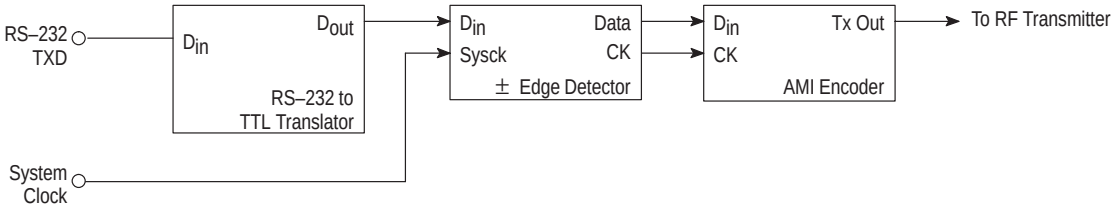
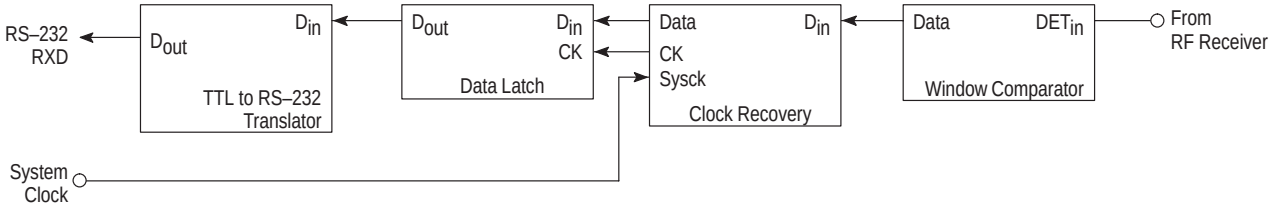


Figure 8. RS–232 Receiver



OBSERVATIONS

The prototype units were tested in two manners: First, by simply typing ASCII messages from one PC to another (simplex) and secondly, by transferring large binary test files using standard protocols such as Z–modem (duplex).

The first method provided a means to study the wireless link during long duration's of inactivity. The units performed very well until common external interference was introduced. The interference source was provided by 900 MHz cordless telephone sets. Even when these sets are not in use, as long as the handset is removed from the baseset, the handset periodically transmits RF signals to the base unit. If the proximity to the prototypes was close enough, the receiver could interpret this unwanted RF as a valid ASCII character. Simply scanning for a clear channel may not sense this interference during the test interval.

Since the prototype functioned as a "dumb" unit, no encryption or error checking of the desired data was available. Also, since this mode of operation emulates very low effective data rates, the digital overhead could have been easily used to either encrypt or verify the data. A simple program was written to test this concept for effective data rates of 1200 baud, and no data errors were encountered over a one hour test period.

Binary file transfer performed extremely well, as all standard protocols have some form of both error checking and re–transmission integrated into them. For very large file transfers, it would have been desirable to examine the error rate and automatically change channels if the link became corrupted. Still, it was not uncommon to transfer files indoors as large as one megabyte with zero or one re–transmission or retry request, yielding an effective data rate very close to the 57.6 kbits/S wireless link's capabilities.

SUMMARY

The availability of low cost FM transceiver ICs targeted for use in unlicensed FCC bands makes the implementation of practical, medium rate data radios for the consumer market a reality. Furthermore, by integrating inexpensive MCUs or high level software with these ICs, robust data communications can be achieved.

Most importantly, a system designer must consider real world anomalies associated with RF transmission and reception in the design, and thoroughly test the product under normal operating conditions to identify and eliminate interference not commonly found in wired communications prior to product acceptance.

REFERENCES

1. MC13145 Data Sheet, Motorola, Inc., Tempe, Az., 1998
2. MC13146 Data Sheet, Motorola, Inc., Tempe, Az., 1998
3. MC33411 Data Sheet, Motorola, Inc., Tempe, Az., 1998
4. AN1687, "A Full–Featured Wireless Interface for RS–232 Communications", Motorola, Inc., Tempe, Az., 1998

How to reach us:

USA / EUROPE / Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

JAPAN: Motorola Japan Ltd.; SPD, Strategic Planning Office, 141,
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan. 81–3–5487–8488

Customer Focus Center: 1–800–521–6274

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 1–602–244–6609
Motorola Fax Back System – US & Canada ONLY 1–800–774–1848
– http://sps.motorola.com/mfax/

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre,
2, Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.
852–26668334

HOME PAGE: http://motorola.com/sps/