AN1726

Using Motorola's Fast Static RAM CAMs on a Media Independent Interface

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Not too long ago we were happy to have a 10 Mbps LAN connection on our desktop computer. However, given the growing popularity of the Internet and other services, we find ourselves needing more bandwidth. 100 Mbps Ethernet promises to deliver the bandwidth we need without the need to rewire or rewrite our existing protocol stacks.

The transition from 10Base to 100Base Ethernet does present some implementation differences. Given the relatively low data rate of 10Base Ethernet, address filtering in bridge applications was often performed by the host CPU in software. The higher data rate of 100Base Ethernet doesn't allow the host CPU in the bridge enough time to accept or reject frames. There is a need to implement a hardware method to accept or reject frames. This need can be filled by the addition of a Content Addressable Memory to the Ethernet Media Access Controller.

A bridge would simply present to the CAM a 48–bit MAC address obtained from an incoming frame. The CAMs job is to search its contents and indicate to the MAC if the incoming address was present within the CAM.

Although CAMs have been available for years, they were often too expensive to justify their use. The MCM69C232 CAM addresses this problem with a different approach to CAM technology. By combining logic with fast and dense SRAM memory cores, Motorola is able to produce cost–effective, fast, and deep CAMs. The MCM69C232 is a 4K x 64 CAM and the MCM69C432 is a 16K x 64 CAM.

The purpose of this application note is to illustrate the connection of a CAM in a system. The CAM would exist between the Physical Interface Device (the PHY) and the MAC. The AMD79C971 MAC was chosen to illustrate. The MAC has an industry standard interface to the PHY known as a Media Independent Interface. What is needed is a single logic device that can interface the CAM to the MII/PHY connection and signal the MAC to accept or reject an incoming frame. This logic is easily implemented in a FPGA. We will discuss the operation of this FPGA in this application note.

MEDIA INDEPENDENT INTERFACE DESCRIPTION

The Media Independent Interface is a standard to facilitate the transfer of data between the MAC and the physical layer interface. The MII interface is a four bit (nibble) wide data path interface that runs at 25 MHz for a 100 Mbps networks and at 2.5 MHz for 10 Mbps networks.

The MII receive clock is generated by the PHY and is sent to the MAC on the RX_CLK pin. The data from the PHY on RXD[3:0] is presented synchronous to the rising edge of RX_CLK. The receive process is started when RX_DV is asserted and remains asserted for the entire receive frame length.

RELEVANT SIGNALS

Pin Name	Pin Function	Type	No. of Pins	Comments
RX_CLK	Receive Clock	Input	1	Recovered receive clock from PHY.
RXD [3:0]	Receive Data	Input	4	Received nibbles.
RX_DV	Receive Data Valid	Input	1	RXD [3:0] has valid data.

CAM DESCRIPTION

In its basic operating mode, the MCM69C232 reads a data input word and compares it to all the entries in its CAM table. Whether a match is found or not, the MC pin is asserted after the comparisons have been made. If a match is found, the MS pin is asserted, and the data associated with the matching entry is output on the MQ bus. If no match is found, the MQ bus remains in a high impedance state to facilitate depth expansion via the cascading of multiple CAMs.

RELEVANT SIGNALS

Pin Name	Pin Function	Type	No. of Pins	Comments
LH/SM	Latch High/Start Match	Input	1	Initiates match sequence on match data present on MQ31 – MQ0.
LL	Latch Low	Input	1	Latches low order bits if match width is greater than 32 bits.
MC	Match Complete	Output	1	Open drain, Pullups required.
MS	Match Successful	Output	1	Open drain, Pullups required.
MQ31 – MQ0	32–bit Common I/O CAM Data	Input/ Output	32	Used for input of match compare data values.

The CAM is prepared for match operations by writing to data and instruction registers via the control port. Since we are only interested in matching 48 bits, it will be necessary to set the global mask to ignore 16 bits of the 64–bit match field. If the MAC has an available EPROM space, the CAMs' control port may be accessed in this space.

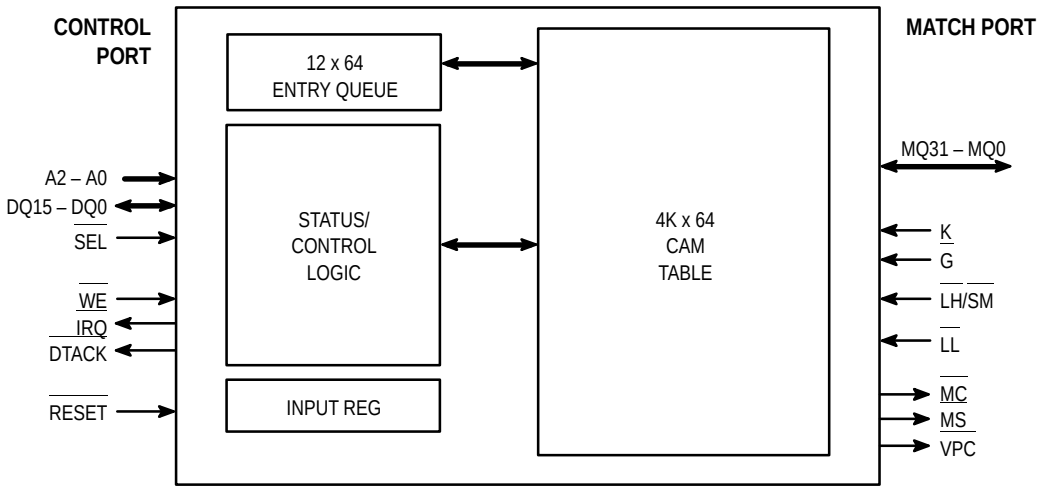
THE EXTERNAL ADDRESS DETECTION INTERFACE

The EADI is provided on the MAC to allow external address filtering. The EADI interface can be used in conjunction with external logic (the purpose of this application note) to capture the packets' destination address from the serial bit stream, to compare the captured address, and determine whether the MAC should accept the packet. The MAC supports external CAMs via its SFBD and EAR pins.

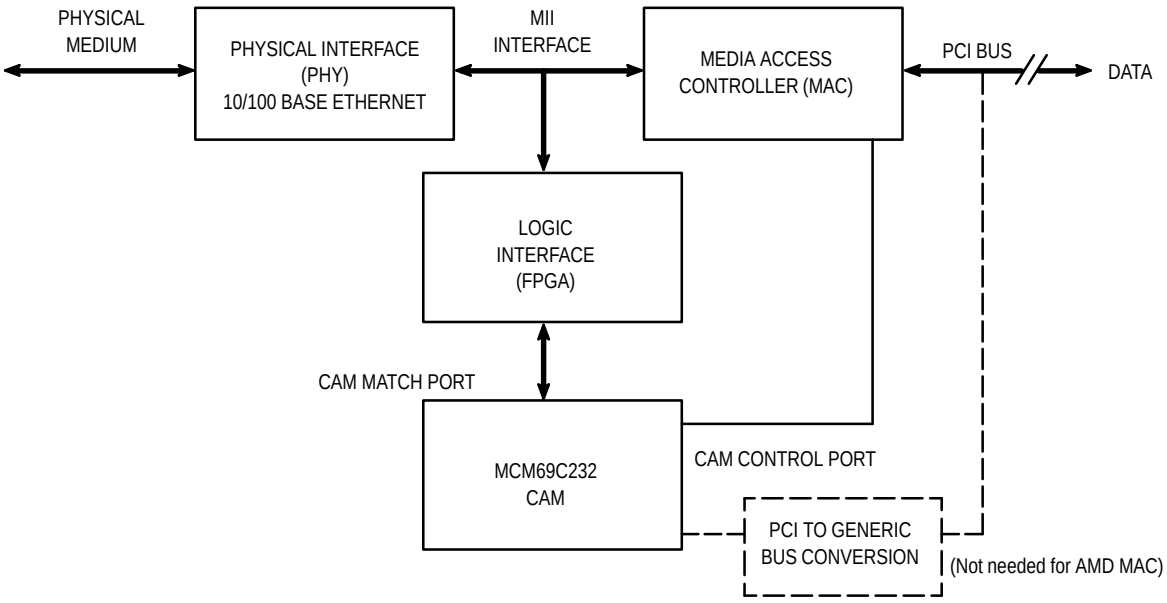
RELEVANT SIGNALS

Pin Name	Pin Function	Type	No. of Pins	Comments
SFBD	Start Frame Byte Delimiter	Output from MAC	1	Used by FPGA to indicate start of frame.
EAR	External Address Reject	Input to MAC	1	Used to reject the current incoming frame.

MCM69C232 CAM BLOCK DIAGRAM

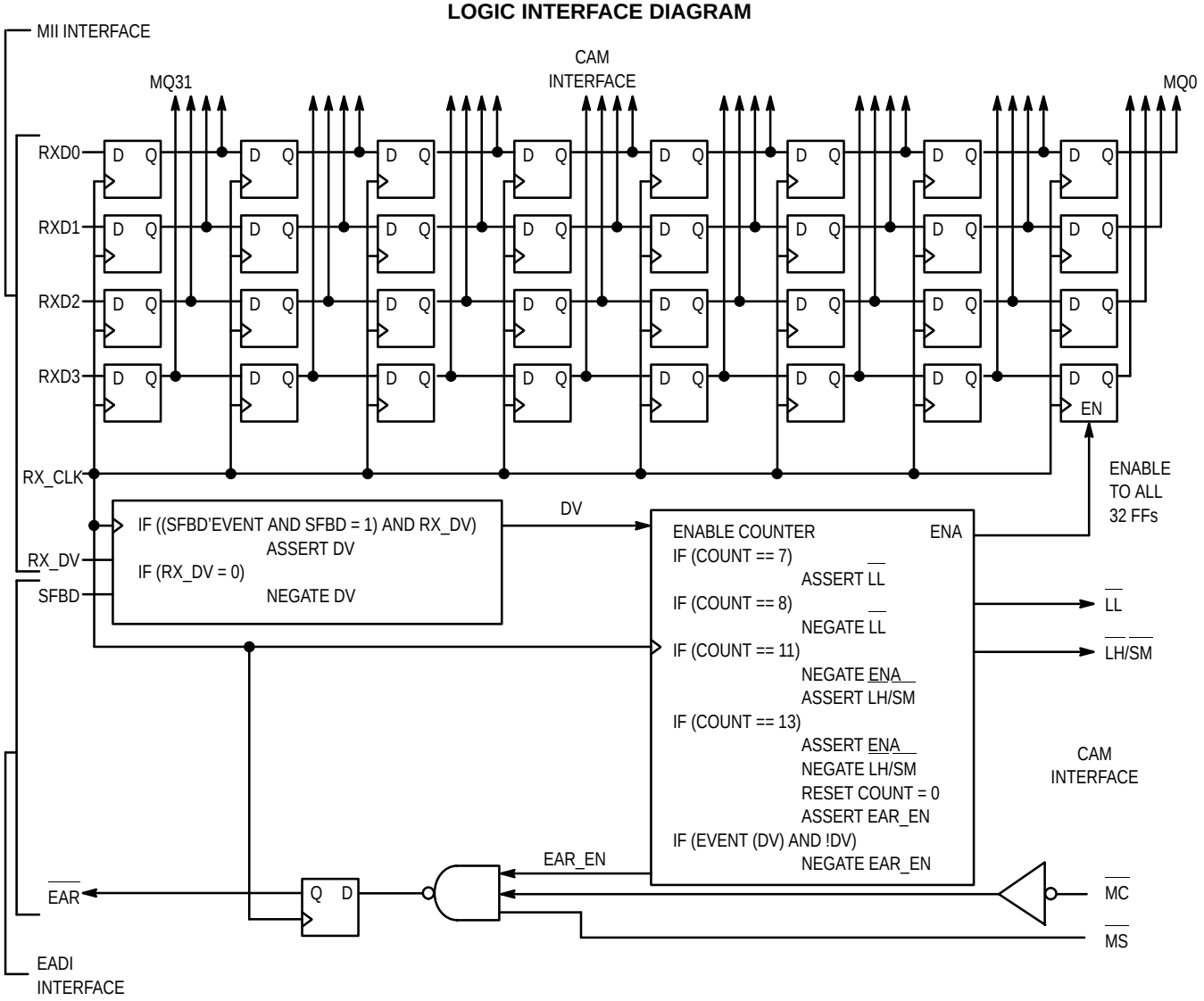


SYSTEM BLOCK DIAGRAM



NOTE: The FPGA uses several signals of both the CAM, MAC, and PHY.

LOGIC INTERFACE DIAGRAM



OPERATION OF THE LOGIC INTERFACE

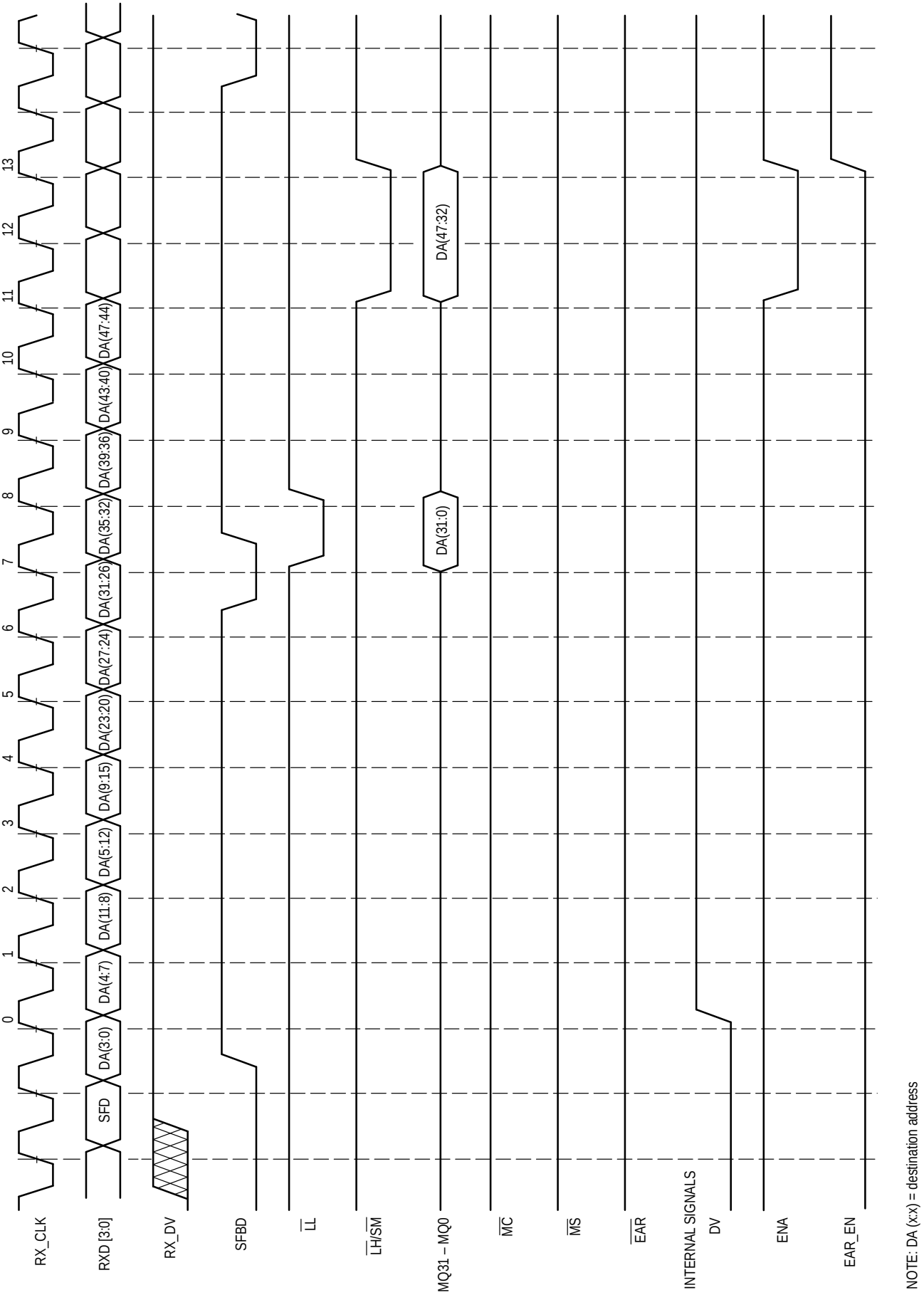
Receive data from the PHY is continuously clocked into the Logic I/F via RXD[3:0] and the RX_CLK signals. RX_DV is used to indicate that valid receive data is being presented on the RXD[3:0] signals. RX_DV remains asserted until after the last nibble of the CRC is driven on RXD[3:0]. RX_DV, when negated, resets the Logic I/F to its initial state.

An initial rising edge of the SFBD signal indicates that a start of valid data is present on the RXD[3:0] pins. The destination address, 48 bits wide, is then shifted into the Logic I/F, four bits per clock, and then presented to the CAM 32 bits at a time via the LL and LH/SM signals. The LH/SM signal then starts the match process of the CAM. The CAM will then respond with MC and if the destination address was not in the CAM, the $\overline{MS}$ will not assert. The Logic I/F then signals rejection of the frame to the EADI via its EAR signal.

RELEVANT SIGNALS

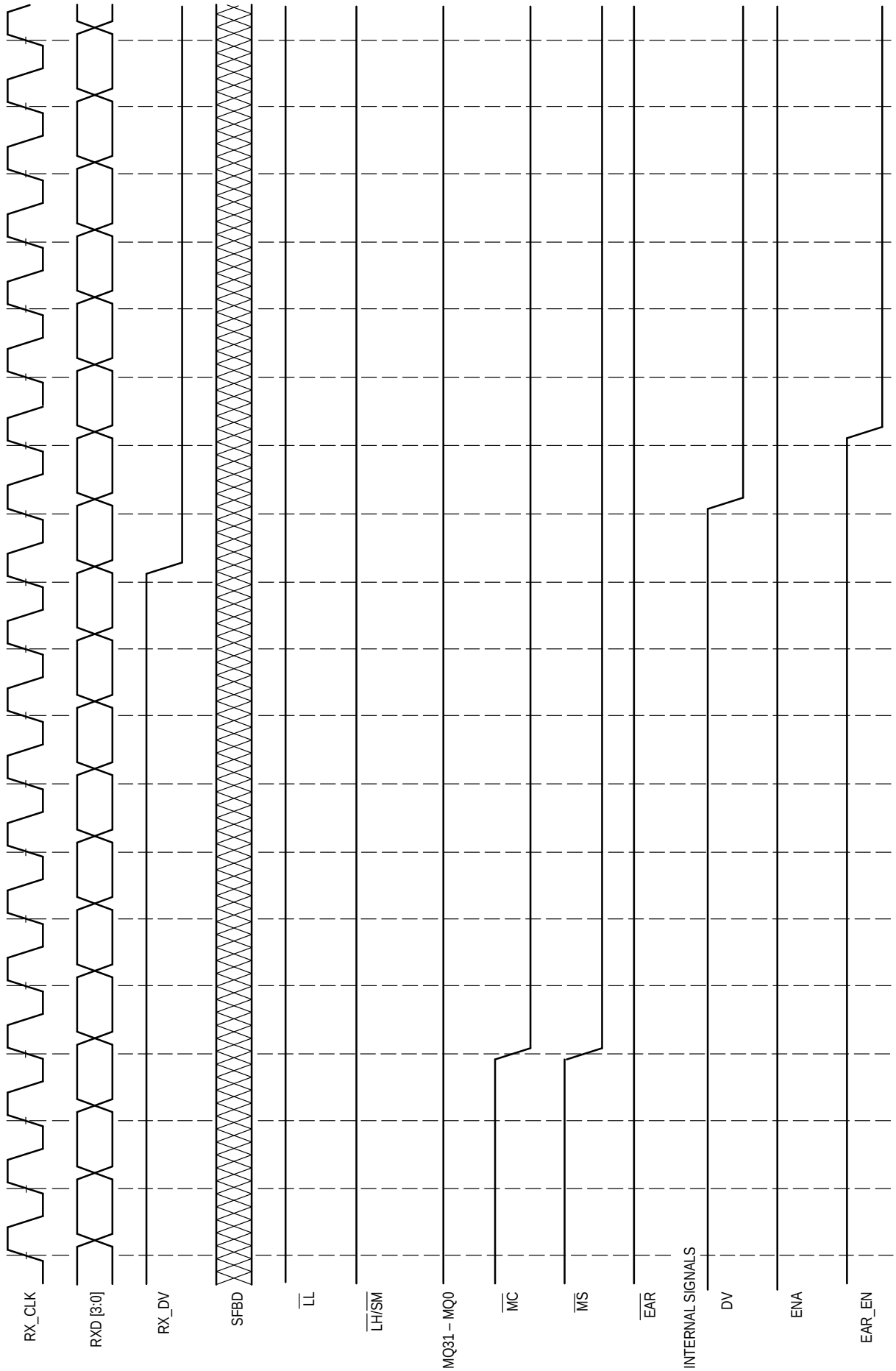
EAR_EN	$\overline{MC}$	$\overline{MS}$	$\overline{EAR}$	Comments
0	X	X	1	Address not yet latched.
1	1	X	1	Address compare in process.
1	0	0	1	Match successful. No Reject.
1	0	1	0	Match fail. Reject.

SIMULATION: ADDRESS CAPTURE

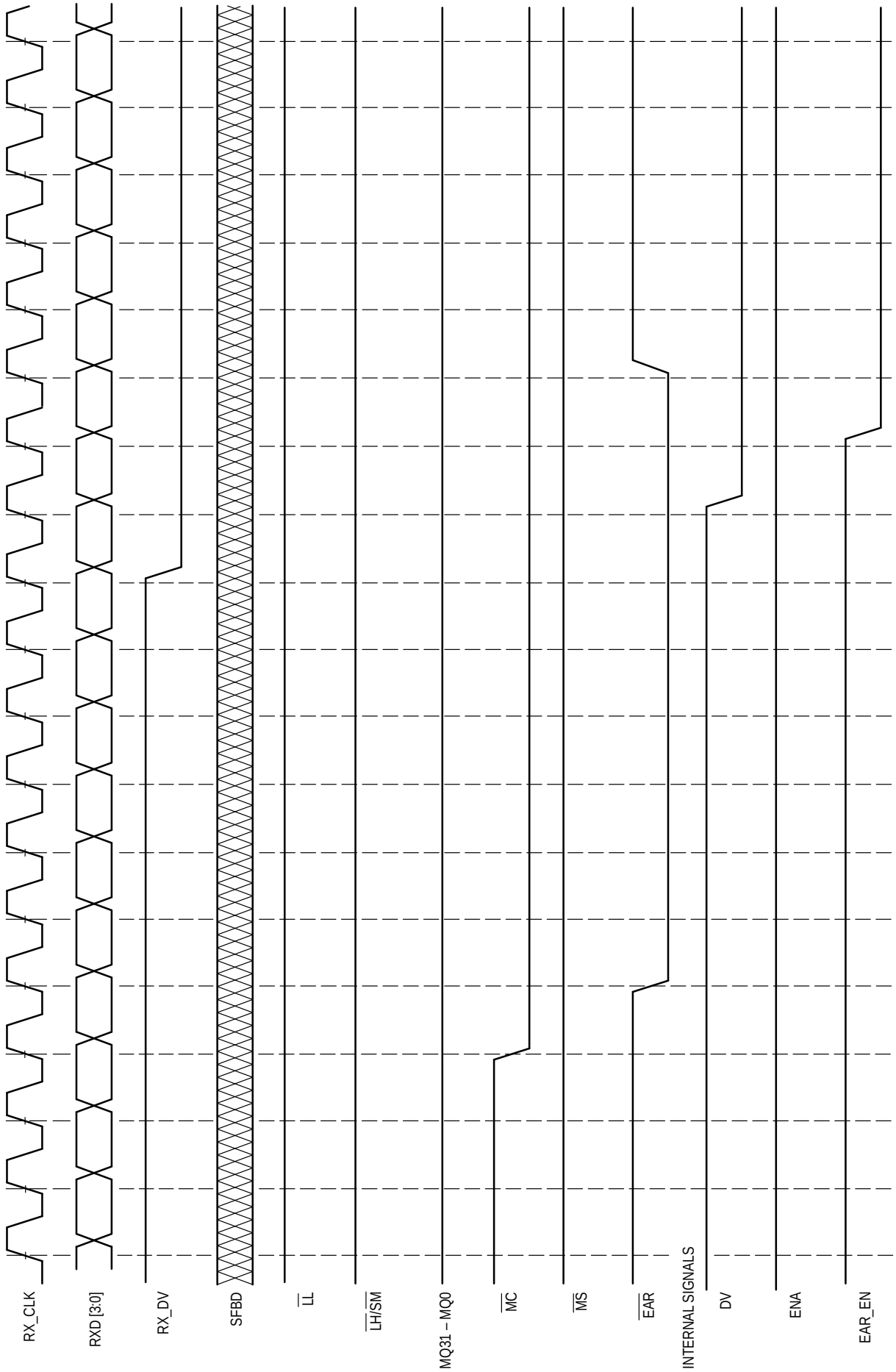


NOTE: DA (x:x) = destination address

SIMULATION: MATCH SUCCESS



SIMULATION: MATCH FAIL



SUMMARY

Motorola's number one global leadership position as a supplier of state of the art FSRAM devices has allowed for the advent of the cost effective CAM. With the addition of a small amount of logic it is easy to interface Motorola's MCM69C232 CAM to a MII / PHY Ethernet interface.

The addition of a CAM to a bridge will greatly increase the routing performance of a bridge at a slight increase to the cost of the bridge.

Changes to the logic can be made to facilitate any manufacturers' MII and EADI interfaces with ease. The logic can be easily implemented in a FPGA such as Motorola's MPA1016, the smallest, lowest cost member of Motorola's fine grain FPGA family.

REFERENCES

1. MCM69C232 4K x 64 CAM, Motorola Inc., 1997.
2. Am79C971 10/100 Mbps Ethernet Controller, AMD Inc, 1996.

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