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Application Note

Designing PCI 2.1-Compliant MPC106 Systems

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RISC Applications

Some PCI target devices are not compliant with specifications found in the PCI Local Bus Specification (Revision 2.1). This application note describes how to best design PCI-based systems using the MPC106. It is assumed that the user is familiar with the MPC106, the PCI Local Bus Specification, and board layout and routing concepts.

The MPC106 has a single clock input (SYSCLK) which is used to clock the PCI interface. The PCI interface of the system must be run in phase with this input. The PCI 2.1 specification allows the system designer to have the flexibility of laying out their PCB such that all components on the PCI bus are required to have their PCI clocks routed within 2.0 ns of each other. This point, combined with the PCI 2.1 specification shown in Figure 1 which states that 0 ns input hold time is required, results in systems where the output hold requirement is 2.0 ns.

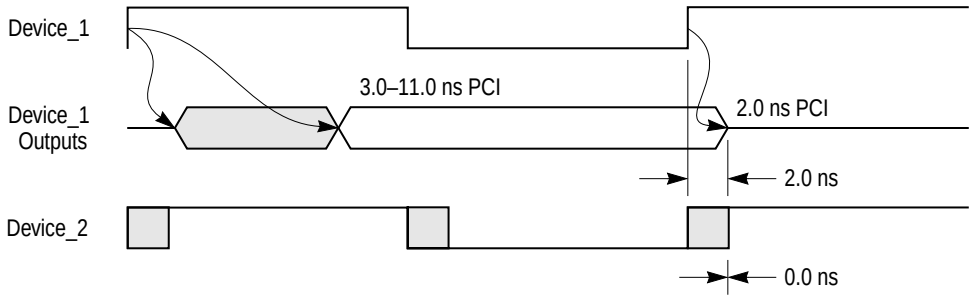

Figure 1. PCI 2.1 Specifications

In Figure 1, Device_2 has its clock shifted 2.0 ns requiring Device_1 to provide 2.0 ns output hold in order to meet Device_2's requirement of 0 ns input hold.

The MPC106 PCI Bridge has an output hold specification of 0.5 ns. In order to maximize the system design constraints with regard to PCI hold time the PCI clock signal to the MPC106 should be delayed by 1.5 ns. with respect to the earliest PCI device. This will effectively place it a maximum of 0.5 ns in front of the last PCI device. This is shown in Figure 2.

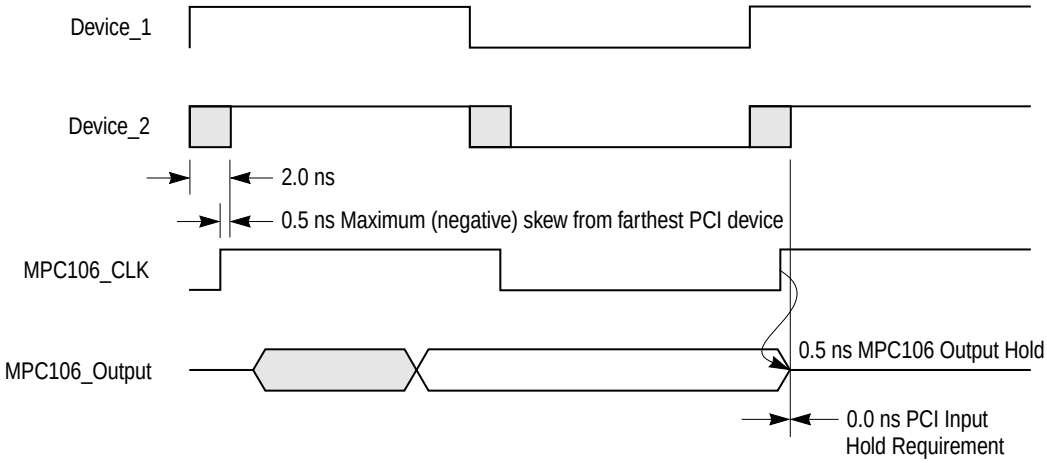

Figure 2. MPC106 PCI Clock Skew

In this fashion, the output hold time of MPC106 (0.5 ns) combined with the 1.5 ns clock skew from the earliest PCI device (Device_1) provides a device shifted 2.0 ns with respect to Device_1 (that is, Device_2) to still "see" a 0 ns input hold.

Delaying the input clock to MPC106 with respect to other devices on PCI also results in a change in the amount of input hold time the MPC106 sees when these devices drive inputs to the MPC106 and provide the minimum 2.0 ns of hold time on their outputs. This is shown Figure 3.

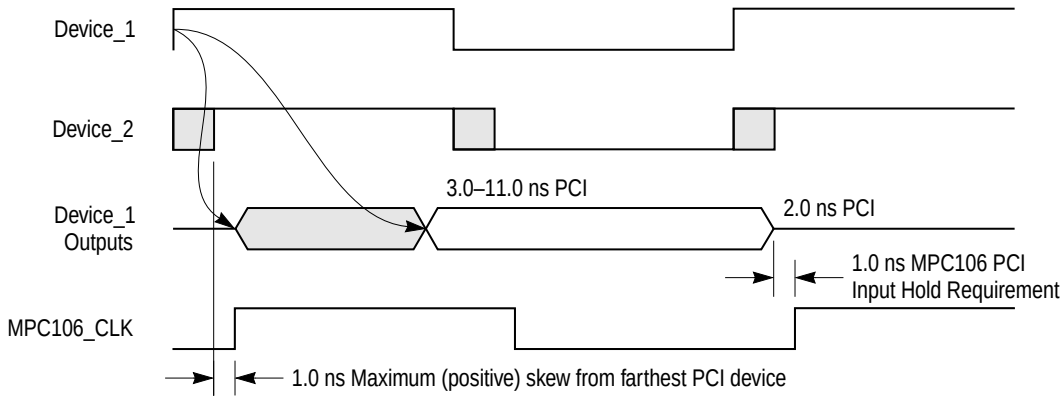

Figure 3. Other Devices Driving to MPC106

In Figure 3, Device_1 is skewed -2.0 ns with respect to Device_2 (worst case PCI 2.1). Since the input hold requirement of MPC106 is -1.0 ns this allows for the MPC106 to be routed a maximum of 1.0 ns behind the farthest PCI device (Device_2).

It should also be noted that when the clock signal to MPC106 is skewed it may be necessary to skew the clocks to all of the other devices that are on the processor interface of MPC106 by the same amount. This maintains the appropriate synchronized timing relationship between the processor module clocks and the MPC106 clock. Additional hold time may also be provided on MPC106 outputs by using the 40ohm output drivers. This is accomplished by programming the MPC106 Output Drive Control Register (ODCR)—0x73. For more information refer to *Addendum to MPC106 PCIB/MC User's Manual*.

Example: A system has the components shown in Table 1. Note that Device_1 is a PCI device that requires 1.5 ns input hold time. The clock driver and layout of the board is such that the clock skew to all the PCI components can be kept to 1.0 ns.

Table 1. PCI Design Example Devices

	Input		Output	
	Setup	**Hold**	**Valid**	**Hold**
Device_1	7	1.5	11	2
Device_2	7	0	11	2
MPC106	7	-1	11	.5

Solution: Place components so that the device requiring the most hold time (Device_1) on inputs is the earliest PCI device (that is, has the shortest clock trace). Route the remaining device (Device_2) such that it is within the 1.0 ns window that can be achieved with this clock driver and layout. Route the MPC106 so that it is the latest PCI device, delaying the clock trace to it by 0.5–2.0 ns with respect to Device_2 (that is, the last device excluding the MPC106). This solution is shown in Figure 4. It can be seen in this example that the MPC106 provides 2.0 ns of output hold to the earliest device (Device_1) and that outputs from this device have the required -1.0 ns of hold time required by the MPC106.

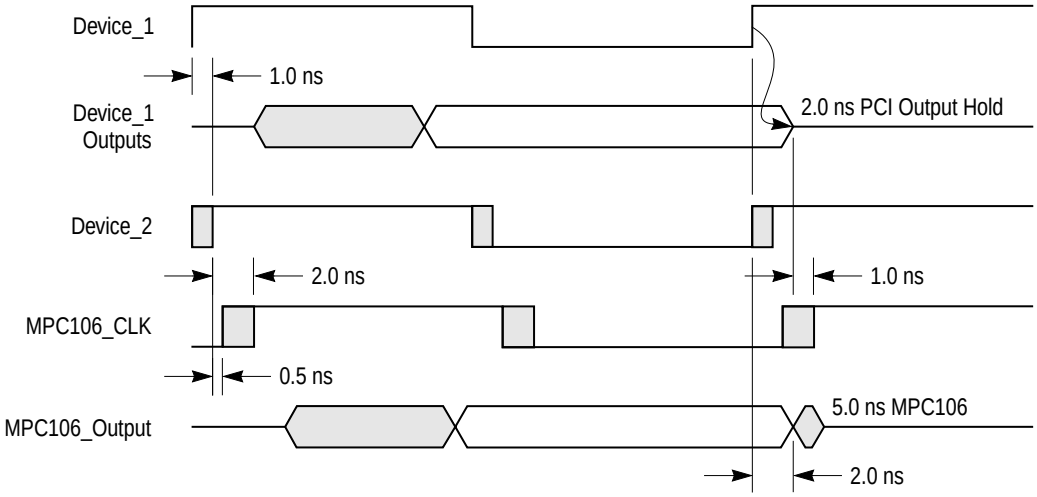

Figure 4. PCI Example Routing Solution

Summary: By routing the PCI clock to MPC106 a maximum of 0.5 ns ahead of the farthest PCI device's clock and not more than 1.0 ns behind that device's clock it is possible to maximize the amount of hold time within a system layout. This window allows for the maximum amount of skew (2.0 ns) between all other PCI devices within the layout. To the extent that the other device's clock-to-clock skew can be minimized, margin can be provided to devices in the system that require more input hold than the PCI 2.1 specified 0 ns.

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