AN1729

BurstRAM to ZBT™ RAM

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The recent product announcements for the ZBT family of synchronous memories have received a warm reception with a wide range of customers. The ability to perform back–to–back read/write cycles without any intermediate deselect cycles offers a substantial performance improvement for a variety of platforms which now utilize standard BurstRAMs. This application note describes some of the footprint changes required to adapt a current BurstRAM socket to a ZBT device. In addition, some of the operational differences are also discussed.

PINOUT DIFFERENCES

Figure 1 shows a comparative pinout for the MCM69P737 BurstRAM and the MCM63Z736 ZBT RAM. Note there are relatively few pinout differences, most of which are easily modified. The changes in pin assignment required to modify a BurstRAM socket to a ZBT device are listed in Table 1.

The ZBT devices do not have a global byte write pin ($\overline{SGW}$), but instead relies upon the state of the byte select inputs ($\overline{SBa}$ – $\overline{SBd}$) to select the current byte write mode. The $\overline{SGW}$ functionality is replicated by forcing all four of the byte selects to a binary low state during a write cycle instantiation ($\overline{SBa}$ – $\overline{SBd}$ = 0). Figure 2 shows a gate–level description of an external implementation of $\overline{SGW}$ in combination with $\overline{SW}$.

Another difference of interest to the designer is that of the simplified burst logic. The ZBT has only the ADV pin to indicate burst cycles. Address and control information is latched with ADV = 0 to initiate a burst cycle. Subsequent cycles have ADV = 1 which causes the address and control inputs to be ignored until the ADV pin is deasserted. For most burst mode applications, tying the BurstRAM $\overline{ADSC}$ to the ZBT ADV will accomplish the burst functionality.

FUNCTIONAL DIFFERENCES

The primary functional difference between the ZBT and BurstRAM involves the write cyles (both burst and non–burst). A typical pipelined BurstRAM (ie., the MCM69P737) requires write data to be presented to the part coincident with the address at the initiation of the write cycle. The ZBT, however, is pipelined for both reads and writes, so the write data is latched into the part two (2) clock cycles after the initiation of the write. It is this one fundamental difference that will require the most attention on the part of the circuit designer.

CONCLUSION

While logic changes may be required for most BurstRAM applications, the conversion to a ZBT architecture should require minimal effort on the part of PCB layout teams. In addition, the logic changes are generally manageable and should require only a modest effort on the part of the circuit designer to allow quick and easy migration to this new and exciting memory technology.

Table 1. Pipelined BurstRAM and ZBT Pin Assignment Differences

Pin Locations	BurstRAM Pin Assignment	ZBT Pin Assignment
14	NC	V_{DD}
16	NC	V_{DD}
64	NC	V_{SS}
66	NC	V_{DD}
83	ADV	NC
84	$\overline{ADSP}$	NC
85	$\overline{ADSC}$	ADV
87	$\overline{SW}$	$\overline{CKE}$ (Tie to V_{SS})
88	$\overline{SGW}$	$\overline{SW}$

ZBT and Zero Bus Turnaround are trademarks of Integrated Device Technology, Inc., and the architecture is supported by Micron Technology, Inc. and Motorola, Inc.

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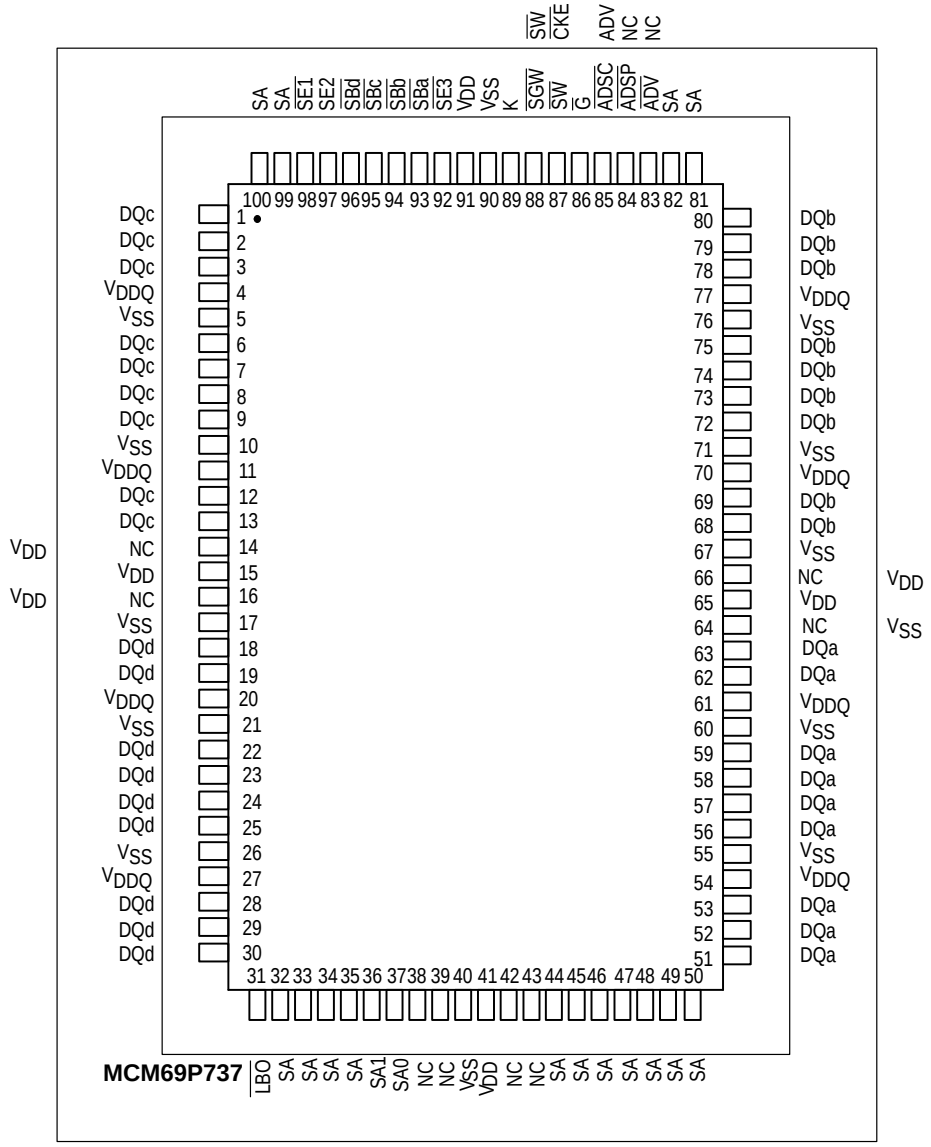

Figure 1. Pipelined BurstRAM and ZBT Pinout Comparison

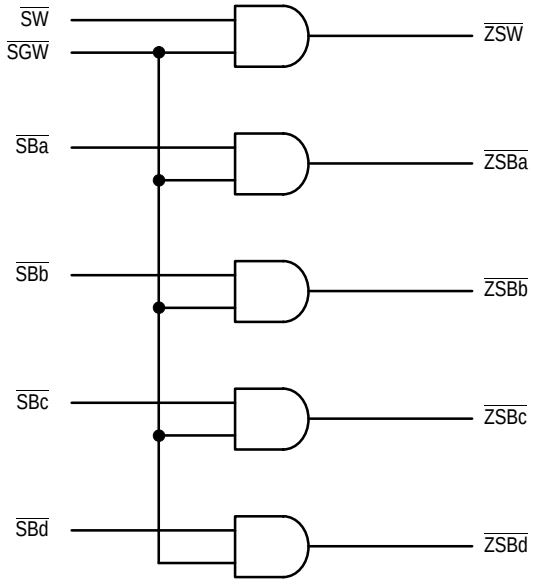

Figure 2. External SGW Logic

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