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MPC8xx to BurstRAM Interfacing

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INTRODUCTION

In many applications DRAM provides sufficient performance for MPC8xx PowerPC™ systems. This family of parts currently includes the MPC860, MPC823, MPC850, MPC801, and in the future MPC8260 PowerQUICC II™. In some cases where performance must be optimized, or cache performance is poor, it may be desirable to manipulate data in fast external memory. The optimum burst performance for an MPC8xx part is a 2,1,1,1 for both external read and write accesses. Current MPC8xx parts are available with external bus frequencies up to 50 MHz; however, future generations will include 66 MHz and 100 MHz requiring fast static memory to achieve optimum performance. This application note describes how to interface the MPC8xx to the MCM69F536C (32K x 36) and the MCM69F618C (64K x 18) synchronous fast static RAMs.

MPC8xx TO BurstRAM INTERFACING (OPTION 1)

Figure 1 shows the hardware interface between the MPC8xx processor and the MCM69F536C BurstRAM. This interface is completely glueless, since the MPC8xx UPM (User Programmable Machine) is used to shape the signals correctly for the BurstRAM.

The address lines are connected directly with SA(14–0) on the BurstRAM mapping to ADDR(15–29) on the MPC8xx. $SA14_{BRAM}$ is connected to $ADDR15_{8xx}$, all the way thru $SA0_{BRAM}$ to $ADDR29_{8xx}$. Note, that in the PowerPC, $ADDR0_{8xx}$ is the most significant address line and $ADDR31_{8xx}$ is the least significant. $ADDR(30–31)_{8xx}$ are not connected, since the UPM byte strobes ($\overline{WE0:3}$)$_{8xx}$ are used to select the individual bytes in a word (a word in 8xx PowerPC is 32 bits).

The data lines of the processor, $Data(0:7)_{8xx}$, are connected to memory data lines $DQ(34:27)_{BRAM}$ and controlled by the MPC8xx using pin $\overline{WE0}_{8xx}$. This, in turn, drives $\overline{SBd}$ of the RAM and consequently, port DQd. $DQ35_{BRAM}$ may be connected to $PRTY0_{8xx}$, if parity is required.

$Data(8:15)_{8xx}$ are connected to memory data lines $DQ(25:18)_{BRAM}$ and controlled by the MPC8xx using pin $\overline{WE1}_{8xx}$. This, in turn, drives $\overline{SBc}$ of the RAM and consequently, port DQc. $DQ26_{BRAM}$ may be connected to $PRTY1_{8xx}$, if parity is required.

$Data(16:23)_{8xx}$ are connected to memory data lines $DQ(16:9)_{BRAM}$ and controlled by the MPC8xx using pin $\overline{WE2}_{8xx}$. This, in turn, drives $\overline{SBb}$ of the RAM and consequently, port DQb. $DQ17_{BRAM}$ may be connected to $PRTY2_{8xx}$, if parity is required.

$Data(24:31)_{8xx}$ are connected to memory data lines $DQ(7:0)_{BRAM}$ and controlled by the MPC8xx using pin $\overline{WE3}_{8xx}$. This, in turn, drives $\overline{SBa}$ of the RAM and consequently, port DQa. $DQ8_{BRAM}$ may be connected to $PRTY3_{8xx}$, if parity is required.

It should be noted the MCM69F536C ports DQa, DQb, DQc, and DQd represent specific groups of data pins on the memory device. Therefore, pin allocation is critical for each port, but the priority of each pin within a port is not fixed and gives flexibility to the designer. Additionally, the allocation of the RAM data ports to the processor data pins could be altered to accommodate different layout requirements or limitations. This is due to the fact that there is no most significant bit or byte (MSB) to least significant bit or byte (LSB) scheme within the RAM. Consequently, any port can be allocated as the MSB or LSB, and any port pin can be weighted MSB or LSB within the port. For additional information, refer to Motorola data sheet MCM69F536C/D.

Synchronous global write, $\overline{SGW}_{BRAM}$, is tied high and disabled to allow byte write capability. This means that byte write selection is controlled via the $\overline{SBx}_{BRAM}$ pins as detailed above.

As byte write inputs are used as read/write control, the synchronous write, $\overline{SW}_{BRAM}$, is disabled by being tied low.

The MPC8xx $\overline{TS}$ signal may be used to initiate transfers to and from the memory. This is connected to $\overline{ADSP}_{BRAM}$ in preference to $\overline{ADSC}_{BRAM}$. $\overline{ADSC}_{BRAM}$ is designed for cache access and has a single cycle initial transfer on a burst write, incompatible with the MPC8xx write cycle, i.e., it expects the data before it is ready from the processor. Therefore, $\overline{ADSC}_{BRAM}$ is pulled high to its inactive state. In comparison, $\overline{ADSP}_{BRAM}$ supports a 2,1,1,1 cycle access, the optimum for the MPC8xx.

The RAM synchronous chip enable, $\overline{SE1}_{BRAM}$, is controlled by one of the MPC8xx $\overline{CS}$ lines, the exact operation of which may be controlled on a one–quarter clock basis, this means down to a 5 ns resolution at 50 MHz. The UPM table entries define the exact operation of the $\overline{CS}_{8xx}$ and are discussed later. $SE2_{BRAM}$ and $\overline{SE3}_{BRAM}$ are configured as high and low respectively, to allow $\overline{SE1}_{BRAM}$ only to act as the chip enable.

Output enable, $\overline{G}_{BRAM}$, and synchronous address advance, $\overline{ADV}_{BRAM}$, lines are also controlled by the UPM, this time using the general purpose lines. These may be toggled at two points during each clock cycle. Refer to Chapter 16 in the *MPC8xx User's Manual* for more information.

The linear burst order, $\overline{LBO}_{BRAM}$, input is tied low, ensuring linear burst counting.

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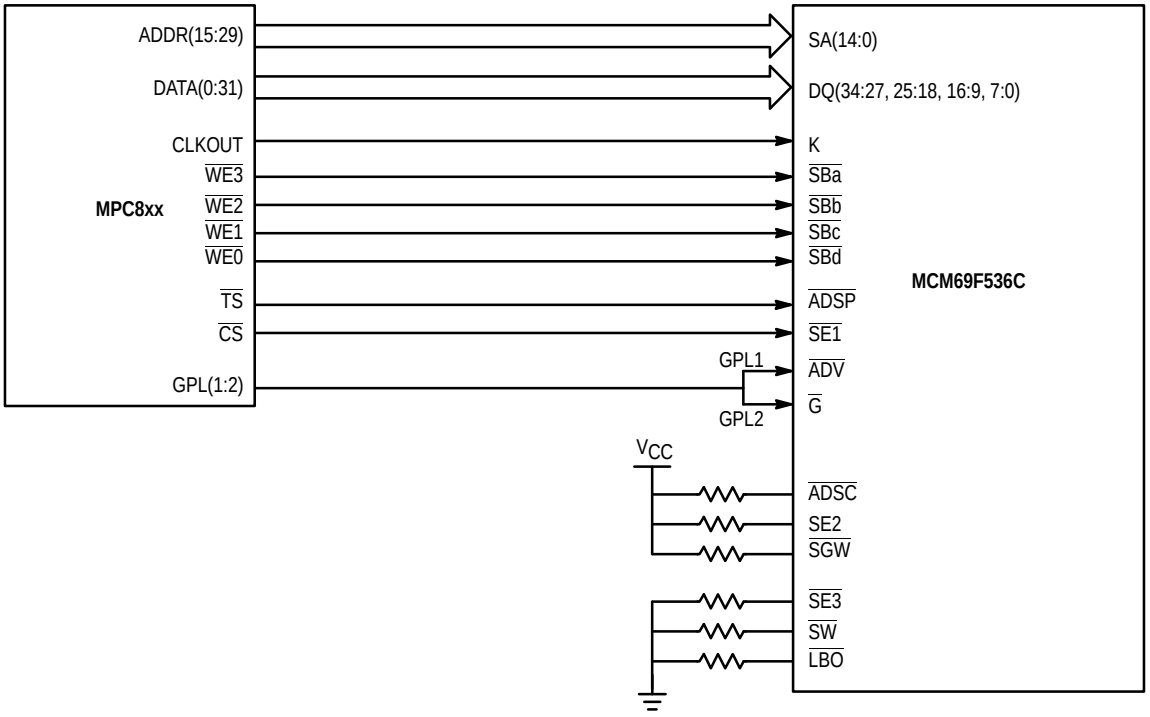

Figure 1. MPC8xx to MCM69F536C Interface

MPC8xx TO BurstRAM INTERFACING (OPTION 2)

Figure 2 illustrates the hardware interface between the processor and the memory. Again, this interface is completely glueless, since the MPC8xx UPM is used to shape the signals correctly for the BurstRAM.

The address lines are connected directly with SA(15–0) on the BurstRAM mapping to ADDR(14–29) on the MPC8xx. $SA15_{BRAM}$ is connected to $ADDR14_{8xx}$, all the way thru $SA0_{BRAM}$ to $ADDR29_{8xx}$. Note that in the PowerPC, $ADDR0_{8xx}$ is the most significant address line and $ADDR31_{8xx}$ is the least significant. $ADDR(30–31)_{8xx}$ are not connected, since the UPM byte strobes $(\overline{WE0:3})_{8xx}$ are used to select the individual bytes in a word (a word in the 8xx PowerPC is 32 bits).

The data is split between the two memory devices. $DATA(0–7)_{8xx}$ is selected by $\overline{WE0}_{8xx}$; therefore, $\overline{WE0}_{8xx}$ is mapped to $\overline{UW}_{BRAM}$ on the first BurstRAM and $DATA(0:7)_{8xx}$ is mapped to $DQ(16:9)_{BRAM}$. Likewise, $\overline{WE1}_{8xx}$ is mapped to $\overline{LW}_{BRAM}$ and $DATA(8:15)_{8xx}$ is mapped to $DQ(7:0)_{BRAM}$. $DQ17_{BRAM}$ and $DQ8_{BRAM}$ may be connected to $PRTY0_{8xx}$ and $PRTY1_{8xx}$, if parity is required.

The second BurstRAM is connected similarly, with $\overline{WE2}_{8xx}$ mapping to $\overline{UW}_{BRAM}$ and $\overline{WE3}_{8xx}$ mapping to $\overline{LW}_{BRAM}$. $DATA(16:23)_{8xx}$ is mapped to $DQ(16:9)_{BRAM}$ and $DATA(24:31)_{8xx}$ to $DQ(7:0)_{BRAM}$. Again, $DQ17_{BRAM}$ and $DQ8_{BRAM}$ may be connected to $PRTY2_{8xx}$ and $PRTY3_{8xx}$, if parity is required.

Synchronous global write, $\overline{SGW}_{BRAM}$, is tied high and disabled to allow byte write capability. This means that byte write selection is controlled via the $\overline{UW}_{BRAM}$ and $\overline{LW}_{BRAM}$ pins as detailed above.

As byte write inputs are used as read/write control, synchronous write, $\overline{SW}_{BRAM}$, is disabled by being tied low.

The MPC8xx $\overline{TS}$ signal may be used to initiate transfers to and from the memory. This is connected to $\overline{ADSP}_{BRAM}$ in preference to $\overline{ADSC}_{BRAM}$. $\overline{ADSC}_{BRAM}$ is designed for cache access and has a single cycle initial transfer on a burst write, incompatible with the MPC8xx write cycle, i.e., it expects the data before it is ready from the processor. Therefore, $\overline{ADSC}_{BRAM}$ is pulled high to its inactive state. In comparison, $\overline{ADSP}_{BRAM}$ supports a 2,1,1,1 cycle access, the optimum for the MPC8xx.

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Output enable, $\overline{G}_{BRAM}$, and synchronous address advance, $\overline{ADV}_{BRAM}$, lines are also controlled by the UPM, this time using the general purpose lines. These may be toggled at two points during each clock cycle. Refer to Chapter 16 in the *MPC8xx User's Manual* for more information.

The linear burst order, $\overline{LBO}_{BRAM}$, input is tied low ensuring linear burst counting.

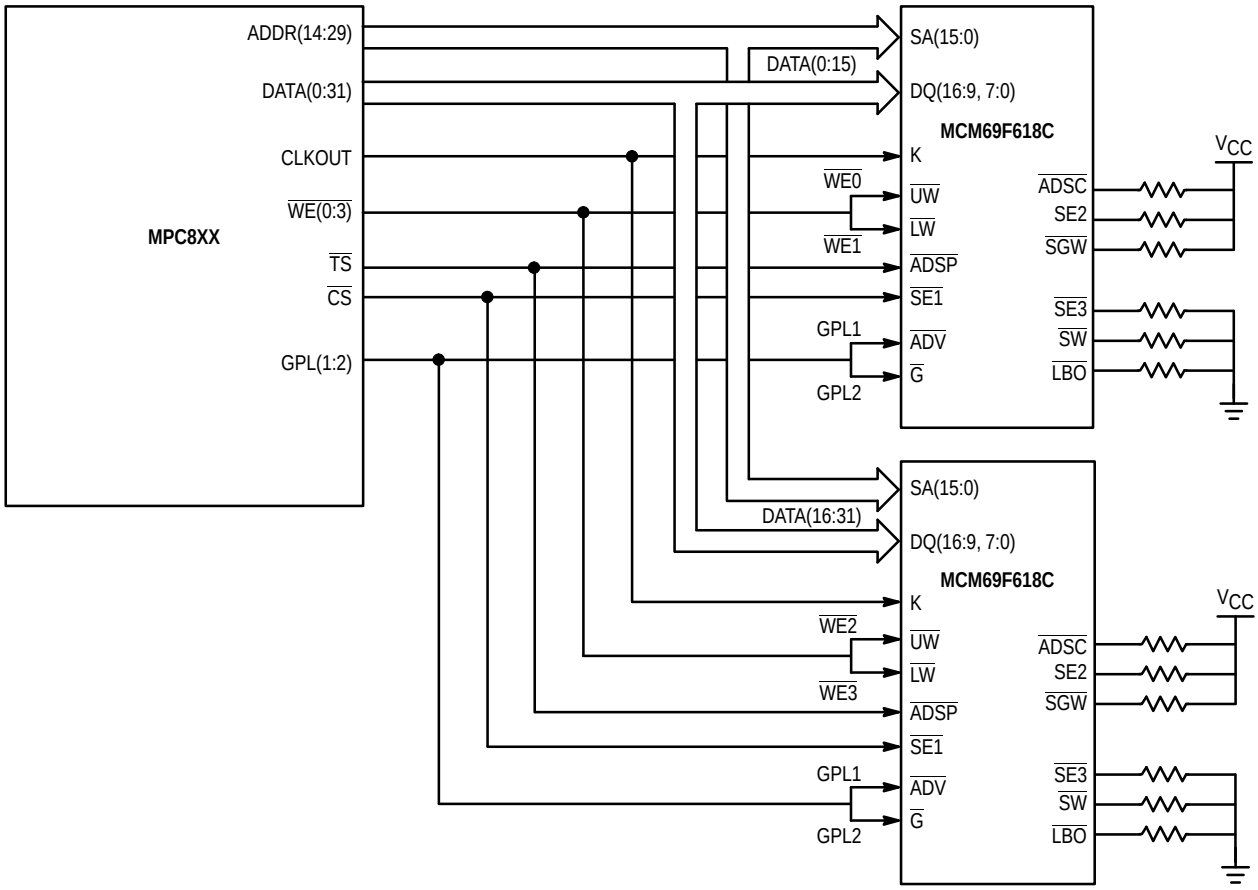

Figure 2. MPC8xx to MCM69F618C Interface

PROGRAMMING A 2,1,1,1 BURST WRITE CYCLE

Figure 3 illustrates a 2,1,1,1 burst write cycle at 50 MHz. The control signals are sampled at the rising edge of clock, K_{BRAM}, where K_{BRAM} is driven by $CLKOUT_{8xx}$ at bus frequencies. Output enable, $\overline{G}_{BRAM}$, is negated for the full write cycle. The first access is a two–cycle write, initiated by asserting $\overline{ADSP}_{BRAM}$ and $\overline{SE1}_{BRAM}$, together with the address on the first rising edge of K_{BRAM}. If $\overline{ADSP}_{BRAM}$ and $\overline{ADSC}_{BRAM}$ are negated and $\overline{UW}_{BRAM}$ and $\overline{LW}_{BRAM}$ are asserted on the following clock, then a write is performed. To implement a burst cycle, $\overline{ADV}_{BRAM}$ is asserted for the full access. The next three writes are performed on subsequent clocks. Note that the address is automatically incremented by the BurstRAM. $\overline{ADV}_{BRAM}$, $\overline{UW}_{BRAM}$, and $\overline{LW}_{BRAM}$ remain asserted for the complete cycle and the burst cycle is only terminated when $\overline{ADV}_{BRAM}$ is negated.

The critical timing for the write is the data valid to clock high, t_{DVKH}. Therefore, the following expression must be met:

$$t_{DVKH} < t_{CLK} - t_8$$

so

$$0 < t_{CLK} - t8 - t_{DVKH}$$

where: t_8 = MPC8xx CLKOUT to data valid = 13 ns
t_{CLK} = clock period at 50 MHz = 20 ns
t_{DVKH} = data setup time for BurstRAM = 2.5 ns

Therefore, 0 < 20 –13 – 2.5, giving a 4.5 ns margin.

The programming of the UPM is as follows.

For the first clock, $\overline{CS}_{8xx}$ drives $\overline{SE1}_{BRAM}$, so it is asserted until the rising edge of $CLKOUT_{8xx}$ and then negated. Therefore, the MSB of the first UPM word is 0001. The $\overline{WE}_{8xx}$ pins are continually asserted and the next nibble is 0000. GPL1 and GPL2 are used for $\overline{ADV}_{BRAM}$ and $\overline{G}_{BRAM}$, and as the next nibble controls GPL0, it is programmed to 1111. Since this is a burst write cycle, $\overline{ADV}_{BRAM}$ is asserted and $\overline{G}_{BRAM}$ negated, and the fourth nibble is programmed to 0011. The remaining GPL lines are not used and the next byte should be programmed to 1111 1111. For the final byte; LOOP is disabled, exceptions are not enabled, address multiplex is disabled, address incrementing is disabled, $\overline{TA}_{8xx}$ is asserted for termination on the next clock, no precharge is enabled, and it is not the last entry. The final entry is 0000 0000. Therefore, the complete first entry is10F3FF00.

The next entry is almost identical, the only difference is in the first nibble, which is 1111 since the $\overline{CS}_{8xx}$ line remains negated. The same is true for the next two entries of the burst that implement the second and third burst accesses. Therefore, the next three entries are F0F3FF00. The final entry negates the $\overline{ADV}_{BRAM}$ signal, enables exceptions, negates $\overline{WE}_{8xx}$, $\overline{TA}_{8xx}$, and sets the LAST bit; making the complete entry F1FFFF45.

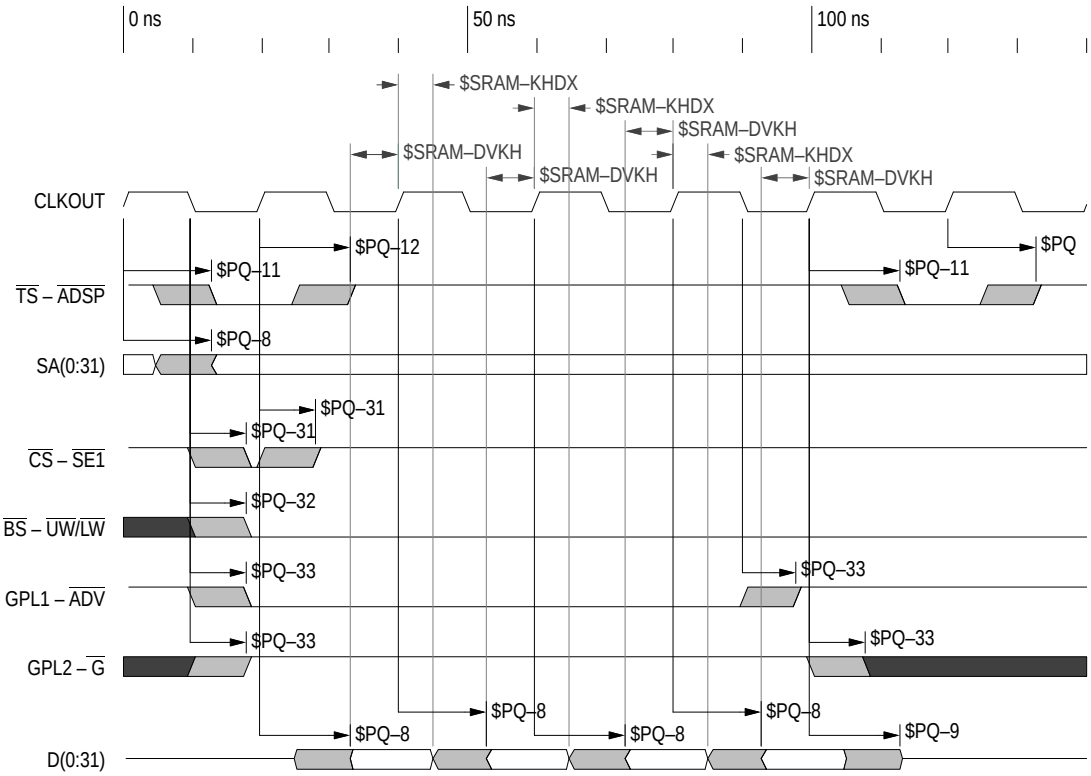

Figure 3. 50 MHz Burst Write Example

When an internal master request for a new access to external memory, the address and type of transfer are compared to each valid bank defined in the base register (BR). The value in the (BRx)[MS] selects the UPM to handle the memory access. External memory access requests are single–beat and burst reads and writes. The UPM RAM array has start addresses associated with each of these cycle types as detailed below.

Read single–beat pattern (RSS) RAM ADDRESS = 0x′00

Read burst cycle pattern (RBS) RAM ADDRESS = 0x′18

Write single–beat pattern (WSS) RAM ADDRESS = 0x′08

Write burst cycle pattern (WBS) RAM ADDRESS = 0x′20

Therefore, as we begin to program a burst write sequence, the UPM entries in this example should commence at location 0x′20 in the UPM table.

In summary, the following entries should be programmed at location 20hex in the UPM table:

10F3FF00

F0F3FF00

F0F3FF00

F0F3FF00

F1FFFF45

PROGRAMMING A 2,1,1,1 BURST READ CYCLE

Figure 4 illustrates a 2,1,1,1 burst read cycle at 50 MHz. Output enable, $\overline{G}_{BRAM}$, is asserted for the full read cycle. The first access is a two–cycle read, initiated by asserting $\overline{ADSP}_{BRAM}$ and $\overline{SE1}_{BRAM}$, together with the address on the first rising edge of K_{BRAM}, where K_{BRAM} is driven by $CLKOUT_{8xx}$. If $\overline{ADSP}_{BRAM}$ and $\overline{ADSC}_{BRAM}$ are negated and $\overline{UW}_{BRAM}$ and $\overline{LW}_{BRAM}$ are negated on the following clock, then a read is performed. To implement a burst cycle, $\overline{ADV}_{BRAM}$ is asserted for the full access. The next three reads are performed on subsequent clocks. Note that the address is automatically incremented by the BurstRAM. $\overline{ADV}_{BRAM}$ remains asserted for the complete cycle and the burst cycle is only terminated when $\overline{ADV}_{BRAM}$ is negated.

The critical timing for the read is data valid to clock high, t_{KHQV}. Therefore, the following expression must be met:

$$t_{KHQV} < t_{CLK} - t_{20}$$

so

$$0 < t_{CLK} - t_{20} - t_{KHQV}$$

where: t_{20} = MPC8xx data valid to CLKOUT (setup time) = 4 ns

t_{CLK} = clock period at 50 MHZ = 20 ns

t_{KHQV} = data setup time for BurstRAM = 11 ns

Therefore, 0 < 20 – 11 – 4, giving a 5 ns margin.

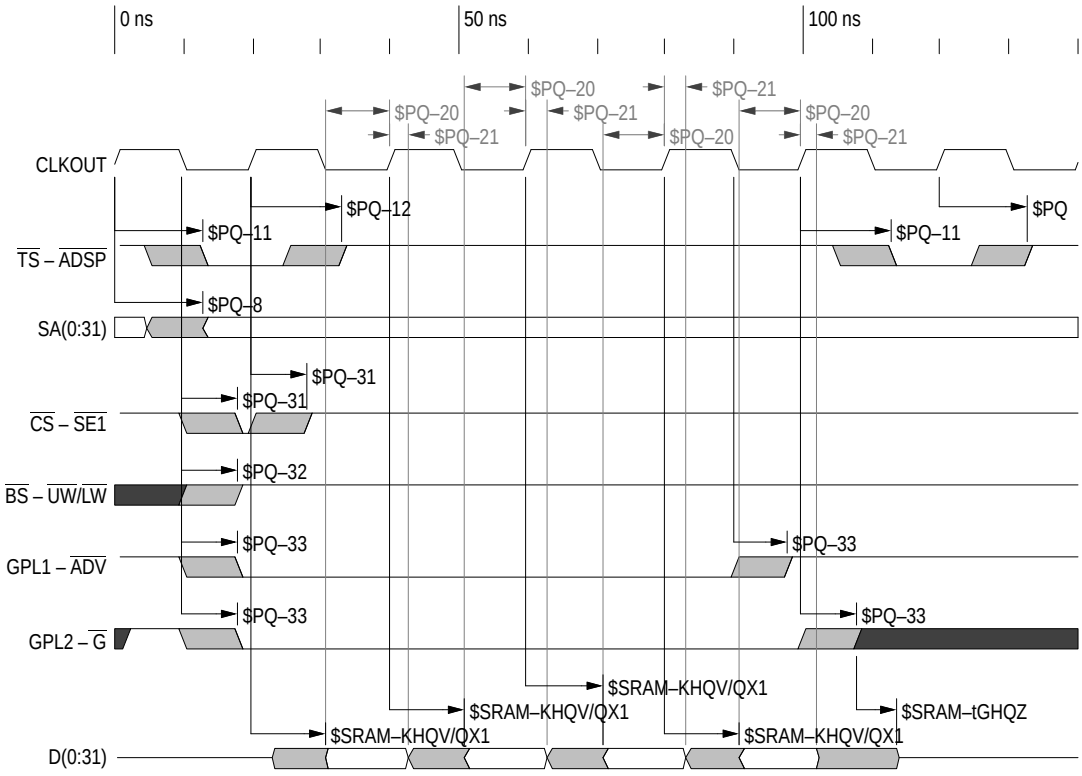

Figure 4. 50 MHz Burst Read Example

The programming of the UPM is as follows.

For the first clock, $\overline{CS}_{8xx}$ drives $\overline{SE1}_{BRAM}$, so it is asserted until the rising edge of $CLKOUT_{8xx}$ and then negated. Therefore, the MSB of the first UPM word is 0001. The $\overline{WE}_{8xx}$ pins are continually negated and the next nibble is 1111. GPL1 and GPL2 are used for $\overline{ADV}_{BRAM}$ and $\overline{G}_{BRAM}$, as the next nibble controls GPL0, it is programmed to 1111. Since this is a burst write cycle, $\overline{ADV}_{BRAM}$ is asserted and $\overline{G}_{BRAM}$ negated, and the fourth nibble is programmed to 0000. The remaining GPL lines are not used, so the next byte should be programmed to 1111 1111. For the final byte; LOOP is disabled, exceptions are not enabled, address multiplexed is disabled, address incrementing is disabled, $\overline{TA}_{8xx}$ is asserted for termination on the next clock, no precharge is enabled, and it is not the last entry. The final entry is 0000 0000. Therefore, the complete first entry is10F3FF00.

The next entry is almost identical, the only difference is in the first nibble, which is 1111 since the $\overline{CS}_{8xx}$ line remains negated. The same is true for the next two entries of the burst that implement the second and third burst accesses. The next three entries are FFF0FF00. The final entry negates the $\overline{ADV}_{BRAM}$ signal, enables exceptions, negates $\overline{G}_{BRAM}$ and $\overline{TA}_{8xx}$, and sets the LAST bit; making the complete entry FFF0FF45.

In summary, the following entries should be programmed in at location 08hex in the UPM table:

1FF0FF00
FFF0FF00
FFF0FF00
FFF0FF00
FFFDFF45

PROGRAMMING A SINGLE WRITE CYCLE

The programming of a single write cycle is essentially similar to the burst write. The first access is 10FFFF00. Note that the only difference is that $\overline{ADV}_{BRAM}$ is negated. The second cycle is set to F1FFFF45, the same as the final cycle for the burst. The following entries should be set at 0x18 in the UPM table:

10FFFF00
F1FFFF45

PROGRAMMING A SINGLE READ CYCLE

The programming of a single read cycle is essentially similar to the burst read. The first access is 10FFFF00. Note that the only difference is that $\overline{ADV}_{BRAM}$ is negated. The second cycle is set to F1FDFF45, the same as the final cycle for the burst. The following entries should be set at 0x00 in the UPM table:

10FCFF00
F1FDFF45

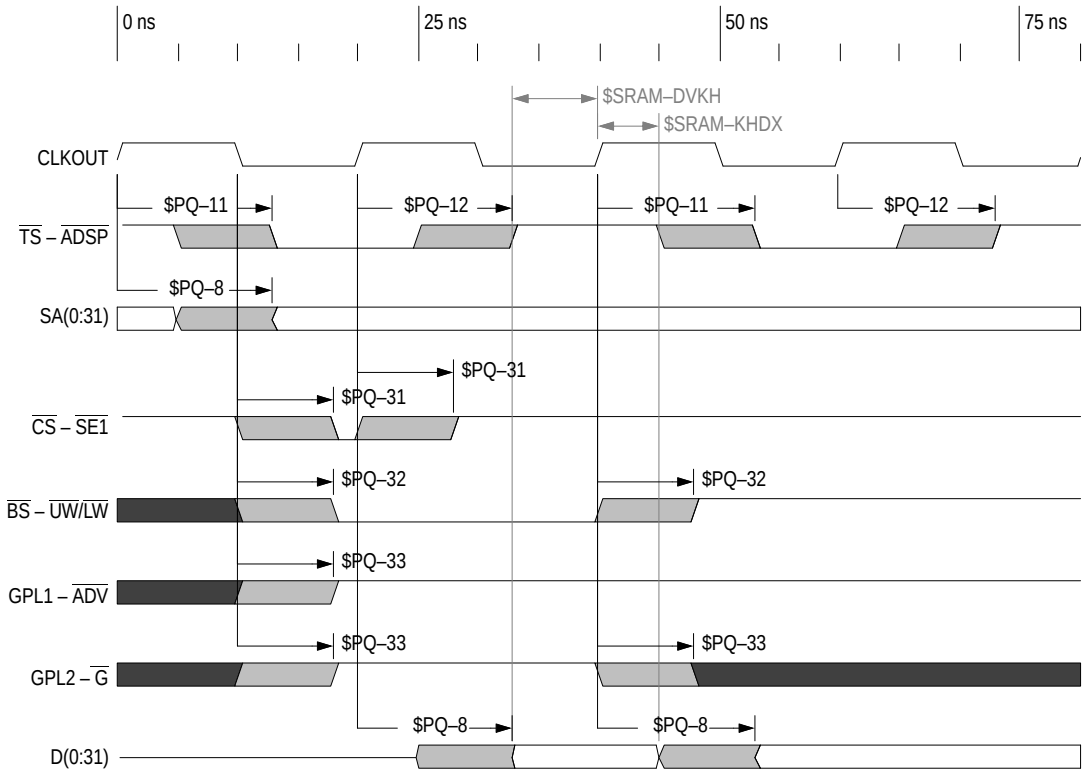

Figure 5. 50 MHz Single Write Example

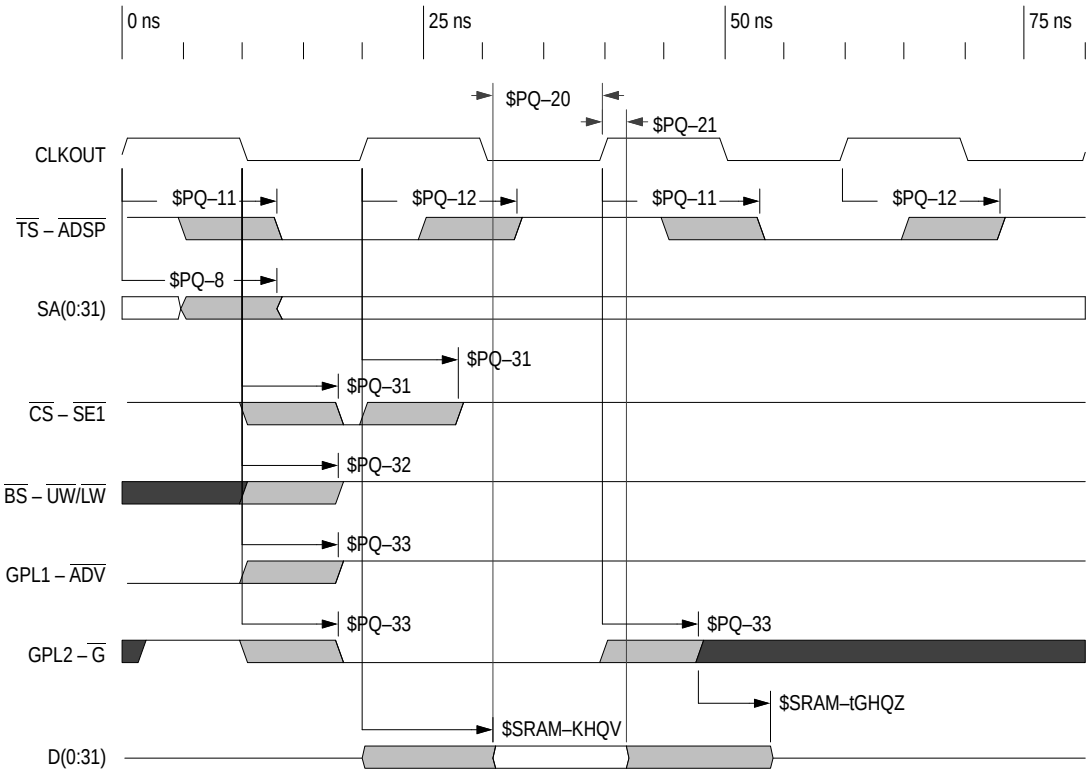

Figure 6. 50 MHz Single Read Example

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