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Converting DSP56303 Designs to DSP56307 Designs

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This document details the differences between the DSP56303 and the DSP56307 that must be considered when a system based on the DSP56303 is redesigned for use on the DSP56307. The differences fall into two major categories: required changes and optional enhancements. Refer to the DSP56303 and DSP56307 technical data sheets and their associated documentation for complete information. Appendix A lists all associated documents.

Contents

1 Required Changes

Both hardware and software changes are required when a DSP56307 replaces a DSP56303 in a system. Revision D of the DSP56303 already includes some of the changes to the Operating Mode Register.

1.1 Hardware/Layout

- Split Voltages — The DSP56307 has split core and I/O supply voltages. The core requires a V_{CC} of 2.5V +/- 0.2V, and I/O requires a V_{CC} of 3.3V +/- 0.3V. The DSP56307 I/O pins are not 5V tolerant as they are on the DSP56303. See the DSP56307 data sheet for the most recent information on supply voltage tolerance.
- Pinout — The DSP56307 physical pinout differs from that of the DSP56303, so you cannot directly replace a DSP56303 with a DSP56307 without adjusting the board layout. Refer to the DSP56307 technical data sheet for details on the device pinout. **Table 1** shows the pin assignment differences between the DSP56303 PBGA packages and the DSP56307 PBGA packages. Because the DSP56307 is not available in a TQFP package, this document does not consider the DSP56303 TQFP package.

Table 1. DSP56303 to DSP56307 Pinout Differences

Pin Number	DSP56303 Signal Name	DSP56307 Signal Name
C7	VCCQ	VCCQL
F12	VCCA	VCCQH
G13	VCCQ	VCCQL
H1	NC	VCCQH
H2	VCCQ	VCCQL
M7	NC	VCCQH
N9	VCCQ	VCCQL

NOTES:
VCCQ - DSP56303 Core supply voltage 3.3V +/- 0.3V
VCCA - DSP56303 I/O supply voltage 3.3V +/- 0.3V
NC - pin is not connected, Reserved
VCCQL - DSP56307 Core supply voltage 2.5V +/- 0.2V
VCCQH - DSP56307 I/O supply voltage 3.3V +/- 0.3V

Bold pin numbers have a new power supply voltage on the DSP56307. Pin F12 has a new signal name on the DSP56307, but the power supply value for this pin has not changed.
See the DSP56307 data sheet for the most recent information on supply voltage tolerance.

- Dual Power Supply Circuits — When working with a split-voltage part, you must take care in designing the power supplies. Two examples of power supply circuits to use as a reference are a switching regulator and a linear regulator. Motorola does not recommend using a switching regulator because of the noise it generates. The PLL supply on the DSP is sensitive to any noise on the board, so noise must be kept to a minimum. If a switching regulator is necessary in a system, take special care to keep the PLL supply clean.

  Figure 1 shows the power supply circuit design used on the DSP56307EVM board. In this design, the voltage supply goes to both a 5.0V and 3.3V linear regulator. The 5.0V output is routed to a 2.5V regulator to give Vccql. This is only one option you can use for a dual-supply circuit. See the *DSP56307EVM User's Manual* for details on this design. Another option would be to channel the input voltage into the 5.0V linear regulator and channel both the 3.3V and 2.5V regulators to come off the output of the 5.0V regulator.
- PLL Supply — On the DSP56303, the PLL supply voltage ranges from -0.3V to +4.0V. For the DSP56307, this supply voltage reaches a maximum of 3.3V instead of 4.0V.

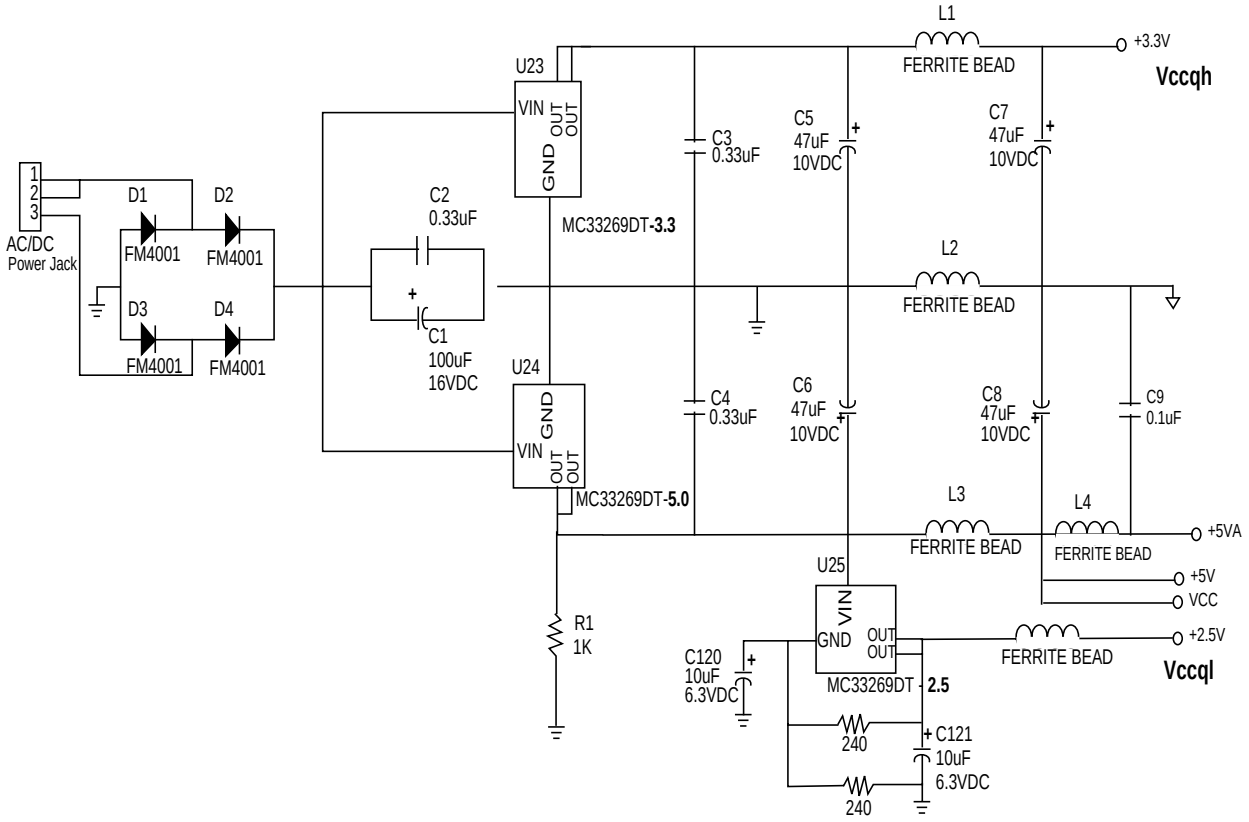

Figure 1. DSP56307 Power Supply Circuit Example

- PLL External Capacitor (PCAP Pin to V_{CCP}) — The equation for calculating the PLL external capacitor specification has changed, as **Table 2** shows. Note that the capacitance range for the DSP56307 is broader than for the DSP56303.

Table 2. PLL External Capacitor Value

Characteristic	Part	100 MHz			Unit
		Recommended	Min	Max	
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}) @ MF <= 4 @ MF > 4	DSP56303	-	(MF x 425) - 125 MF x 920	(MF x 590) - 175 MF x 920	pF
	DSP56307	(MF x 680) - 120 MF x 1100	(MF x 580) - 100 MF x 830	(MF x 780) - 140 MF x 1470	pF
NOTE: C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}).					

- Packaging — The DSP56303 is available in both 144-pin TQFP and 196-pin PBGA packages. The DSP56307 is available only in the 196-pin PBGA.
- Thermal Characteristics — Thermal resistance characteristics differ slightly between the DSP56303 and DSP56307. **Table 3** details these changes.

Table 3. Differences Between DSP56303 and DSP56307 Thermal Characteristics

Characteristic	Symbol	DSP56303 PBGA Value	DSP56307 PBGA Value	DSP56303 PBGA Value[3]	DSP56307 PBGA Value[3]	Unit
Junction-to-ambient thermal resistance[1]	$R_{\theta JA}$ or θ_{JA}	57	51.9	28	29.0	°C/W
Junction-to-case thermal resistance[2]	$R_{\theta JC}$ or θ_{JCA}	15	13.1	-	-	°C/W
Thermal characterization parameter	ψ_{JT}	8	2.45	-	1.68	°C/W

Notes: 1. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per SEMI G38-87 in natural convection. Measurements were done with parts mounted on thermal test boards conforming to specification EIA/JESD51-3.
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.
3. The test board has two 2-ounce signal layers and two 1-ounce solid ground planes internal to the test board.

- DC Characteristics — Because the DSP56307 pins are not 5V tolerant, the system designer must consider the input voltages on the MOD/$\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, PINIT, $\overline{\text{NMI}}$, and all JTAG, ESSI/SCI/Timer/HI08 pins. For the DSP56303, the maximum input on these pins is V_{CC} + 3.95; in contrast, the maximum value on the DSP56307 is V_{CCQH} + 0.3. Other differences between the DSP56303 and the DSP56307 are listed as follows:
  - The TTL output high voltage minimum is decreased on the DSP56307 to 2.4V from V_{CC}-0.4 (~2.9V) on the DSP56303.
  - Typical internal supply current during Normal and Wait modes is decreased on the DSP56307, **Table 4** shows.

Table 4. Internal Supply Current Comparison

Internal Supply Current	Symbol	DSP56303 Typ	DSP56307 Typ	DSP56303 Max	DSP56307 Max	Unit
In Normal mode	I_{CCI}	127	120	181	-	mA
In Wait mode	I_{CCW}	7.5	5	11	-	mA
In Stop mode	I_{CCS}	100	100	150	-	µA

  - The DC electrical characteristics are measured using a capacitive load (C_L) equal to 50pF for the DSP56307. In the DSP56303 data sheet, the values are measured with C_L = 50 pF + 2 TTL loads.

1.2 Software

This section presents software changes that may be required depending on the application.

1.2.1 Processor Type ID

The device ID register for both the DSP56303 and DSP56307 is at location $FFFFF5. The revision number varies for each device, but the derivative number (bits 11:0) reflects the processor derivative number ($303 or $307, respectively).

1.2.2 Control Registers

The DSP56307 Operating Mode Register (OMR) has four more bits than the DSP56303. The following figure highlights the new bits.

DSP56303 OMR

SCS								EOM								COM							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			SEN	WRP	EOV	EUN	XYS	ATE			BRT	TAS	BE	CDP[1:0]		MS	SD		EBD	MD	MC	MB	MA

DSP56307 OMR

SCS								EOM								COM							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSW[1:0]		SEN	WRP	EOV	EUN	XYS	ATE	**APD**	**ABE**	BRT	TAS	BE	CDP[1:0]		MS	SD		EBD	MD	MC	MB	MA

MSW1-
MSW0 Memory Switch Configuration
SEN Stack Extension Enable
WRP Extended Stack Wrap Flag
EOV Extended Stack Overflow Flag
EUN Extended Stack Underflow Flag
XYS Stack Extension Space Select

ATE Address Tracing Enable
APD Address Attribute Disable
ABE Asyn. Bus Arbitration Enable
BRT Bus Release Timing
TAS $\overline{TA}$ Synchronize Select
BE Burst Mode Enable
CDP1 Core-DMA Priority 1
CDP0 Core-DMA Priority 0

MS Memory Switch Mode
SD Stop Delay
EBD External Bus Disable
MD Operating Mode D
MC Operating Mode C
MB Operating Mode B
MA Operating Mode A

Note: The differences are in bold.

Reserved bit; read as zero; should be written with zero for future compatibility

Figure 2. Differences Between the DSP56303 and DSP56307 Operating Mode Registers

The Memory Switch Configuration bits (MSW[1:0]), along with the CE and SC bits in the Status Register, allow you to set the DSP56307 memory map in as many as 20 different configurations. In comparison, the DSP56303 allows only eight possible configurations.

Bit 14 of the DSP56307 OMR is the Address Attribute (AA) Priority Disable bit, APD. This bit allows the priority assigned to the Address Attribute signals (AA0-AA3) to be disabled. When APD=0 (default setting), the four AA signals each have a certain priority: AA3 has the highest priority and AA0 has the lowest priority. Therefore, only one AA signal can be active at one time. Certain functions, such as using the AA signals as additional address lines, require additional interface hardware. When APD=1, the priority mechanism is disabled, allowing more than one AA signal to be active simultaneously.

When set, the Asynchronous Bus Arbitration Enable bit (ABE, bit 13) eliminates the setup and hold time requirements (with respect to CLKOUT) for $\overline{BB}$ and $\overline{BG}$. This bit substitutes a required non-overlap interval between the deassertion of one $\overline{BG}$ input to a DSP56300 family device and the assertion of a second $\overline{BG}$ input to a second DSP56300 family device on the same bus. When the ABE bit is set, the $\overline{BG}$ and $\overline{BB}$ inputs are synchronized. This synchronization causes a delay between a change in $\overline{BG}$ or $\overline{BB}$ until the receiving device actually accepts this change.

The additional bits on the DSP56307 are reserved on all revisions of the DSP56303 before Revision D. Nonetheless, you should ensure that bits 13, 14, 21, and 22 are not written in any DSP56303 code before Revision D, keeping in mind that bit 13, ABE, is available on Revision D of the DSP56303.

1.2.3 Memory Switches

The DSP56307 has a total of 64k x 24 words of on-chip RAM, whereas the DSP56303 has a total of 8k x 24 words. As shown in the OMR previously, the possible memory configurations on the DSP56307 differ from those on the DSP56303 (see **Table 5**).

Table 5. Memory Configurations Available on the DSP56307

Program RAM Size	Instruction Cache Size	X Data RAM Size*	Y Data RAM Size*	Instruction Cache	Switch Mode (MS)	MSW[1]	MSW[0]
16Kx24-bit	0	24Kx24-bit	24Kx24-bit	disabled	disabled	0/1	0/1
15Kx24-bit	1024x24-bit	24Kx24-bit	24Kx24-bit	enabled	disabled	0/1	0/1
48Kx24-bit	0	8Kx24-bit	8Kx24-bit	disabled	enabled	0	0
47Kx24-bit	1024x24-bit	8Kx24-bit	8Kx24-bit	enabled	enabled	0	0
40Kx24-bit	0	12Kx24-bit	12Kx24-bit	disabled	enabled	0	1
39Kx24-bit	1024x24-bit	12Kx24-bit	12Kx24-bit	enabled	enabled	0	1
32Kx24-bit	0	16Kx24-bit	16Kx24-bit	disabled	enabled	1	0
31Kx24-bit	1024x24-bit	16Kx24-bit	16Kx24-bit	enabled	enabled	1	0
24Kx24-bit	0	20Kx24-bit	20Kx24-bit	disabled	enabled	1	1
23Kx24-bit	1024x24-bit	20Kx24-bit	20Kx24-bit	enabled	enabled	1	1

* Includes 4Kx24-bit shared memory (i.e., shared by the core and the EFCOP and not accessible by the DMA controller)

Figure 3 shows the default configurations of the DSP56307 and DSP56303 memory maps. Because the DSP56307 has more on-chip RAM, DSP56303 code that accesses external memory may use a memory space that is now considered on-chip. The programmer should verify that this memory space difference has been considered. Also, the EFCOP shares the lower 4k of X and Y memory with the core. This means that DMA can no longer access this area of memory. This restriction is made for design reasons and to avoid contention between the EFCOP and DMA accesses. If previous DSP56303 code accessed this area of memory for other software purposes using DMA, the data must be moved to higher sections in memory where DMA does not contend with the EFCOP, or it can be accessed in the lower area of memory using the core. For details on the DSP56307 and DSP56303 memory maps, refer to the respective user's manuals.

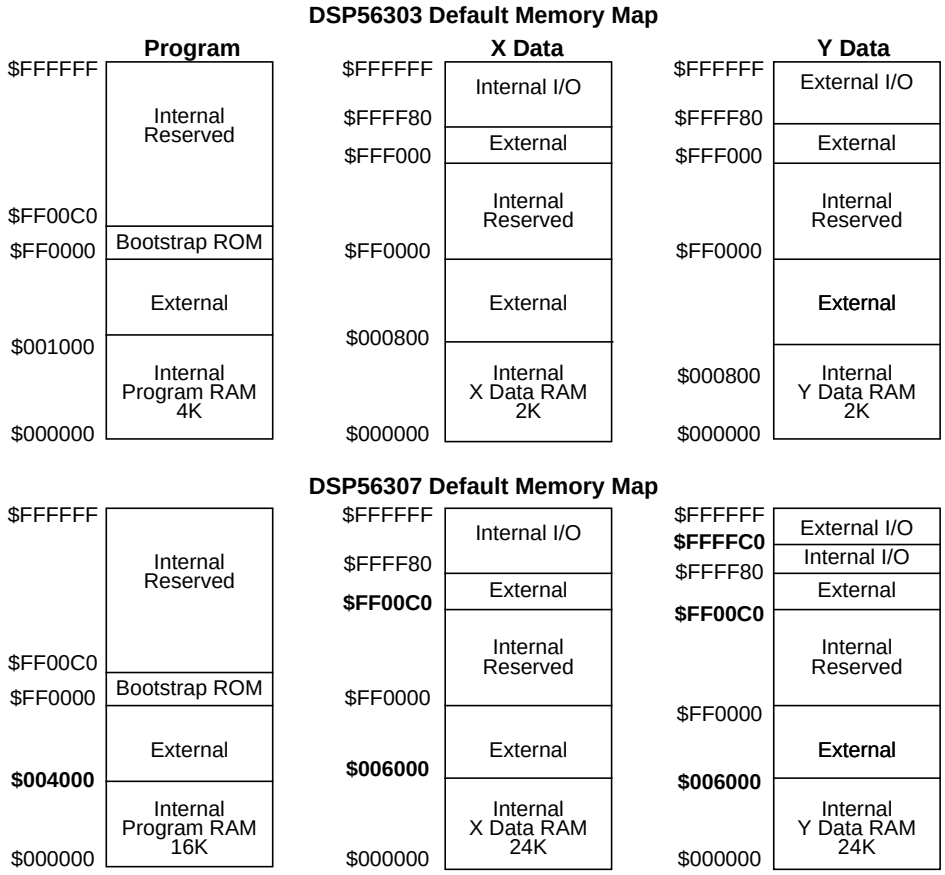

Figure 3. Comparison of Default DSP56303 and DSP56307 Memory Maps

1.2.4 Bootstrap and Operating Modes

The DSP56307 operating modes have been updated from the DSP56303 modes. **Table 6** details these differences. Bootstrap ROM resides at the same location ($FF0000 to $FF00BF) in both devices.

Table 6. Comparison of DSP56303 and DSP56307 Operating Modes

Mode	MODD	MODC	MODB	MODA	Reset Vector	DSP56303 Description	DSP56307 Description
0	0	0	0	0	$C00000	Expanded mode	Expanded mode
1	0	0	0	1	$FF0000	Bootstrap from byte-wide memory (at $D00000)	**Reserved**
2	0	0	1	0	$FF0000	Bootstrap through SCI	**Reserved**
3	0	0	1	1	$**FF0000**	Reserved	Reserved
4	0	1	0	0	$FF0000	HI08 Bootstrap in ISA/DSP5630X mode	**Reserved**
5	0	1	0	1	$FF0000	HI08 Bootstrap in HC11 non-multiplexed mode	**Reserved**
6	0	1	1	0	$FF0000	HI08 Bootstrap in 8051 multiplexed bus mode	**Reserved**

Table 6. Comparison of DSP56303 and DSP56307 Operating Modes (Continued)

Mode	MODD	MODC	MODB	MODA	Reset Vector	DSP56303 Description	DSP56307 Description
6	0	1	1	0	$FF0000	HI08 Bootstrap in 8051 multiplexed bus mode	**Reserved**
7	0	1	1	1	$FF0000	HI08 Bootstrap in 68302 bus mode	**Reserved**
8	1	0	0	0	$008000	Expanded mode	Expanded mode
9	1	0	0	1	$FF0000	Bootstrap from byte-wide memory (at $D00000)	Bootstrap from byte-wide memory (at $D00000)
A	1	0	1	0	$FF0000	Bootstrap through SCI	Bootstrap through SCI
B	1	0	1	1	**$FF0000**	Reserved	Reserved
C	1	1	0	0	$FF0000	HI08 Bootstrap in ISA/DSP5630X mode	HI08 Bootstrap in ISA/DSP5630X mode
D	1	1	0	1	$FF0000	HI08 Bootstrap in HC11 non-multiplexed mode	HI08 Bootstrap in HC11 non-multiplexed mode
E	1	1	1	0	$FF0000	HI08 Bootstrap in 8051 multiplexed bus mode	HI08 Bootstrap in 8051 multiplexed bus mode
F	1	1	1	1	$FF0000	HI08 Bootstrap in 68302 bus mode	HI08 Bootstrap in 68302 bus mode

Bold items highlight where the two devices differ in their operating modes definitions.
In the DSP56303, the reset vector for modes 3 and B is not defined.

2 Enhancements

In addition to required changes, there are some optional enhancements to the DSP56307, which pertain to the Enhanced Filter Coprocessor (EFCOP). This completely new coprocessor in the DSP56300 family resides on the DSP56307. It is a peripheral module that functions as a general-purpose, fully programmable complex filter. It has optimized modes of operation to perform complex finite impulse response (FIR) filtering, infinite impulse response (IIR) filtering, adaptive FIR filtering, and multichannel FIR filtering. The EFCOP allows filter operations to complete concurrently with DSP56300 core operations, with minimal CPU intervention. This coprocessor affects the memory-mapped registers, DMA access to internal memory, DMA request sources, and interrupt request sources. See application note APR39, titled, *Programming the ESP56307 Enhanced Filter Coprocessor (EFCOP)*, for more information. The changes are as follows:

- Memory-Mapped Registers — The EFCOP has nine memory-mapped registers that are mapped to the internal Y I/O memory space from address $FFFFB0 to $FFFFB8. Only EFCOP registers reside in Y I/O memory. All other memory-mapped registers reside in internal X I/O memory space and remain unchanged from the DSP56303.
- DMA Access — Because the EFCOP has direct access to internal memory below $001000, DMA can not access this area of memory. This is done in order to avoid contention and for design purposes. Any DMA access to addresses in X and Y memory from $000000 to $000FFF results in nothing being transferred. If previous DSP56303 code accessed this area of memory using DMA, you must ensure that the data is moved to a higher location in memory

or that the access is changed to a core access. The EFCOP Filter Control Status Register (FCSR) includes a Filter Contention (FCONT) sticky bit that notifies the user of any contention between the EFCOP and the core.

- DMA Request Sources — Two new DMA request sources originate from the EFCOP. One is a request when the EFCOP input buffer is empty. To use this request, set the DRS[4:0] bits equal to 10101. The second request occurs when the EFCOP output buffer is full. To use this request, set the DRS[4:0] bits equal to 10110. No other DMA request sources are affected.
- Interrupt Request Sources — Two new interrupt sources are available on the DSP56307. They are similar to the DMA request sources. One is an EFCOP data input buffer empty request, and the other is an EFCOP data output buffer full request. Their vector base addresses are at $68 and $6A, respectively. The EFCOP interrupt sources have the lowest priority within an IPL. Two bits are added to the Interrupt Priority Register P (IPRP) for setting the EFCOP IPL. They are bits 10 and 11.

Appendix: Related Documents

For details on the DSP56303 and the DSP56307, refer to the following documents, which you can order from your Motorola Literature Distribution Center using the reference numbers shown:

- DSP56300 Family Manual - DSP56300FM/AD
- DSP56303 Technical Data Sheet - DSP56303/D
- DSP56303 User’s Manual - DSP56303UM/AD
- DSP56307 Technical Data Sheet - DSP56307/D
- DSP56307 User’s Manual - DSP56307UM/D
- APR39, *Programming the DSP56307 Enhanced Filter Coprocessor (EFCOP)*
- You can download these documents from the Web at the following URL:

  `http://www.mot.com/SPS/DSP`

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