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Hardware Differences Between the DSP56002 and the DSP56303

by Barbara Johnson

The hardware differences between the DSP56002 and the DSP56303 must be considered when a system based on the DSP56002 is redesigned to use the DSP56303. This application note describes these hardware differences in detail. The DSP56300 is a rich product family, and, where applicable, this document also addresses changes that enable DSP56303 designs to migrate easily to other DSP56300 devices.

This application note does not describe an application *per se*. Rather it summarizes the hardware differences between two DSP products as a convenient reference for designers and programmers who are migrating to the DSP56303 from the DSP56002. It saves you the time that would be required to review the documentation and determine what these differences are.

For details on the software differences between the DSP56002 and DSP56303, refer to the application note AN1829/D, *Software Differences Between the DSP56002 and the DSP56303*, which covers the differences in the instruction pipeline, the instruction cache controller, and the instruction set. It also covers differences in various core modules—such as the arithmetic logic unit and address generation unit—and differences in the programming model.

Contents

1 Hardware Layout

The DSP56002 is available in the following package types:

- 144-pin plastic quad flat pack (PQFP)
- 144-pin thin quad flat pack (TQFP)

The DSP56303 is available in the following package types:

- 144-pin thin quad flat pack (TQFP)
- 196-pin plastic ball grid array (PBGA)

The 196-pin PBGA is strongly recommended for new DSP56303 designs. It is signal-pin compatible with future, higher-performance members of the DSP56300 family.

DSP56002-based designs require at least four 0.1µF bypass capacitors positioned as closely as possible to the four sides of the package to connect the V_{CC} power source to GND. Refer to **Table 4**, *Differences Between the PLL of the DSP56002 and DSP56303*, on page 8 for the PLL capacitor value.
DSP56303-based designs require at least six 0.01-0.1uF bypass capacitors positioned as closely as possible to the four sides of the package to connect the V_{CC} power source to GND. Refer to **Table 4**, *Differences Between the PLL of the DSP56002 and DSP56303*, on page 8 for the PLL capacitor value.

The physical pinout of the DSP56002 differs from that of the DSP56303, so a direct replacement of the DSP is not possible. The board layout must be changed to reflect the differences in pinout. **Table 1** shows the signal names and pin numbers of the TQFP package, and **Table 2** shows the signal names and pin numbers of the PBGA package.

Table 1. DSP56002 and DSP56303 TQFP Pinout

Pin No.	DSP56002 Signal Name	DSP56303 Signal Name	Pin No.	DSP56002 Signal Name	DSP56303 Signal Name	Pin No.	DSP56002 Signal Name	DSP56303 Signal Name
1	Not Connected (NC), reserved	SRD1/PD4	49	SC0/PC3	NC, reserved	97	A8	A15
2	D22	STD1/PD5	50	V_{CCS}	AA3/$\overline{RAS3}$	98	A9	A16
3	D23	SC02/PC2	51	SCK/PC6	AA2/$\overline{RAS2}$	99	GND_A	A17
4	MODC/$\overline{NMI}$	SC01/PC1	52	SC2/PC5	CAS	100	A10	D0
5	MODB/$\overline{IRQB}$	DE	53	STD/PC8	XTAL	101	A11	D1
6	MODA/$\overline{IRQA}$	PINIT/$\overline{NMI}$	54	GND_S	GND_Q	102	A12	D2
7	GND_{CK}	SRD0/PC4	55	NC, reserved	EXTAL	103	V_{CCA}	V_{CCD}
8	CKOUT	V_{CCS}	56	SC1/PC4	V_{CCQ}	104	A13	GND_D
9	V_{CCCK}	GND_S	57	GND_Q	V_{CCC}	105	GND_A	D3
10	RESET	STD0/PC5	58	V_{CCQ}	GND_C	106	A14	D4
11	CKP	SC10/PD0	59	SRD/PC7	CLKOUT	107	A15	D5

Table 1. DSP56002 and DSP56303 TQFP Pinout (Continued)

Pin No.	DSP56002 Signal Name	DSP56303 Signal Name	Pin No.	DSP56002 Signal Name	DSP56303 Signal Name	Pin No.	DSP56002 Signal Name	DSP56303 Signal Name
12	V_{CCP}	SC00/PC0	60	TIO	BCLK	108	NC, reserved	D6
13	PCAP	RXD/PE2	61	NC, reserved	BCLK	109	NC, reserved	D7
14	GND_P	TXD/PE1	62	BN	TA	110	D0	D8
15	PLOCK	SCLK/PE2	63	WT	BR	111	D1	V_{CCD}
16	PINIT	SCK1/PD3	64	BG	BB	112	GND_D	GND_D
17	XTAL	SCK0/PC3	65	BR	V_{CCC}	113	D2	D9
18	NC, reserved	V_{CCQ}	66	V_{CCC}	GND_C	114	D3	D10
19	EXTAL	GND_Q	67	WR	WR	115	V_{CCD}	D11
20	V_{CCQ}	NC, reserved	68	RD	RD	116	D4	D12
21	GND_Q	$\overline{HDS}$/HDS, $\overline{HWR}$/HWR, PB12	69	GND_C	AA1/$\overline{RAS1}$	117	D5	D13
22	HA2/PB10	HRW, $\overline{HRD}$/HRD, PB11	70	NC, reserved	AA0/$\overline{RAS0}$	118	GND_D	D14
23	GND_H	$\overline{HACK}$/HACK, $\overline{HRRQ}$/HRRQ, PB15	71	DSCK/OS1	BG	119	D6	V_{CCD}
24	HA1/PB9	$\overline{HREQ}$/HREQ, $\overline{HTRQ}$/HTRQ, PB14	72	NC, reserved	A0	120	D7	GND_D
25	HA0/PB8	V_{CCS}	73	NC, reserved	A1	121	D8	D15
26	$\overline{HACK}$/PB14	GND_S	74	DR	V_{CCA}	122	D9	D16
27	V_{CCH}	TIO2	75	DSO	GND_A	123	V_{CCQ}	D17
28	$\overline{HEN}$/PB12	TIO1	76	DSI/OS0	A2	124	GND_Q	D18
29	GND_H	TIO0	77	BS	A3	125	GND_D	D19
30	HR/$\overline{W}$/PB11	$\overline{HCS}$/HCS, HA10, PB13	78	X/$\overline{Y}$	A4	126	D10	V_{CCQ}
31	$\overline{HREQ}$/PB13	HA2, HA9, PB10	79	GND_A	A5	127	NC, reserved	GND_Q
32	H7/PB7	HA1, HA8, PB9	80	DS	V_{CCA}	128	D11	D20

Table 1. DSP56002 and DSP56303 TQFP Pinout (Continued)

Pin No.	DSP56002 Signal Name	DSP56303 Signal Name	Pin No.	DSP56002 Signal Name	DSP56303 Signal Name	Pin No.	DSP56002 Signal Name	DSP56303 Signal Name
33	H6/PB6	HA0, $\overline{\text{HAS}}$/HAS, PB8	81	V_{CCA}	GND_A	129	V_{CCD}	V_{CCD}
34	GND_H	H7, HAD7, PB7	82	PS	A6	130	D12	GND_D
35	H5/PB5	H6, HAD6, PB6	83	A0	A7	131	D13	D21
36	NC	H5, HAD5, PB5	84	A1	A8	132	GND_D	D22
37	NC, reserved	H4, HAD4, PB4	85	GND_A	A9	133	D14	D23
38	H4/PB4	V_{CCH}	86	A2	V_{CCA}	134	D15	MODD/ $\overline{\text{IRQD}}$
39	H3/PB3	GND_H	87	A3	GND_A	135	D16	MODC/ $\overline{\text{IRQC}}$
40	V_{CCH}	H3, HAD3, PB3	88	A4	A10	136	D17	MODB/ $\overline{\text{IRQB}}$
41	H2/PB2	H2, HAD2, PB2	89	GND_S	A11	137	GND_D	MODA/ $\overline{\text{IRQA}}$
42	GND_H	H1, HAD1, PB1	90	GND_Q	GND_Q	138	D18	TRST
43	H1/PB1	H0, HAD0, PB0	91	NC, reserved	V_{CCQ}	139	D19	TDO
44	H0/PB0	RESET	92	A5	A12	140	V_{CCD}	TDI
45	RXD/PC0	V_{CCP}	93	V_{CCA}	A13	141	D20	TCK
46	TXD/PC1	PCAP	94	GND_A	A14	142	D21	TMS
47	GND_S	GND_P	95	A6	V_{CCA}	143	GND_D	SC12/PD2
48	SCLK/PC2	GND_{P1}	96	A7	GND_A	144	NC, reserved	SC11/PD1

Table 2. DSP56303 PBGA Pinout

Pin No.	DSP56303 Signal Name	Pin No.	DSP56303 Signal Name	Pin No.	DSP56303 Signal Name	Pin No.	DSP56303 Signal Name
A1	NC, reserved	D8	GND	H1	NC, reserved	L8	GND
A2	SC11/PD1	D9	GND	H2	V_{CCQ}	L9	GND
A3	TMS	D10	GND	H3	SCK0/PC3	L10	GND
A4	TDO	D11	GND	H4	GND	L11	GND
A5	MODB/IRQB	D12	D1	H5	GND	L12	V_{CCA}
A6	D23	D13	D2	H6	GND	L13	A3
A7	V_{CCD}	D14	V_{CCD}	H7	GND	L14	A4
A8	D19	E1	STD0/PC5	H8	GND	M1	HA1, HA8, PB9
A9	D16	E2	V_{CCS}	H9	GND	M2	HA2, HA9, PB10
A10	D14	E3	SRD0/PC4	H10	GND	M3	HA0, $\overline{\text{HAS}}$/HAS, PB8
A11	D11	E4	GND	H11	GND	M4	V_{CCH}
A12	D9	E5	GND	H12	V_{CCA}	M5	H0, HAD0, PB0
A13	D7	E6	GND	H13	A10	M6	V_{CCP}
A14	NC, reserved	E7	GND	H14	A11	M7	NC, reserved
B1	SRD1/PD4	E8	GND	J1	$\overline{\text{HACK}}$/HACK, $\overline{\text{HRRQ}}$/HRRQ, PB15	M8	EXTAL
B2	SC12/PD2	E9	GND	J2	HRW, $\overline{\text{HRD}}$/HRD, PB11	M9	CLKOUT
B3	TDI	E10	GND	J3	$\overline{\text{HDS}}$/HDS, $\overline{\text{HWR}}$/HWR, PB12	M10	BCLK
B4	TRST	E11	GND	J4	GND	M11	WR
B5	MODD/$\overline{\text{IRQD}}$	E12	A17	J5	GND	M12	RD
B6	D21	E13	A16	J6	GND	M13	A1
B7	D20	E14	D0	J7	GND	M14	A2
B8	D17	F1	RXD/PE0	J8	GND	N1	H6, HAD6, PB6
B9	D15	F2	SC10/PD0	J9	GND	N2	H7, HAD7, PB7

Table 2. DSP56303 PBGA Pinout (Continued)

Pin No.	DSP56303 Signal Name	Pin No.	DSP56303 Signal Name	Pin No.	DSP56303 Signal Name	Pin No.	DSP56303 Signal Name
B10	D13	F3	SC00/PC0	J10	GND	N3	H4, HAD4, PB4
B11	D10	F4	GND	J11	GND	N4	H2, HAD2, PB2
B12	D8	F5	GND	J12	A8	N5	RESET
B13	D5	F6	GND	J13	A7	N6	GND_P
B14	NC, reserved	F7	GND	J14	A9	N7	AA3/$\overline{RAS3}$
C1	SC02/PC2	F8	GND	K1	V_{CCS}	N8	CAS
C2	STD1/PD5	F9	GND	K2	$\overline{HREQ}$/HREQ, $\overline{HTRQ}$/HTRQ, PB14	N9	V_{CCQ}
C3	TCK	F10	GND	K3	TIO2	N10	BCLK
C4	MODA/$\overline{IRQA}$	F11	GND	K4	GND	N11	BR
C5	MODB/$\overline{IRQB}$	F12	V_{CCA}	K5	GND	N12	V_{CCC}
C6	D22	F13	A14	K6	GND	N13	AA0/$\overline{RAS0}$
C7	V_{CCQ}	F14	A15	K7	GND	N14	A0
C8	D18	G1	SCK1/PD3	K8	GND	P1	NC, reserved
C9	V_{CCD}	G2	SCLK/PE2	K9	GND	P2	H5, HAD5, PB5
C10	D12	G3	TXD/PE1	K10	GND	P3	H3, HAD3, PB3
C11	V_{CCD}	G4	GND	K11	GND	P4	H1, HAD1, PB1
C12	D6	G5	GND	K12	V_{CCA}	P5	PCAP
C13	D3	G6	GND	K13	A5	P6	GND_{P1}
C14	D4	G7	GND	K14	A6	P7	AA2/$\overline{RAS2}$
D1	PINIT/$\overline{NMI}$	G8	GND	L1	$\overline{HCS}$/HCS, HA10, PB13	P8	XTAL
D2	SC01/PC1	G9	GND	L2	TIO1	P9	V_{CCC}
D3	DE	G10	GND	L3	TIO0	P10	TA
D4	GND	G11	GND	L4	GND	P11	BB
D5	GND	G12	A13	L5	GND	P12	AA1/$\overline{RAS1}$
D6	GND	G13	V_{CCQ}	L6	GND	P13	BG
D7	GND	G14	A12	L7	GND	P14	NC, reserved

2 Core

The DSP56300 core can execute an instruction on every clock cycle, thus yielding a twofold performance increase (at the same clock rate) as compared to the DSP56000 core, while maintaining object code compatibility. For example, a DSP56002 running at 40 MHz can deliver 20 million instructions per second (MIPS), while a DSP56303 running at 40 MHz can deliver 40 MIPS. In addition to the performance increase inherent in the "1X" architecture of the DSP56300 core, devices in this family can operate at much greater clock rates than those of the DSP56000 family devices. This section compares the core characteristics of the DSP56002 and the DSP5603 in terms of power supply, electrical characteristics, phase locked-loop (PLL), DMA controller, memory, instruction cache, and other core features.

2.1 Power Supply

The DSP56002 requires a supply voltage (V_{CC}) of 5V. The DSP56303 requires a V_{CC} of 3.3V. For easier migration to DSP56300 derivatives using Motorola's High-Performance (HiP4) process technology, a split power supply design for the core and I/Os is recommended. For example, the DSP56311 uses split power supplies to separate the I/O and peripheral sections, which operate at 3.3V, from the processor core, which runs at 1.8V.

2.2 Electrical Characteristics

Table 3 shows the differences in electrical characteristics between the DSP56002 and the DSP56303.

Table 3. DSP56002 and DSP56303 Electrical Characteristics

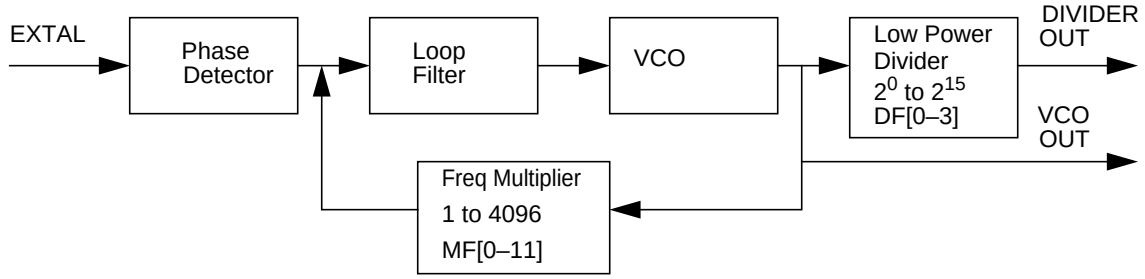
Characteristics	DSP56002		DSP56303	
	MIN	MAX	MIN	MAX
Input High Voltage	4.0V (Note 1) 2.5V (Note 2) 3.5V (Note 3) 2.0V (Note 4)	V_{CC} V_{CC} V_{CC} V_{CC}	2.0V (Note 5) 2.0V (Note 6) $0.8V_{CC}$ (Note 1)	V_{CC} V_{CC}+3.95V V_{CC}
Input Low Voltage	-0.5V -0.5V -0.5V	0.6V (Note 1) 2.0V (Note 3) 0.8V (Note 4)	-0.3V -0.3V -0.3V	0.8V (Note 7) 0.8V (Note 8) $0.2V_{CC}$ (Note 1)
Output High Voltage	2.4V	--	V_{CC}-0.4V (TTL) V_{CC}-0.01V (CMOS)	--
Output Low Voltage	--	0.4V	--	0.4V (TTL) 0.01V (CMOS)

NOTES: 1. EXTAL
2. RESET
3. MODA/MODB/MODC
4. All other inputs
5. D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$
6. MOD/$\overline{IRQ}$, $\overline{RESET}$, PINIT/$\overline{NMI}$, JTAG, ESSI, SCI, Timer, HI08
7. D[0–23], BG, BB, TA, MOD/$\overline{IRQ}$, $\overline{RESET}$, PINIT/$\overline{NMI}$
8. JTAG, ESSI, SCI, Timer, HI08

2.3 Phase-Locked Loop (PLL)

There are several key differences in the PLL of the DSP56002 and the DSP56303. To help you understand these differences, **Figure 1** shows the DSP56002 and DSP56300 PLL block diagrams. **Table 4** compares the different PLL elements shown in the block diagrams.

DSP56002 PLL Block Diagram



DSP56303 PLL Block Diagram

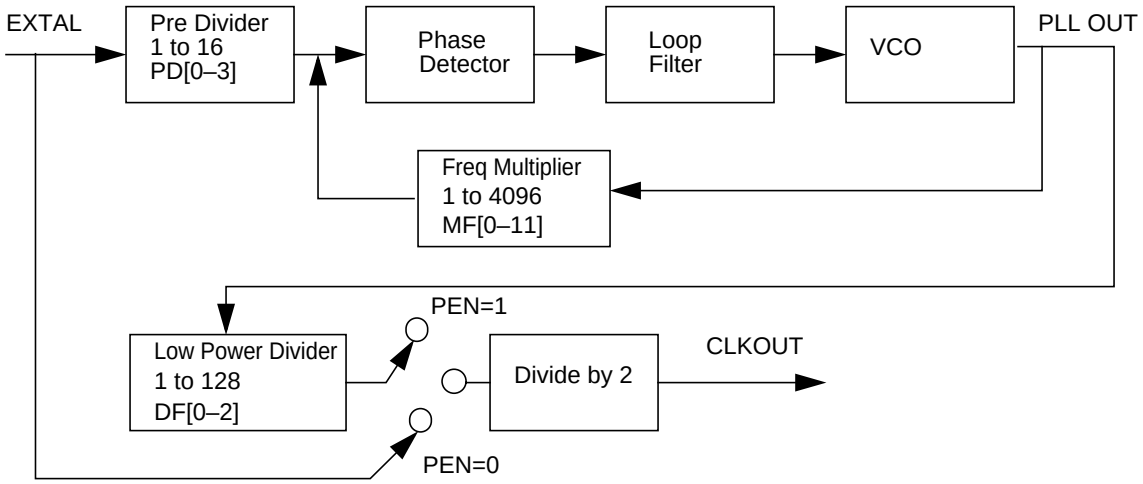


Figure 1. PLL Block Diagrams

Table 4. Differences Between the PLL of the DSP56002 and DSP56303

DSP56002	DSP56303
Frequency Pre-divider Not Available	A **frequency pre-divider** is available on the DSP56303. This programmable division factor applies to the PLL input frequency and ranges from 1 to 16. The pre-divider factor bits PD[0–3] are written into bits 20–23 of the PLL Control Register (PCTL).
Fixed Divide by 2 Not Available	In the DSP56300 core, the output of the voltage-controlled oscillator (VCO) is **divided by 2**. This results in a constant x2 multiplication of the PLL clock output that generates the special chip clock phases.

Table 4. Differences Between the PLL of the DSP56002 and DSP56303

DSP56002	DSP56303
The **low power divider** divides the output frequency of the VCO by any power of 2 from 2^0 to 2^{15}. The division factor bits DF[0–3] are written into bits 12–15 of the PCTL.	The clock generator performs the low power division. The **low power divider** divides the output frequency of the PLL by any power of 2 from 2^0 to 2^7. The division factor bits DF[0–2] are written into PCTL bits 12–14.
The **operating frequency** is governed by the frequency control bits in the PCTL as follows: $F_{002} = F_{EXT}$ x MF / DF = F_{VCO} / DF When the PLL is disabled, the internal chip clock and CKOUT are driven from the EXTAL input.	The **operating frequency** is governed by the frequency control bits in the PCTL, as follows: $F_{303} = F_{EXT}$ x MF / (PDF x DF) = F_{VCO} / DF where: F_{CHIP} is the chip operating frequency. F_{EXT} is the external input frequency to the chip at the EXTAL pin. MF is the multiplication factor defined by the MF[0–11] bits. DF is the division factor defined by the DF[0–3] bits. PDF is the pre-division factor defined by the PD[0–3] bits. F_{VCO} is the output frequency of the VCO. When the PLL is disabled, the frequency of the CLKOUT is half the EXTAL input.
PLL Filter Capacitor The recommended PCAP value is 400 pF for a multiplication factor of MF <= 4 and 540 pF for a multiplication factor of MF > 4. For example, if a 40 MHz crystal is used and the desired operating frequency is 40 MHz, the MF factor is: $F_{002} = F_{EXT}$ x MF / DF = 40 MHz = 40 MHz * MF MF is 1. The PCAP value should be 400 pF, since MF <= 1.	**PLL Filter Capacitor** The recommended PCAP value is (500*MF-150) pF for a multiplication factor of MF <= 4 and (690*MF) pF for a multiplication factor of MF > 4. For example, if a 16.9344 MHz crystal is used and the desired operating frequency is 68 MHz, the MF factor is: $F_{303} = F_{EXT}$ * MF / (PDF * DF) = 68 MHz = 16.9344 MHz * MF MF is approximately 4. The PCAP value should be (500 * 4 - 150) pF = 1850 pF, since MF <= 4.
PLL Pins The Phase and Frequency Lock (PLOCK) pin is asserted when the PLL is enabled and has locked on the proper phase and frequency of EXTAL. The Clock Output Polarity Control (CKP) pin is an input that defines the polarity of the CKOUT clock output.	**PLL Pins** **PLOCK and CKP pins Not available**

Figure 2 and **Figure 3** show the recommended connection and component values for the DSP56002 and DSP56303, respectively, if the system clock derives from the on-chip crystal oscillator.

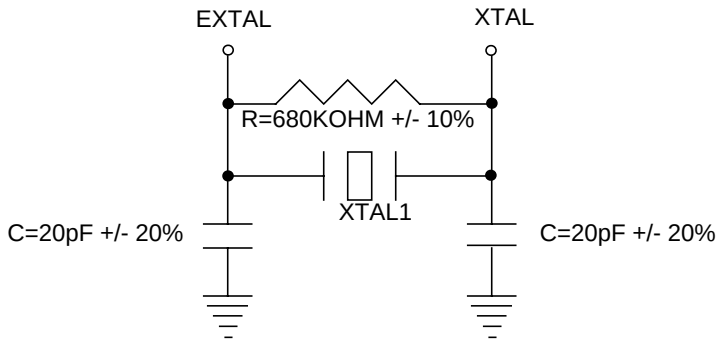


Figure 2. DSP56002 Fundamental Frequency Crystal Oscillator Circuit

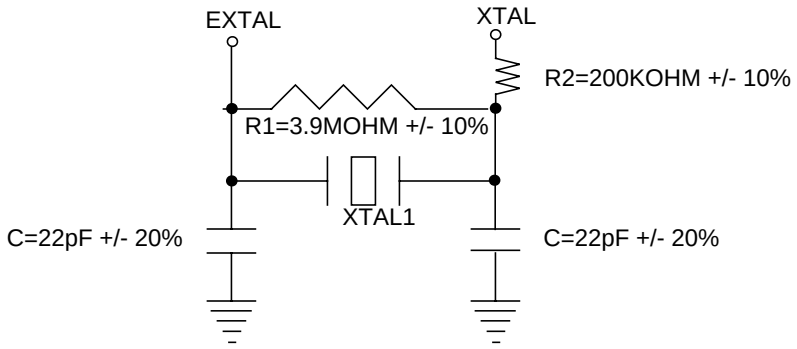


Figure 3. DSP56303 Fundamental Frequency Crystal Oscillator Circuit

2.4 DMA Controller

A key difference between the DSP56002 and the DSP56303 is that a DMA controller is available on the DSP56300 core. The DMA permits data transfers between internal/external memory and/or internal/external I/O independently of core operation. The DMA controller has six channels, each with its own register set. Data transfer for one channel requires a minimum of two clock cycles per single word. **Table 5** shows the various types of DMA data transfers available.

Table 5. DSP56300 DMA Controller Data Transfers

Source	Destination	Clock Cycles per Single Word Transfer
Internal Memory	Internal Memory	2
Internal Memory	External Memory	2 + wait states
Internal Memory	Internal I/O	2
External Memory	Internal Memory	2 + wait states

Table 5. DSP56300 DMA Controller Data Transfers (Continued)

Source	Destination	Clock Cycles per Single Word Transfer
External Memory	External Memory	2 + wait states
External Memory	Internal I/O	2 + wait states
Internal I/O	Internal Memory	2
Internal I/O	External Memory	2 + wait states
Internal I/O	Internal I/O	2

The DMA supports various types of address generation schemes, such as:

- Constant addressing:
  The address remains unchanged throughout the data transfer.
- Uni-dimensional addressing:
  One block is transferred using consecutive addresses.
- Two-dimensional addressing:
  Equally-spaced blocks are transferred using consecutive addresses within each block. The spacing between the blocks is programmed into an offset register.
- Three-dimensional addressing:
  Equally-spaced groups of equally-spaced blocks are transferred using consecutive addresses within each block. The two spacings are programmed into two offset registers.

2.5 Memory

Table 6 compares the on-chip memory for the DSP56002 and the DSP56303. In DSP56300 derivatives using the HiP4 process technology, the internal memory block size is 1024 x 24-bit words compared to 256 x 24-bit words in Motorola's Communication Design Rules (CDR) process technology derivatives.

Table 6. On-Chip Memory

DSP56002 (words)			DSP56303 (words)					
P RAM	**X RAM**	**Y RAM**	**I-Cache On/Off**	**Switch Mode**	**P RAM**	**X RAM**	**Y RAM**	**I-Cache**
512	256	256	Off	Off	4 K	2 K	2 K	0
			On	Off	3 K	2 K	2 K	1 K
			Off	On	2 K	3 K	3 K	0
			Off	Off	1 K	3 K	3 K	1 K
P ROM	X ROM	Y ROM	P ROM	X ROM	Y ROM			
64	256	256	192	--	--			

The DSP56002 PROM contains the bootstrap program, and the XROM and YROM contain sine, A-law, and mu-law tables. In contrast, the DSP56303 PROM contains the bootstrap program; XROM or YROM contain no data. You can program the DSP56303 PRAM, XRAM, YRAM, and instruction cache sizes by changing the values of the following bits:

- Cache Enable (CE) bit in the Status Register (SR): When the instruction cache is enabled, the lowest 1K of program words are allocated to the instruction cache.
- Memory Switch (MS) bit in the Operating Mode Register (OMR): When the memory switch mode is set, XRAM and YRAM can be reallocated as PRAM.

Table 7 shows the off-chip memory expansion for each device.

Table 7. Off-Chip Memory Expansion

Memory Space	DSP56002 (words)	DSP56303 (words)
PRAM	64 K	16 M in 24-bit mode or 64 K in 16-bit mode
XRAM	64 K	16 M in 24-bit mode or 64 K in 16-bit mode
YRAM	64 K	16 M in 24-bit mode or 64 K in 16-bit mode

2.6 Instruction Cache Controller

An instruction cache controller is present on the DSP56300 core but not on the DSP5600 core. This cache acts as buffer memory between the main memory and the CPU, storing instruction sequences that execute frequently. An increase in throughput results when instruction words that a program needs are available in the on-chip cache, eliminating the time required to access them on the external bus.

2.7 Address Space Selection

Address space is selected differently on the DSP56002 than on the DSP56303. In the DSP56002, the Program Memory Select ($\overline{PS}$) signal is a program memory chip select signal that enables the program memory. The Data Memory Select ($\overline{DS}$) signal enables two data memories, and the X/$\overline{Y}$ Select (X/Y) signal selects X or Y data memory space. The three external memory spaces (program, X data, and Y data) do not have to reside in separate physical memories. A single memory suffices if the $\overline{PS}$, $\overline{DS}$, and X/$\overline{Y}$ signals are used as additional address lines to segment the memory into three spaces. **Table 8** shows how these signals are decoded.

Table 8. DSP56002 Program and Data Memory Select Encoding

PS	DS	X/$\overline{Y}$	External Memory References
1	1	1	No Activity
1	0	1	X Data Memory on Data Bus
1	0	0	Y Data Memory on Data Bus
0	1	1	Program Memory on Data Bus

In the DSP56303, the Address Attribute AA[3–0] signals can function as chip selects or as additional address lines. By default, only one AA signal can be asserted at a time. However, when the OMR AA Priority Disable (APD) bit is set, the AA lines are used together as four external lines externally decoded into 16 chip select signals. The AA pin is asserted if the address in the appropriate Address Attribute Register AAR[3–0] matches the external address and if the external access is aimed to a space that is enabled in the appropriate AAR register.[1]

3 Mode Control and Interrupts

This section compares how the DSP56002 and DSP56303 operating modes are controlled. It also compares the ways that interrupts are addressed, sourced, and prioritized.

3.1 Operating Modes

When the DSP56002 leaves the reset state, it samples the mode MOD[C–A] signal lines and loads their values into the MC, MB, and MA bits in the OMR to set the initial operating mode. **Table 9** shows the DSP56002 operating modes.

Table 9. DSP56002 Operating Modes

Operating Mode	MC	MB	MA	Description
0	0	0	0	Single-Chip mode
1	0	0	1	Bootstrap from EPROM
2	0	1	0	Normal Expanded mode
3	0	1	1	Development mode
5	1	0	1	Bootstrap from host
6	1	1	0	Bootstrap from SCI

When the DSP56303 leaves the reset state, it samples the mode MOD[D–A] signal lines and loads their values into the MD, MC, MB, and MA bits in the OMR to set the initial operating mode. **Table 10** shows the DSP56303 operating modes. For a complete description of the various modes, refer to the *DSP56303 User's Manual*.

Table 10. DSP56303 Operating Modes

Operating Mode	MD	MC	MB	MA	Description
0	0	0	0	0	Expanded mode
1	0 or 1	0	0	1	Bootstrap from byte-wide memory
2	0 or 1	0	1	0	Bootstrap from SCI
4	0 or 1	1	0	0	HI08 bootstrap in ISA/DSP5630x

1. Specified by the Address to Compare BAC[11–0] bits and the Number of Address Bits to Compare BNC[3–0].

Table 10. DSP56303 Operating Modes

Operating Mode	MD	MC	MB	MA	Description
5	0 or 1	1	0	1	HI08 bootstrap in HC11 non-multiplexed
6	0 or 1	1	1	0	HI08 bootstrap in 8051 multiplexed Bus
7	0 or 1	1	1	1	HI08 bootstrap in 68302 bus
8	1	0	0	0	Expanded mode

3.2 Interrupt Addresses and Sources

The Vector Base Address (VBA) register is available on the DSP56300 core and not on the DSP5600 core. The VBA is a 24-bit read/write register used as a base address of the interrupt vector and interrupt vector+1. Bits 7–0 are read-only and are always cleared. The VBA is referenced implicitly by interrupt processing or directly via the MOVEC instruction. **Table 11** shows the interrupt starting addresses and the interrupt priority level ranges for each interrupt source of both the DSP56002 (for which there is no VBA) and the DSP56303.

Table 11. Interrupt Starting Addresses and Sources

DSP56002			DSP56303		
Interrupt Starting Address	**Interrupt Priority Level Range**	**Interrupt Source**	**Interrupt Starting Address**	**Interrupt Priority Level Range**	**Interrupt Source**
$00	3	Hardware $\overline{\text{RESET}}$	VBA:$00	3	Hardware $\overline{\text{RESET}}$
$02	3	Stack Error	VBA:$02	3	Stack Error
$04	3	Trace	VBA:$04	3	Illegal Instruction
$06	3	SWI	VBA:$06	3	Debug Request Interrupt
$08	0–2	IRQA	VBA:$08	3	Trap
$0A	0–2	IRQB	VBA:$0A	3	Non–Maskable Interrupt $\overline{\text{NMI}}$
$0C	0–2	SSI Receive Data	VBA:$0C	3	Reserved
$0E	0–2	SSI Receive Data w/ Exception Status	VBA:$0E	3	Reserved
$10	0–2	SSI Transmit Data	VBA:$10	0–2	IRQA
$12	0–2	SSI Transmit Data w/ Exception Status	VBA:$12	0–2	IRQB
$14	0–2	SCI Receive Data	VBA:$14	0–2	IRQC
$16	0–2	SCI Receive Data w/ Exception Status	VBA:$16	0–2	IRQD
$18	0–2	SCI Transmit Data	VBA:$18	0–2	DMA Channel 0
$1A	0–2	SCI Idle Line	VBA:$1A	0–2	DMA Channel 1
$1C	0–2	SCI Timer	VBA:$1C	0–2	DMA Channel 2

Table 11. Interrupt Starting Addresses and Sources (Continued)

DSP56002			DSP56303		
Interrupt Starting Address	**Interrupt Priority Level Range**	**Interrupt Source**	**Interrupt Starting Address**	**Interrupt Priority Level Range**	**Interrupt Source**
$1E	3	Non-Maskable Interrupt $\overline{\text{NMI}}$	VBA:$1E	3	DMA Channel 3
$20	0–2	Host Receive Data	VBA:$20	0–2	DMA Channel 4
$22	0–2	Host Transmit Data	VBA:$22	0–2	DMA Channel 5
$24	0–2	Host Command	VBA:$24	0–2	TIMER 0 Compare
$26	0–2	Available for Host Command	VBA:$26	0–2	TIMER 0 Overflow
$28	0–2	Available for Host Command	VBA:$28	0–2	TIMER 1 Compare
$2A	0–2	Available for Host Command	VBA:$2A	0–2	TIMER 1 Overflow
$2C	0–2	Available for Host Command	VBA:$2C	0–2	TIMER 2 Compare
$2E	0–2	Available for Host Command	VBA:$2E	0–2	TIMER 2 Overflow
$30	0–2	Available for Host Command	VBA:$30	0–2	ESSI0 Receive Data
$32	0–2	Available for Host Command	VBA:$32	0–2	ESSI0 Receive Data w/ Exception Status
$34	0–2	Available for Host Command	VBA:$34	0–2	ESSI0 Receive Last Slot
$36	0–2	Available for Host Command	VBA:$36	0–2	ESSI0 Transmit Data
$38	0–2	Available for Host Command	VBA:$38	0–2	ESSI0 Transmit Data w/ Exception Status
$3A	0–2	Available for Host Command	VBA:$3A	0–2	ESSI0 Transmit Last Slot
$3C	0–2	Timer	VBA:$3C	0–2	Reserved
$3E	3	Illegal Instruction	VBA:$3E	0–2	Reserved
$40	0–2	Available for Host Command	VBA:$40	0–2	ESSI1 Receive Data
$42	0–2	Available for Host Command	VBA:$42	0–2	ESSI1 Receive Data w/ Exception Status
$44	0–2	Available for Host Command	VBA:$44	0–2	ESSI1 Receive Last Slot
$46	0–2	Available for Host Command	VBA:$46	0–2	ESSI1 Transmit Data

Table 11. Interrupt Starting Addresses and Sources (Continued)

DSP56002			DSP56303		
Interrupt Starting Address	**Interrupt Priority Level Range**	**Interrupt Source**	**Interrupt Starting Address**	**Interrupt Priority Level Range**	**Interrupt Source**
$48	0–2	Available for Host Command	VBA:$48	0–2	ESSI1 Transmit Data w/ Exception Status
$4A	0–2	Available for Host Command	VBA:$4A	0–2	ESSI1 Transmit Last Slot
$4C	0–2	Available for Host Command	VBA:$4C	0–2	Reserved
4E	0–2	Available for Host Command	VBA:4E	0–2	Reserved
$50	0–2	Available for Host Command	VBA:$50	0–2	SCI Receive Data
$52	0–2	Available for Host Command	VBA:$52	0–2	SCI Receive Data w/ Exception Status
$54	0–2	Available for Host Command	VBA:$54	0–2	SCI Transmit Data
$56	0–2	Available for Host Command	VBA:$56	0–2	SCI Idle Line
$58	0–2	Available for Host Command	VBA:$58	0–2	SCI Timer
$5A	0–2	Available for Host Command	VBA:$5A	0–2	Reserved
$5C	0–2	Available for Host Command	VBA:$5C	0–2	Reserved
$5E	0–2	Available for Host Command	VBA:$5E	0–2	Reserved
$60	0–2	Available for Host Command	VBA:$60	0–2	Host Receive Data Full
$62	0–2	Available for Host Command	VBA:$62	0–2	Host Transmit Data Empty
$64	0–2	Available for Host Command	VBA:$64	0–2	Host Command
$66	0–2	Available for Host Command	VBA:$66	0–2	Reserved
:	:	:	:	:	:
$7E	0–2	Available for Host Command	VBA:$7E	:	:
:			:	:	:
$FE			VBA:$FE	0–2	Reserved

3.3 Interrupt Priority Register

You can program interrupt priority levels for each on-chip peripheral device and for each external interrupt source under software control by writing to the interrupt priority register. Level 3 interrupts are non-maskable and have the highest priority; level 0 interrupts are maskable and have the lowest priority. **Table 12** shows the DSP56002 Interrupt Priority Register (IPR) configuration.

Table 12. DSP56002 Interrupt Priority Register

Bit No.	Bit Description	
23–18	Reserved	Read as zero
17–16	TIL[1–0]	Timer Interrupt Priority Level
15–14	SCL[1–0]	SCI Interrupt Priority Level
13–12	SSL[1–0]	SSI Interrupt Priority Level
11–10	HPL0	Host Interrupt Priority Level
9–6	Reserved	Read as zero
5–3	IBL[2–0]	$\overline{\text{IRQB}}$ Mode
2–0	IAL[2–0]	$\overline{\text{IRQA}}$ Mode

The DSP56303 has two interrupt priority registers. The IPR-C is dedicated to the DSP56300 core interrupt sources, and the IPR-P is dedicated to the DSP56303 peripherals. **Table 13** and **Table 14** show the bits of each interrupt priority register.

Table 13. DSP56303 Interrupt Priority Register C

Bit No.	Bit Name	
23–22	D5L[1–0]	DMA5 Interrupt Priority Level
21–20	D4L[1–0]	DMA4 Interrupt Priority Level
19–18	D3L[1–0]	DMA3 Interrupt Priority Level
17–16	D2L[1–0]	DMA2 Interrupt Priority Level
15–14	D1L[1–0]	DMA1 Interrupt Priority Level
13–12	D0L[1–0]	DMA0 Interrupt Priority Level
11–9	IDL[2–0]	$\overline{\text{IRQD}}$ Mode
8–6	ICL[2–0]	$\overline{\text{IRQC}}$ Mode
5–3	IBL[2–0]	$\overline{\text{IRQB}}$ Mode
2–0	IAL[2–0]	$\overline{\text{IRQA}}$ Mode

Table 14. DSP56303 Interrupt Priority Register P

Bit No.	Bit Name	
23–10	Reserved	Read as zero
9–8	T0L1–T0L0	Triple Timer Interrupt Priority Level
7–6	SCL1–SCL0	SCI Interrupt Priority Level
5–4	S1L1–S1L0	ESSI1 Interrupt Priority Level
3–2	S0L1–S0L0	ESSI0 Interrupt Priority Level
1–0	HPL1–HPL0	HI08 Interrupt Priority Level

4 Peripherals

The DSP56002 and DSP56303 peripherals compared in this section are the host interface, Enhanced Synchronous Serial Interface (SCI), triple timer, and the OnCE/JTAG port.

4.1 Host Interface

The DSP56002 host interface supports only non-multiplexed buses, single-strobe buses, and single host request bus modes. The DSP56303 HI08 host port supports non-multiplexed or multiplexed buses, single- or dual-strobe buses, and single- or double- host request bus modes. The discussion that follows refers to several DSP56002 and DSP56303 registers and to bits in those registers. To provide a context for this discussion, **Figure 4** and **Figure 5** show the DSP56002 and DSP56303 host block diagrams, respectively.

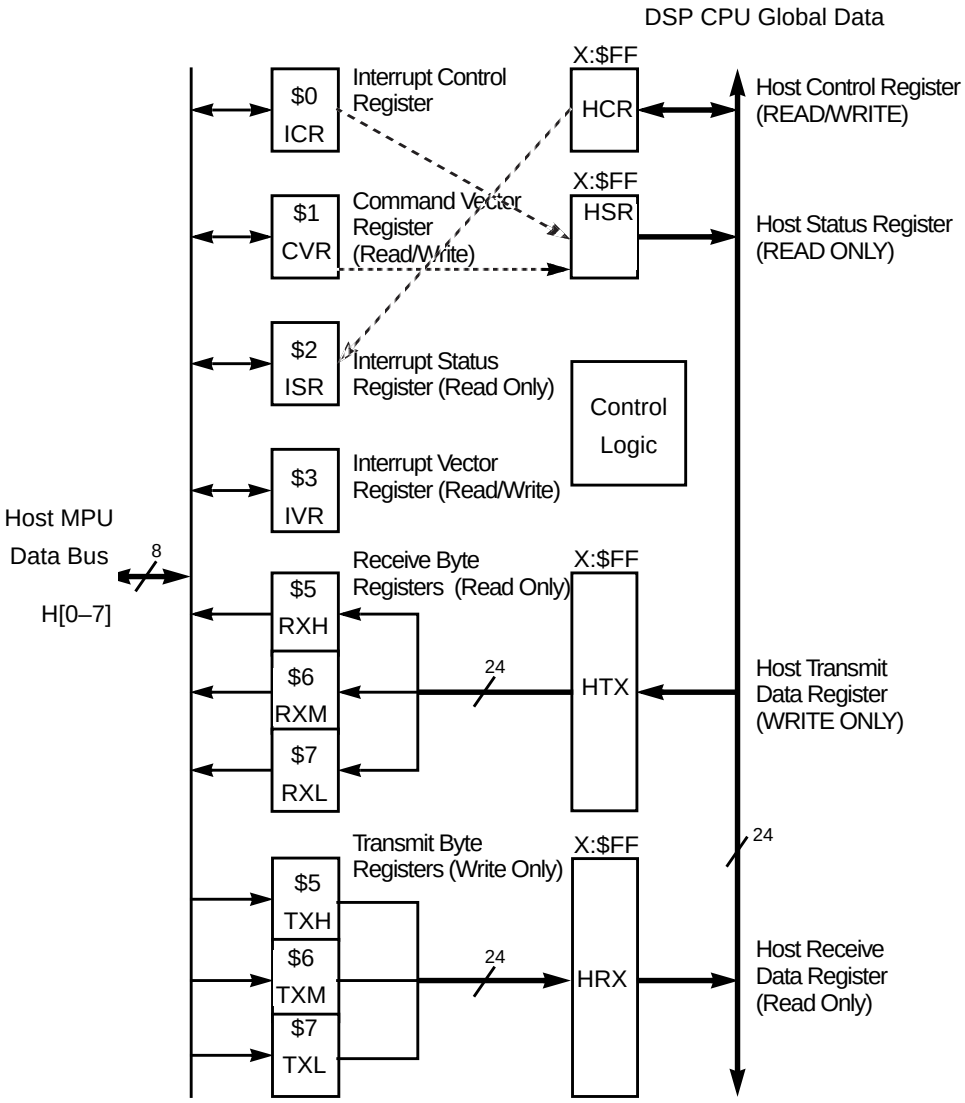


Figure 4. DSP56002 Host Block Diagram

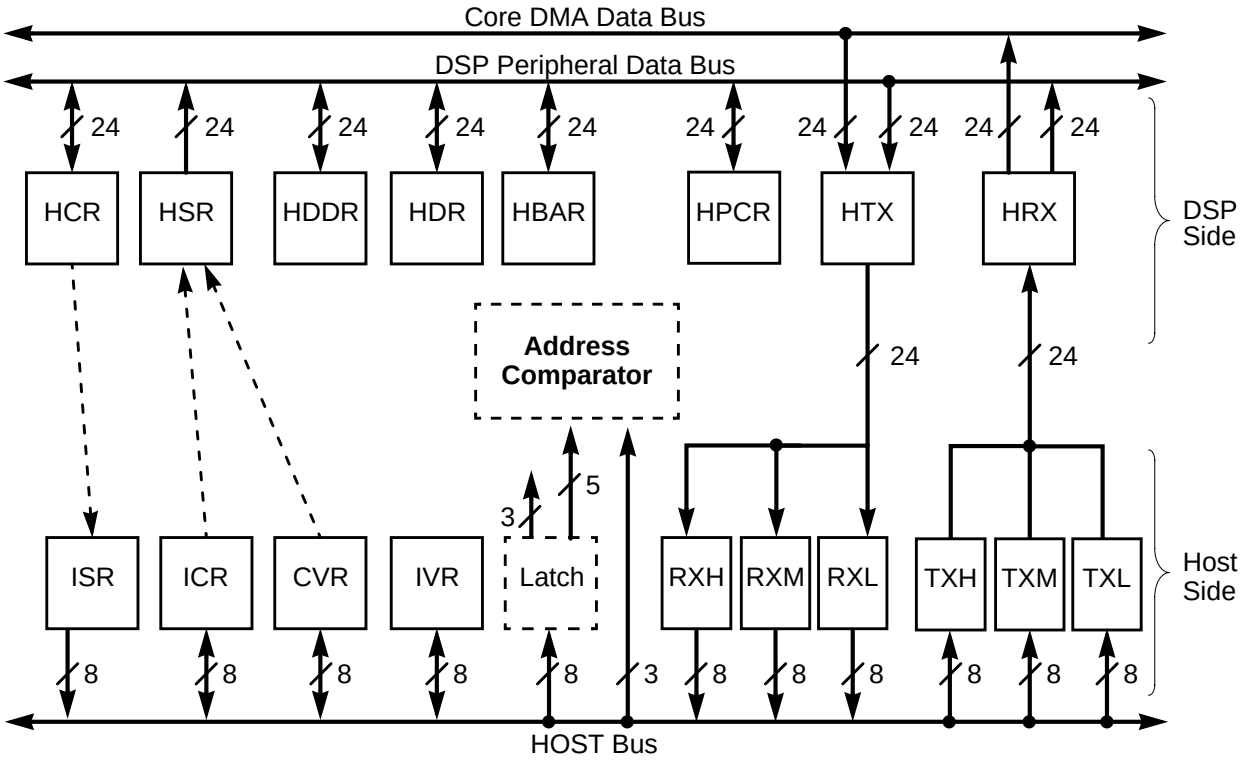
DSP-Side Registers

Control Registers

HCR = Host Control Register
HSR = Host Status Register
HPCR = Host Port Control Register
HBAR = Host Base Address Register

Data Registers

HTX = Host Transmit Register
HRX = Host Receive Register
HDDR = Host Data Direction Register
HDR = Host Data Register



Host-Side Registers

Control Registers

ISR = Interface Status Register
ICR = Interface Control Register
CVR = Command Vector Register
IVR = Interrupt Vector Register

Data Registers

RXH = Receive Register High
RXM = Receive Register Middle
RXL = Receive Register Low
TXH = Transmit Register High
TXM = Transmit Register Middle
TXL = Transmit Register Low

Figure 5. HI08 Block Diagram

4.1.1 Multiplexed Address/Data and Non-Multiplexed Bus Modes

In the DSP56002, the host data bus signals H[7–0] transfer data between the host processor and the DSP56002. The host address signals HA[2–0] provide the address selection for each host interface register. In the DSP56303, the HI08 connects to a multiplexed bus when the Host Multiplexed Bus (HMUX) bit in the Host Port Control Register (HPCR) is set. The HI08 employs the following signals (see **Table 15**):

- The Host Address/Data HAD[7–0] signals are lines 7–0 of the address/data bidirectional, multiplexed bus.
- The HAS/HAS signal is the Host Address Strobe input.
- The Host Address HA[10–8] signals are lines 10–8 of the Host Address input bus.

When the HPCR[HMUX] bit is cleared, the HI08 connects to a non-multiplexed bus (see **Table 15**):

- The values of the address lines are taken from the HI08 input pins.
- The Host Data H[7–0] signals are lines 7–0 of the data bidirectional bus.
- The Host Address Inputs HA[2–0] signals are lines 2–0 of the Host Address input bus.
- The HCS/HCS signal is the Host Chip Select input.

Table 15. HI08 Pin Definitions for Multiplexed/Non-Multiplexed Bus Modes

HI08 Signal	MUltiplexed Address/Data Bus Mode HMUX=1 in HPCR	Non-Multiplexed Bus Mode HMUX=0 in HPCR
HAD[7–0]	HAD[7–0]	H[7–0]
HAS/HA0	$\overline{\text{HAS}}$/HAS	HA0
HA8/HA1	HA8	HA1
HA9/HA2	HA9	HA2
HCS/HA10	HA10	$\overline{\text{HCS}}$/HCS

In the multiplexed bus mode, the Host Base Address Register (HBAR) selects the base address in which the host-side registers are mapped into the bus address space. The address from the host bus is compared with the address as programmed in the HBAR. If the addresses match, an internal chip select is generated. As **Table 16** shows, the Base Address bits, BA[10–3], reflect the base address in which the host-side registers map into the bus address space.

Table 16. DSP56303 Host Base Address Register (HBAR)

Bit No.	Bit Description	
15–8	Reserved	Read as zero
7–0	BA[10–3]	Base Address

4.1.2 Single/Dual Data Strobe Bus Modes

In the DSP56002, the host port operates in single-strobe bus mode. The Host Read/Write (HR/$\overline{W}$) input signal selects the direction of data transfer for each host processor access:

- If HR/$\overline{W}$ is high and the Host Enable (HEN) pin is asserted, H[7–0] are outputs and DSP data transfers to the host processor.
- If HR/$\overline{W}$ is low and the HEN pin is asserted, H[7–0] are inputs and host data transfers to the DSP.

In the DSP56303, the HI08 operates in the single-strobe bus mode when the Host Dual Data Strobe (HDDS) bit in the HPCR is cleared. The bus has a single data strobe signal for both read and write operations. The HDS/HDS signal qualifies the access, while the HRW signal specifies the direction of the access (see **Table 17**).

- When the HPCR[HDDS] bit is set, the HI08 operates in the dual data strobe bus mode. The bus has two separate data strobes, one for data reads ($\overline{HRD}$/HRD) and the other for data writes ($\overline{HWR}$/HWR).
- When the Host Data Strobe Polarity (HDSP) bit in the HPCR is cleared, the data strobe pin is configured as an active low input, and the data transfers when the data strobe is low.
- When HPCR[HDSP] is set, the data strobe pin is configured as an active high input, and the data transfers when the data strobe is high.

Table 17. HI08 Pin Definitions for Single- and Dual-Data Strobe Bus Modes

HI08 Signal	Single-Strobe Bus HDDS=0 in HPCR	Dual-Strobe Bus HDDS=1 in HPCR
HRW/HRD	HRW	$\overline{HRD}$/HRD
HDS/HWR	$\overline{HDS}$/HDS	$\overline{HWR}$/HWR

4.1.3 Single/Double Host Request Bus Modes

The DSP56002 supports the single-host request bus. The host interface uses the Host Request $\overline{HREQ}$ signal to request service from the host processor. In the DSP56303, the single-host request bus is selected when the Double-Host Request (HDRQ) bit in the Interface Control Register (ICR) is cleared. The HREQ/HTRQ and HACK/HRRQ signal pins are configured as the Host Request ($\overline{HREQ}$) and the Host Acknowledge ($\overline{HACK}$), respectively (see **Table 18**).

The $\overline{HREQ}$ pin is asserted when:

- The Receive Request Enable (RREQ) bit in the ICR is set and the Receive Data Register Full (RXDF) status bit in the Interface Status Register (ISR) is set.
- The Transmit Request Enable (TREQ) bit in the ICR is set and the Transmit Data Register Empty (TXDE) status bit in the (ISR) is set.

When the HDRQ bit is set, the double host request bus is selected. The HREQ/HTRQ and HACK/HRRQ signal pins are configured as the Transmit Host Request $\overline{HTRQ}$ and Receive Host Request $\overline{HRRQ}$, respectively. When the ICR[RREQ] bit is set and the ISR[RXDF] status bit is set, the $\overline{HRRQ}$ pin is asserted. When the ICR[TREQ] bit is set and the ISR[TXDE] status bit is set, the $\overline{HTRQ}$ pin is asserted.

Table 18. HI08 Pin Definitions for Single and Double Host Request Bus Modes

HI08 Signal	Single-Host Request Bus HDRQ=0 in ICR	Double-Host Request Bus HDRQ=1 in ICR
HREQ/HTRQ	$\overline{\text{HREQ}}$	$\overline{\text{HTRQ}}$
HACK/HRRQ	$\overline{\text{HACK}}$	$\overline{\text{HRRQ}}$

4.1.4 Big-Endian/Little-Endian Byte Order

The host can access the DSP56002 host port in little-endian byte order. The Receive/Transmit Register High (RXH/TXH) is located at address $5, the Receive/Transmit Register Middle (RXM/TXM) is located at address $6, and the Receive/Transmit Register Low (RXL/TXL) is located at address $7.

The DSP56303 host port supports both big-endian and little-endian byte order. If the Host Little-Endian (HLEND) bit in the ICR is cleared, the HI08 can be accessed in little-endian byte order. If ICR[HLEND] is set, the HI08 can be accessed in big-endian byte order, where RXH/TXH is located at address $7, RXM/TXM is located at address $6, and RXL/TXL is located at address $5 (see **Table 19**).

Table 19. Host-Side Register Map

Host Address	DSP56002	DSP56303		Registers
		Little Endian HLEND=0	Big Endian HLEND=1	
$0	ICR	ICR	ICR	Interface Control
$1	CVR	CVR	CVR	Command Vector
$2	ISR	ISR	ISR	Interface Status
$3	IVR	IVR	IVR	Interrupt Vector
$4				Unused
$5	RXH/TXH	RXH/TXH	RXL/TXL	Receive/Transmit Bytes
$6	RXM/TXM	RXM/TXM	RXM/TXM	
$7	RXL/TXL	RXL/TXL	RXH/TXH	

4.1.5 Host Registers

The DSP56002 and DSP56303 host control and host status registers are as follows:

- Host Control Register (HCR): In the DSP56002, the HCR is an 8-bit read/write control register by which the DSP controls the host interface interrupts and flags. In the DSP56303, the HCR is a 16-bit control register.
- Host Status Register (HSR): In the DSP56002, the HSR is an 8-bit read-only status register by which the DSP interrogates status and flags of the host interface. In the DSP56303, the HSR is a 16-bit read-only status register.

4.2 Enhanced Synchronous Serial Interface

The DSP56303 has two independent and identical Enhanced Synchronous Serial Interfaces: ESSI0 and ESSI1. The ESSI enhances the Synchronous Serial Interface (SSI) of the DSP56000 family with network, audio, and general improvements.

4.2.1 Network Enhancements

ESSI network enhancements include time slot registers, the end-of-frame interrupt, and the drive enable signal.

4.2.1.1 ESSI Time Slot Registers

The Transmit Slot Mask Registers (TSMA and TSMB) and the Receive Slot Mask Registers (RSMA and RSMB) reside on the DSP56303 but not on the DSP56002. TSMA and TSMB are accessible as a single 32-bit register with bits TS[31–0]. Bit ***n*** is an enable/disable control bit for transmission in slot number N. When TSn is cleared, all the transmit data registers of the enabled transmitters are tri-stated during transmit time slot number N. The data still transfers from the enabled Transmit Data Register(s) to the Transmit Shift Register, but the Transmit Data Empty (TDE) and the Transmit Underrun Error (TUE) flags in the SSI Status Register (SSISRx) are not set. During a disabled slot, no transmitter empty interrupt is generated. The DSP is interrupted only for the enabled slots. Data written to the Transmit Data Register when the transmitter empty interrupt request is serviced is transmitted in the next enabled transmit time slot. When TSn is set, data is transferred from the transmit register to the shift register during slot number N and the TDE flag is set.

RSMA and RSMB are accessible as a single 32-bit register with bits RS[31–0]. Bit *n* is an enable/disable control bit for time slot number N. When RSn is cleared, all the data signals of the enabled receivers are tri-stated during receive time slot number N. Data transfers from the Receive Data Register(s) to the Receive Shift Register, but the Receive Data Full (RDF) and the Receive Overrun Error (ROE) flags in the SSI Status Register (SSISRx) are not set. During a disabled slot, no receiver full interrupt is generated. The DSP is interrupted only for the enabled slots. When RSn is set, data is received during slot number N, and the RDF flag is set.

4.2.1.2 End-of-Frame Interrupt

When the Transmit Last Slot Interrupt Enable (TLIE) bit in the ESSI Control Register A (CRAx) is set, the DSP is interrupted at the start of the last slot in a frame, regardless of the Transmit Mask Register setting. When TLIE is cleared, the transmit last slot interrupt is disabled.

When the Receive Last Slot Interrupt Enable RLIE bit in the ESSI Control Register A (CRAx) is set, the DSP is interrupted after the last slot of a frame ends, regardless of the Receive Mask Register setting. When RLIE is cleared, the receive last slot interrupt is disabled.

4.2.1.3 Drive Enable Signal

When the Select SC1 as Transmitter 0 Drive Enable (SSC1) bit in the CRAx register is set, the SC1 signal acts as the driver enable of transmitter 0 while the SC1 signal is configured as output. This enables the use of an external buffer for the transmitter 0 output. When SSC1 is cleared, the ESSI is configured in synchronous mode, and transmitter 2 is disabled, the SC1 acts as the serial I/O flag and the SC1 signal is configured as output.

4.2.2 Audio Enhancements

The DSP56303 has three transmitters (TX0, TX1, and TX2) per ESSI, which is ideal for 6-channel surround mode. For example, the DSP can transmit the following channels: left/right, center/subwoofer, and left surround/right surround.

4.2.3 General Enhancements

Some general enhancements on the DSP56303 are as follows:

- DMA Interrupts: The DMA can service the ESSI transmitters and receivers.
- Separate Exception Enable Bits: You can enable the exceptions listed in **Table 20** by setting the following bits in the CRBx register:

Table 20. ESSI Receive and Transmit Exceptions

Exception	Enable Bit in CRB
Receive Data with Exception Status	23
Receive Data	19
Receive Last Slot	21
Transmit Data with Exception Status	22
Transmit Data	18
Transmit Last Slot	20

- Internal Bit Clock: The divide by 2 block in the DSP56002 SSI clock generator chain is absent in the DSP56303 ESSI clock generator. **Figure 6** shows the internal bit clock block diagram of each device.

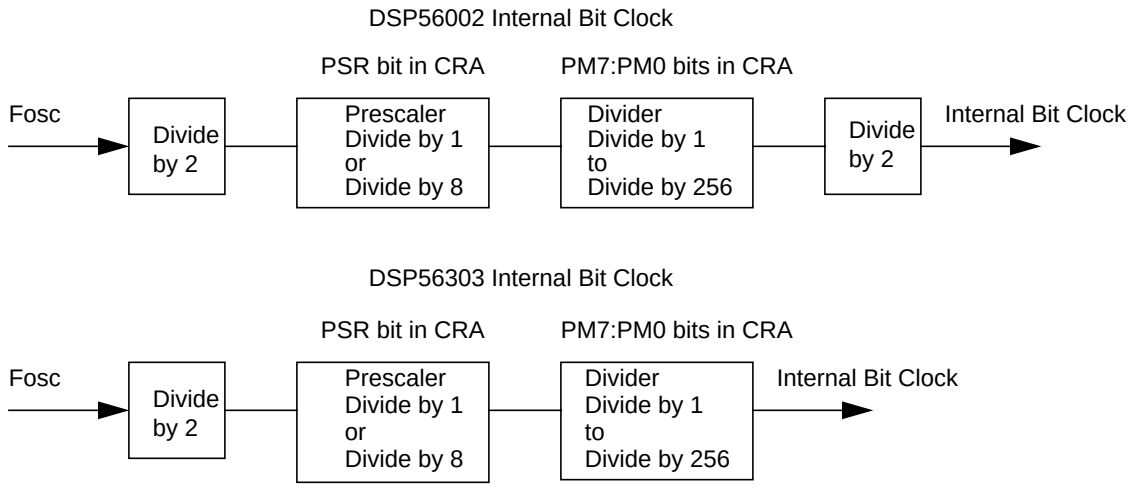


Figure 6. DSP56002 and DSP56303 Internal Bit Clock Block Diagram

- CRA Prescaler Range Bit Definition: In the DSP56002, when the Prescaler Range (PSR) bit in the CRA is set, the fixed divide-by-eight prescaler is operational. When PSR is cleared, the fixed prescaler is bypassed. In the DSP56303, the bit definition is reversed. When CRAx[PSR] is set, the fixed prescaler is bypassed. When CRAx[PSR] is cleared, the fixed divide-by-eight prescaler is bypassed.
- Gated Clock Mode: In the DSP56002, the Gated Clock Control (GCK) bit in the CRB register selects between a continuously running data clock or a gated clock that runs only when there is data to be sent in the transmit shift register. This mode is not available in the DSP56303.

4.3 Triple Timer

The DSP56303 triple timer module consists of a common 21-bit prescaler and three independent and identical general-purpose 24-bit timer/event counters, each with its own register set. Each timer TIO[2–0] can use internal or external clocking and can perform the following functions:

- Interrupt the DSP after a specified number of events
- Signal an external device after counting internal events
- Trigger DMA transfers after a specified number of events

4.3.1 Operating Modes

In the DSP56002, the Timer Control TC[2–0] bits in the Timer Control and Status Register (TCSR) control the source of the timer clock, the behavior of the TIO pin, and the timer mode of operation. (see **Table 21**).

Table 21. DSP56002 Timer Modes of Operation

Bit Settings			Mode Characteristics			
TC2	**TC1**	**TC0**	**TIO**	**Clock**	**#**	**Name**
0	0	0	GPIO	Internal	0	Timer GPIO
0	0	1	Output	Internal	1	Timer Pulse
0	1	0	Output	Internal	2	Timer Toggle
1	0	0	Input	Internal	4	Measurement Input Width
1	0	1	Input	Internal	5	Measurement Input Period
1	1	0	Input	External	6	Standard Timer Counter
1	1	1	Input	External	7	Event Counter

In the DSP56303, the TC[3–0] bits in the TCSR[2–0] registers control the source of the timer clock, the behavior of the TIO signal, and the timer mode of operation. Whereas the DSP56002 supports only timer and measurement modes of operation, the DSP56303 also supports pulse-width modulation and watchdog modes of operation (see **Table 22**).

Table 22. DSP56303 Triple Timer Modes of Operation

Bit Settings				Mode Characteristics			
TC3	TC2	TC1	TC0	TIO	Clock	No.	Name
0	0	0	0	GPIO	Internal	0	Timer GPIO
0	0	0	1	Output	Internal	1	Timer Pulse
0	0	1	0	Output	Internal	2	Timer Toggle
0	0	1	1	Input	External	3	Timer Event Counter
0	1	0	0	Input	Internal	4	Measurement Input Width
0	1	0	1	Input	Internal	5	Measurement Input Period
0	1	1	0	Input	Internal	6	Measurement Capture
0	1	1	1	Output	Internal	7	Pulse Width Modulation
1	0	0	1	Output	Internal	9	Watchdog Pulse
1	0	1	0	Output	Internal	10	Watchdog Toggle

- Pulse-Width Modulation mode: The timer generates periodic pulses of a preset width. The value to count is loaded into the Timer Compare Register (TCPR). When the first timer clock is received from the DSP56303 internal clock divided by two or the prescaler clock output, the counter is loaded with the Timer Load Register (TLR) value. Each subsequent timer clock increments the counter.

  When the counter equals the value in the TCPR, the TIO output signal is toggled and the Timer Compare Flag (TCF) in the Timer Control/Status Register (TCSR) is set. The contents of the counter are placed into the Timer Count Register (TCR). If the Timer Compare Interrupt Enable (TCIE) bit in the TCSR is set, a compare interrupt is generated. The counter continues to increment on each timer clock.

- Watchdog Pulse mode: The timer generates an external signal at a preset rate. The signal period is equal to the period of one timer clock. The value to count is loaded into the TCPR. When the first timer clock is received from the DSP56303 internal clock divided by two or the prescaler clock output, the counter is loaded with the TLR value. Each subsequent timer clock increments the counter.

  When the counter equals the value in the TCPR, the TCSR[TCF] bit is set. The contents of the counter are placed into the TCR. If the TCSR[TCIE] bit is set, a compare interrupt is generated. The counter continues to increment on each timer clock.

- Watchdog Toggle mode: The timer toggles an external signal after a preset period. The value to count is loaded into the TCPR. When the first timer clock is received from the DSP56303 (the internal clock divided by two or the prescaler clock output), the counter is loaded with the TLR value. Each subsequent timer clock increments the counter. When the counter equals the value in the TCPR, the TCSR[TCF] bit is set. The contents of the counter are placed into the TCR. If the TCSR[TCIE] bit is set, a compare interrupt is generated. The counter continues to increment on each timer clock.

- DMA Trigger: In the DSP56303, each timer can trigger DMA transfers when a DMA channel is programmed to trigger by a timer event. The timer issues a DMA trigger on every event in all modes of operation. The DMA channel cannot save multiple DMA triggers generated by the timer. To ensure that all DMA triggers are serviced, you must provide for the preceding DMA trigger to be serviced before the DMA channel receives the next trigger.

5 OnCE/JTAG PORT

Unlike the DSP56000, the DSP56300 core On-Chip Emulation (OnCE) functionality is accessed through the Joint Test Access Port (JTAG).

5.1 Signals

In the DSP56000 core, the following pins are associated with the OnCE controller:

- Debug Serial Input/Chip Status 0 (DSI/OS0):
  - — As input: provides serial data or commands to the OnCE controller.
  - — As output: works in conjunction with the OS1 pin to provide chip status information.
- Debug Serial Output (DSO):
  Carries serial data that is read from the OnCE and provides acknowledge pulses to the external command controller.
- Debug Serial Clock/Chip Status 1 (DSCK/OS1):
  - — As input: supplies the serial clock to shift data in and out of the OnCE port.
  - — As output: works in conduction with the OS0 pin to provide chip status information.
- Debug Request ($\overline{\text{DR}}$):
  This input pin allows you to enter Debug mode from the external command controller.

In the DSP56300 core, the following pins are associated with the OnCE/JTAG controller:

- Test Data Input (TDI):
  Serial test instruction and data are received through this pin.
- Test Data Output. (TDO):
  Serial output for test instructions and data are transmitted through this pin.
- Test Clock (TCK):
  Synchronizes the test logic.
- Test Mode Select (TMS):
  Sequences the test controller’s state machine.
- Test Mode Select ($\overline{\text{TRST}}$):
  Initializes the test controller.
- Debug Event ($\overline{\text{DE}}$):
  Enters Debug mode

5.2 Debug Mode

Asserting the $\overline{DR}$ pin causes the DSP56000 core to finish executing the current instruction, save the instruction pipeline information, and enter Debug mode. The DSO pin pulses low to acknowledge that the OnCE is in Debug mode and is awaiting commands from the DSI signal.

Asserting the $\overline{DE}$ pin causes the DSP56300 core to finish executing the current instruction, save the instruction pipeline information, and enter Debug mode. A pulse is generated on the $\overline{DE}$ line every time the chip acknowledges the execution of an instruction in Debug mode. The DSP56300 core can also enter Debug mode when software executes the JTAG DEBUG_REQUEST instruction by shifting in the four bits '0111' on the TDI pin and using the TMS to sequence the test controller's state machine. Sending the DEBUG_REQUEST instruction again shifts the status information '1101' out on the TDO pin to indicate that the DSP is in Debug mode.

Before you can perform system debug functions, you must execute the JTAG ENABLE_ONCE instruction by shifting in the four bits '0110' in the TDI pin while using the TMS to sequence the test controller's state machine.

5.3 Chip Status

In the DSP56000 core, the OS1 and OS0 pins provide chip status information. In the DSP56300 core, chip status information is provided by the read-only status bits OS1and OS0 (bits 7-6) in the OnCE Status and Control Register (OSCR) (see **Table 23**).

Table 23. DSP56300 Chip Status Information

OS1	OS0	Chip Status
0	0	Core is executing instructions.
0	1	Core is in Wait or Stop state.
1	0	Core is waiting for bus.
1	1	Core is in Debug mode.

5.4 TAP Controller State Machine

The TAP controller state machine is available only on the DSP56300 core. The JTAG port consists of a TAP controller state machine that controls the operation of the JTAG logic. The value on the TMS signal changes the TAP controller's state on the rising edge of the TCK signal. **Figure 7** shows the TAP controller state machine. As the figure shows, there are two paths to the TAP controller state machine. The first path consists of the Select_DR_Scan, Capture_DR, Shift_DR, Exit_DR, and Update_DR states, which capture and load data into the test data register. For example, reading the pipeline registers requires the use of this sequence.

The second path consists of the Select_IR_Scan, Capture_IR, Shift_IR, Exit_IR, and Update_IR states, which capture and load instructions into the instruction register. For example, shifting in the JTAG ENABLE_ONCE instruction requires the use of this sequence.

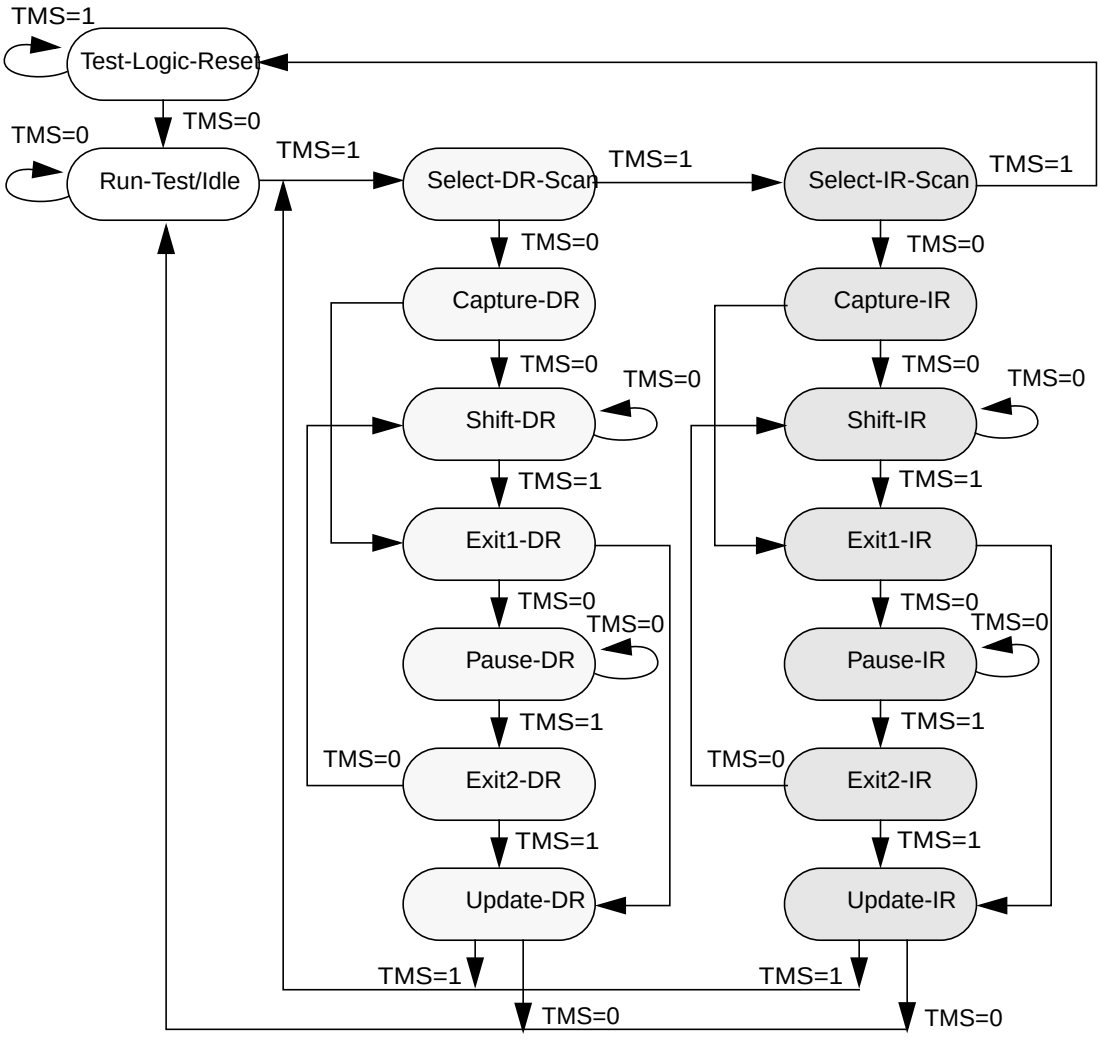


Figure 7. TAP Controller State Machine

5.5 OnCE Controller

Three key components associated with the OnCE Controller are the OnCE Status and Control Register (OSCR), OnCE Memory Breakpoint Logic, and the OnCE pipeline.

5.5.1 OnCE Status and Control Register

In the DSP56000 core, the OnCE Status and Control Register (OSCR) is a 16-bit register that selects the events to put the DSP in Debug mode and to indicate the reason for entering Debug mode. In the DSP56300 core, the OSCR is a 24-bit register.

5.5.2 OnCE Memory Breakpoint Logic

Table 24 compares the OnCE memory breakpoint logic on the DSP56002 and the DSP56303.

Table 24. OnCE Memory Breakpoint Logic on the DPS56002 and DSP56303

DSP56002	DSP56303
OnCE Memory Address Latch (OMAL)	
The OMAL is a 16-bit register that latches the PAB, XAB, or YAB on every instruction cycle according to the Memory Breakpoint Control BC[3–0] bits in the OSCR.	The OMAL is a 24-bit register that latches the PAB, XAB or YAB on every instruction cycle according to the Memory Breakpoint Select MBS[1–0] bits in the OnCE Breakpoint Control Register (OBCR).
Memory Limit Registers	
The OnCE Memory Upper Limit Register (OMULR) is a 16-bit register that stores the memory breakpoint upper limit. The OnCE Memory Lower Limit Register OMLLR is a 16-bit register that stores the memory breakpoint lower limit.	The OnCE Memory Limit Register 0 (OMLR0) is a 24-bit register that stores the memory breakpoint upper limit. The OnCE Memory Limit Register 1 (OMLR1) is a 24-bit register that stores the memory breakpoint lower limit.
Memory Address Comparators	
The OnCE Memory High Address Comparator (OMHC) compares the current memory address stored in the OMAL with the OMULR contents. The OnCE Memory Low Address Comparator OMLC compares the current memory address stored in the OMAL with the OMLLR contents.	The OnCE Memory Address Comparator 0 (OMAC0) compares the current memory address stored in the OMAL with the OMLR0 contents. The OnCE Memory Address Comparator 1 (OMAC1) compares the current memory address stored in the OMAL with the OMLR1 contents.

5.5.3 OnCE Pipeline

Table 25 compares the OnCE pipeline on the DSP56002 and the DSP56303.

Table 25. OnCE Pipeline on the DSP56002 and the DSP56303

DSP56002	DSP56303
Program Address Bus for Fetch Register (OPABFR)	
The OPABFR is a 16-bit register that stores the address of the last instruction fetched before Debug mode was entered.	The OPABFR is a 24-bit register that stores the address of the last instruction fetched before Debug mode was entered.
Program Address Bus for Decode Register (OPABDR)	
The OPABDR is a 16-bit register that stores the address of the instruction currently in the instruction latch. This is the instruction that would have been decoded if the DSP had not entered Debug mode.	In the DSP56300 core, the OPABDR is a 24-bit register that stores the address of the instruction currently on the program data bus. This is the instruction whose fetch completed before the DSP entered Debug mode.
Program Address Bus for Execute Register (OPABEX)	
Not Available	The OPABEX is a 24-bit register that stores the address of the instruction currently in the instruction latch. This is the instruction that would have decoded and executed if the DSP had not entered Debug mode.
Trace Buffer	
The Program Address Bus (PAB) FIFO stores the addresses of the last five instructions that executed. The FIFO is a circular buffer containing five 16-bit registers and one 3-bit counter.	The trace buffer stores the addresses of the last 12 change of flow instructions that executed and the address of the last executed instructions. The trace buffer is a circular buffer containing twelve 25-bit registers and one 4-bit counter.

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