AN4005

Thermal Management and Mounting Method for the PLD 1.5 RF Power Surface Mount Package

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THERMAL MANAGEMENT DESIGN AND POWER DISSIPATION

Thermal management of surface mount components is an important issue when dissipating power levels in excess of 2 watts. At less than 2 watts, thermal management can be accomplished through the contact pad on the printed circuit board (PCB). The power dissipation of the surface mount device is a function of the pad size used for the source contact. However, in excess of 2 watts alternative thermal management techniques are necessary to remove the heat dissipated in the device in order to maintain device junction temperatures within the specified range of reliable operation 150°C maximum which is for plastic encapsulated devices. Typical applications of the PLD 1.5 package (case 466–02) produce a power dissipation of 5–7 watts, with maximum dissipation in the range of 10–12 watts for short periods of time. The thermal management approach often considered for these power levels is the use of a metal slug soldered directly to the source contact of the device which then protrudes down through the PCB. The metal slug is typically soldered along the sides of the PCB through–hole, and a thermal grease or thermal pad contact is made from the bottom of the metal slug to a larger heat sink or chassis. Although this approach produces very good thermal transfer characteristics, Coefficient of Thermal Expansion (CTE) mismatches create undesirable stress in this overall structure which can result in premature device failure. This thermal management technique is not recommended for leadless power surface mount components (See Technical Bulletin EB209/D “Mounting Method for RF Power Leadless Surface Mount Transistors,” for more detailed information.)

The recommended method for thermal management of the PLD 1.5 package is the use of solder filled thermal vias fabricated in the PCB. The number of vias, via diameter, and via density will be a function of the specific application. A trade–off exists between the required performance of the thermal via structure and the cost of the PCB which must be evaluated for each specific application. The recommended design detailed here is one which achieves thermal performance for solder–filled vias while maintaining PCB manufacturability. This recommended thermal via pattern is shown in Figures 1a, 1b and 1c.

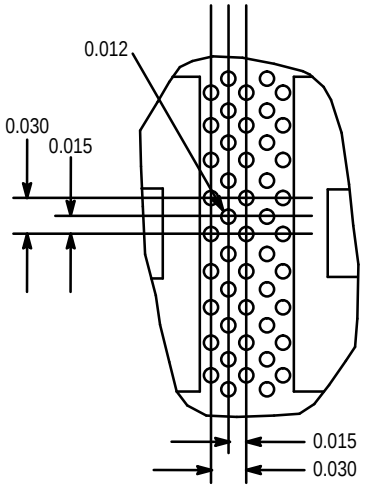

Figure 1a. Top View of the Thermal Via Pattern with Dimensions

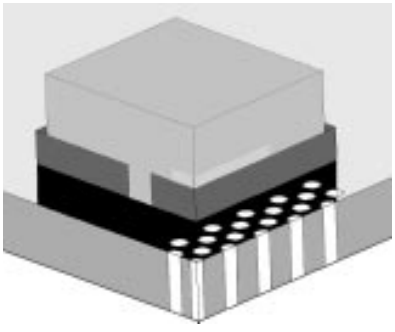

Figure 1b. PLD 1.5 Mounted on PCB with Thermal Vias, One–quarter Exploded Solid Model View

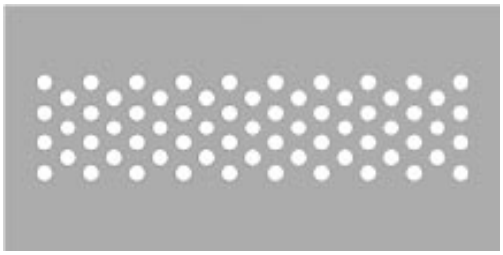

Figure 1c. Closeup of the PCB Via Layout with 12 mil Diameter Centers, 15 x 30 mil Pitch

Finite Element Analysis (FEA) models were developed using ANSYS 5.0. The models were validated with empirical data taken on circuits constructed of 0.040″ thick glass–epoxy PCBs with the solder–filled thermal via design described in Figure One. The data yielded a typical thermal resistance from junction–to–heat sink of 4.2°C/W. Using sufficient engineering margin and allowing for as much as 20% voiding in the thermal vias, the junction–to–heatsink thermal resistance is specified to be 6.25°C/W maximum. The maximum power dissipation for this device at a heatsink temperature of 25°C can then be calculated as follows:

$$P_{Dmax} = (T_{Jmax} - T_S) / \theta_{JS}$$

where:

T_{Jmax} is the maximum allowable junction temperature (°C)

T_S is the heatsink temperature (°C)

P_{Dmax} is the maximum allowable dissipated power (W)

θ_{JS} is the junction–to–heatsink thermal resistance (°C/W)

$$P_{Dmax} = (150°C - 25°C) / 6.25°C/W$$
$$P_{Dmax} = 20\ W$$

Since it is typically impractical to maintain the heatsink temperature at 25°C, a calculation of the maximum heatsink temperature is of importance to the radio designer, especially for portable units in which space is extremely limited. The following calculation is based upon 8 watts of RF output power @ 50% efficiency and sufficient gain such that the input power is negligible. The dissipated power is then approximately 8 watts.

$$T_S = T_{Jmax} - P_D \times \theta_{JS}$$
$$T_S = 150°C - (8\ W \times 6.25°C/W)$$
$$T_S = 100°C$$

Thus, the maximum heatsink temperature with the MRF1507 and a thermal via board with the dimensions and construction detailed herein is 100°C.

COMPONENT BOARD ASSEMBLY MANUFACTURING PROCESS

Solder coverage of the device contacts and percentage fill of the thermal vias are critical to the overall thermal performance of the design. This is best accomplished by the board supplier using a hot air solder leveling process. If this has not been done by the supplier, then the manufacturing process must encompass two additional steps: 1) solder fill of the vias using a screenprinting process and 2) then screenprint of the component solder. This is then followed by pick–and–place of the components and reflow.

Component lands must have features to maintain a consistent solderable land area when the component is placed on a ground plane or is connected to other lands with conductors wider than 0.015 inches. (IPC–SM–782 recommends 0.010″ maximum). This can be accomplished in one of two ways:

a. Solder mask over bare copper: The solder mask must be over the bare copper or over a metal which does not melt during reflow. If it is placed over the tin/lead, the solder will flow under the mask during reflow. The minimum web width for solder mask between features is 0.005 inches.

b. Conductor narrowing: Necking down the track before it enters the component land area is another effective way to block the migration of solder away from the part. The “neck-down” width should be a maximum of 0.010″ to 0.015 inches. The length of the necked down conductor should also be 0.015″ minimum.

As stated above, it is recommended that the vias in the PCB be filled during board fabrication using a hot air solder leveling process (HASL). If this is not done, then the board will be processed through assembly in two steps. The first screen printing step fills the vias with solder, and the second step solders the components to the board. To minimize “doming” at the bottom surface of the vias during the reflow, it is recommended that the vias are kept small, i.e., less than 0.012″ diameter. Kapton tape can also be applied over the vias on the bottom side of the board to restrict solder flow from the vias.

Paste is then screened on using standard equipment types and process settings for 62/36/2 Sn/Pb/Ag. The stainless steel solder stencil used for our application was 6 mils thick. A FUJI CP4–3 pick–and–place was used for component placement and programmed force used is specific to the component geometry which is being placed. The reflow ovens used were convection style BTU.

In the solder reflow step, the board is first preheated to 150°C. Once preheated, the temperature then is raised to just above 150°C in a “soak” for one minute minimum to stabilize the board temperature. Best reflow characteristics are then achieved by a “spike” above the 183°C liquidus. Peak temperature is at 215°C + / – 10°C. Maximum time above the liquidus temperature is 90 seconds with 30–60 seconds typical, while maximum time above 150°C is 5.5 minutes.

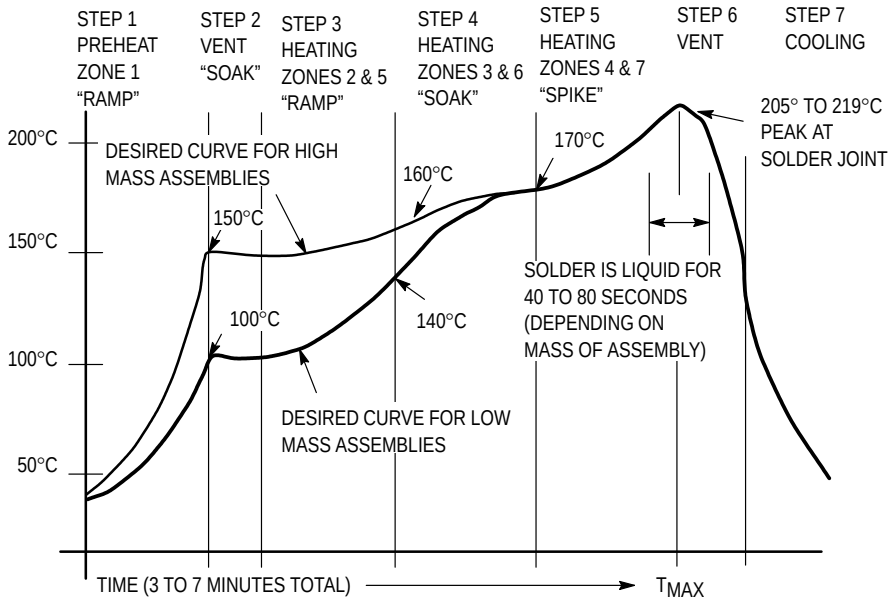

Figure 2. Typical Solder Heating Profile

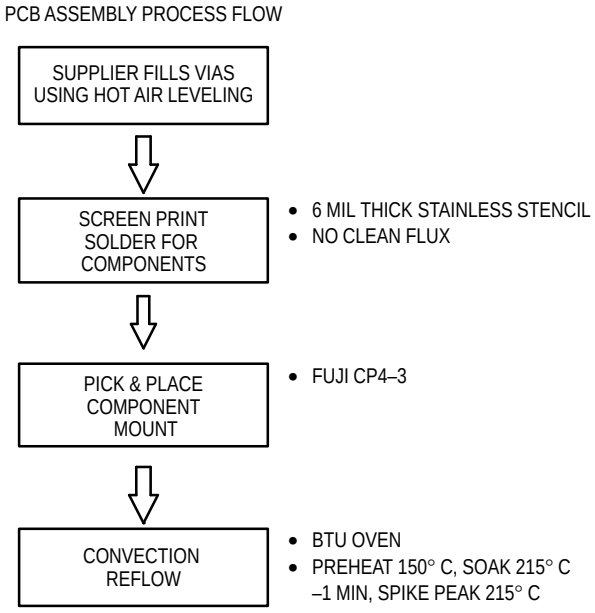

Figure 3. PCB Assembly Steps for the Process Flow

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