An MC88100/MC88200 20/25/33 MHz system DRAM Design

By John Ralston
European High-end Microprocessor Applications Group
Motorola Ltd
East Kilbride

INTRODUCTION

This Application Note has a lengthy companion document for those who need it. This is Reference AN447A/D, which gives details of the Schemata, Programmable Logic Devices source code and Timing Diagrams, in the form of Appendices A, B and C. Reference AN447A/D may be obtained from any Motorola Distributor or from the European Literature Centre listed on the back page of this document.

This Application Note describes a DRAM design for an MC88100/MC88200 system. A block diagram of the system is shown in Figure 1. Only the CPU NODE (MC88100/MC88200s) and DRAM will be discussed in detail in this document. This includes timing for other interfaces, VME (master and slave) and Input/Output Processor (IOP), that concern the DRAM. The system/DRAM is designed to operate at a range of frequencies (20MHz, 25MHz and 33MHz) and memory configurations, with no modifications to the final printed circuit board. This is achieved by changing five jumpers and two Programmable Logic Devices (PLD) for each configuration. The supported DRAM memory configurations are detailed in Table 1.

DRAM Module Configuration	Number of Banks	Total Memory
1M x 8	One	4MB
1M x 8	Two	8MB
4M x 8	One	16MB
4M x 8	Two	32MB

Table 1. DRAM Memory Configurations

The performance of the DRAM subsystem, using 80ns SIMMs, is shown in Table 2. The 80ns versions of the DRAM modules were chosen, as at the time of design/manufacture this was the only speed available in both 1Mx8 and 4Mx8 DRAM modules in any volume.

Cycle Type	Number of DRAM BANKS	Frequency	Number of Access cycles
MBUS ACCESSES			
Read Burst	One	20/25MHz	4-2-2-2
Read Burst	Two	20/25MHz	4-1-1-1
Read	One or Two	20/25MHz	4
Write Burst	One or Two	20/25MHz	2-2-2-2
Write	One or Two	20/25MHz	2
Read Burst	One	33MHz	6-3-3-3
Read Burst	Two	33MHz	6-2-2-2
Read	One or Two	33MHz	6
Write Burst	One or Two	33MHz	2-3-2-2
Write	One or Two	33MHz	2
IOP ACCESS			
Read	One or Two	20/25MHz	6
Write	One or Two	20/25MHz	5
Read	One or Two	33MHz	7
Write	One or Two	33MHz	6
VME ACCESS			
Read	One or Two	20/25MHz	6
Write	One or Two	20/25MHz	5
Read	One or Two	33MHz	7
Write	One or Two	33MHz	6

Table 2. DRAM Subsystem Performance
(Using 80ns nibble mode, 1Mx8 MCM8101F80 or 4MBx1 MCM84001F80)

DESIGN IMPLEMENTATION

The design is a single master configuration with respect to the MBUS. As the CPU NODE requires access to the VME (Slave) as well as the DRAM, and the VME (Master) also requires access to the DRAM, the MBUS and VME (Master) use a common secondary bus called MV (MBUS/VME bus) that connects into the DRAM subsystem. The IOP requires access only to the DRAM and it has its own separate port into the DRAM subsystem. The entire design is synchronous with respect to the MBUS clock. Detailed below is the functional description of the various blocks making up the design.

SYSTEM CLOCKS

All clocks for the system are generated from a Low Skew CMOS PLL Clock Driver, MC88915. This device is used as it gives CMOS levels with the correct duty cycle and has rise and fall times required for the MC88100 and MC88200. Also, it has many outputs that have a skew of less than one nanosecond allowing for, in this case, a single clock source solution for this synchronous design.

M88000 Interface

The M88000 interface includes logic for decoding MBUS transactions, performing arbitration for the two MC88200s (code and data), and reset control for the MC88100.

CPU NODE

The CPU node consists of a single MC88100 cpu, an MC88200 used as a data cache, and a second MC88200 used as a code cache.

PHASE LOCKING

The MC88100 and MC88200s of the CPU node require to be phase locked to the MBUS clock; this phase locking is performed by PLD **M_RESET** shown in Figure 1 of the schemata in Appendix A of Reference AN447A/D. The PLD **M_RESET** ensures that the **M_PLLEN** signal is asserted with the correct relationship to the **M_RST-** via a simple counter, counting MBUS clocks.

(Note: A minus sign postfixing a signal means its asserted state is a logic zero.)

MBUS ARBITRATION

The arbitration between the two MC88200s for the MBUS is performed in PLD **M_ARB** shown in Figure 2 of Appendix A of AN447A/D. The data MC88200 has the highest priority. This is done to ensure loads and stores complete in a timely fashion.

MBUS SYSTEM STATUS LINES

The local status **M_CST(3:0)** and **M_DST(3:0)** from the code and data MC88200 are combined in PLD **M_RESET** with the following control signals from the DRAM, VME, and MV/MBUS interface control, detailed in Table 3 below, to form the MBUS system status signals **M_SS-(3:0)**.

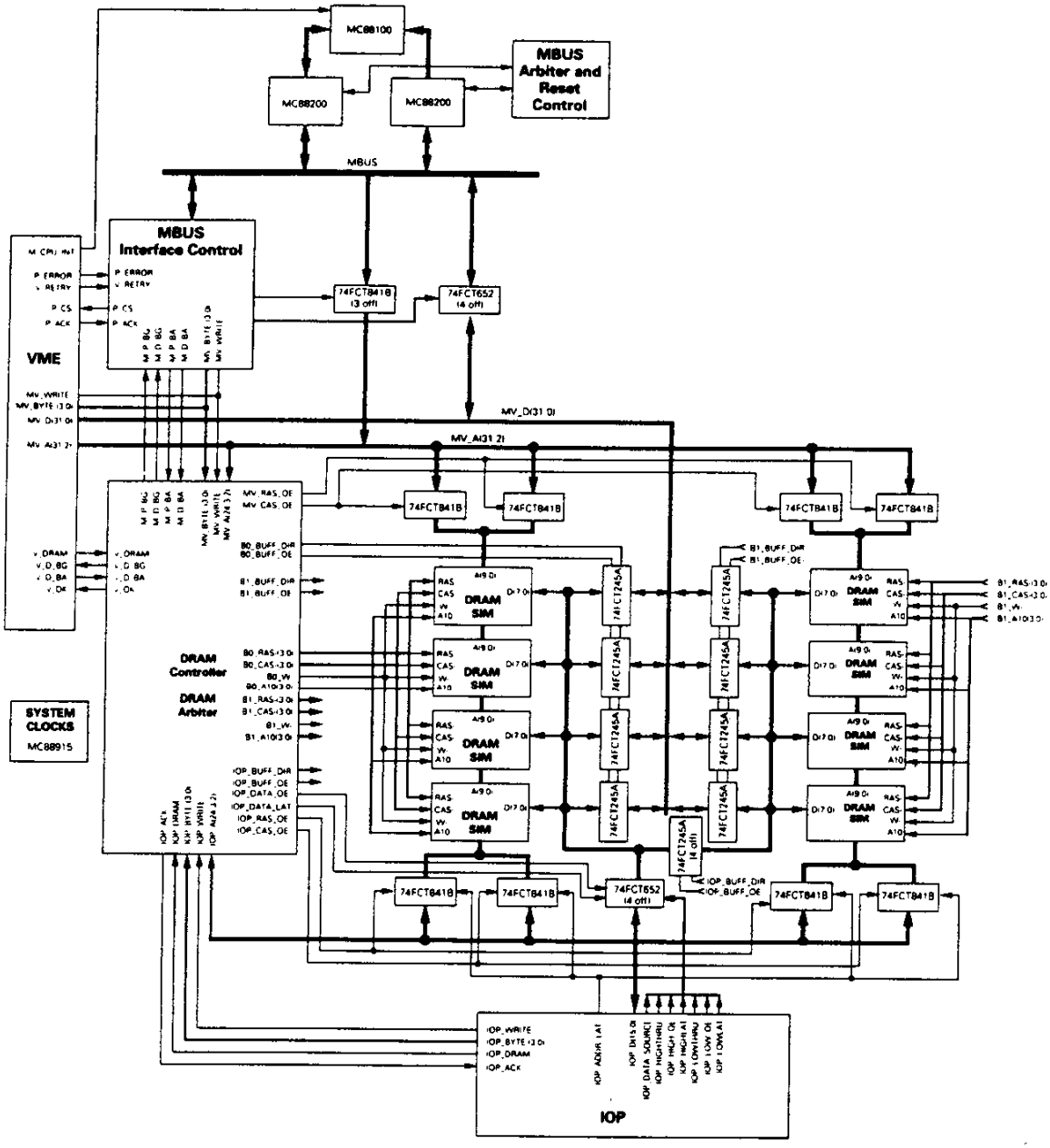

Figure 1. System Block Diagram

Signal Name	Action	Description
V_RETRY-	Forces MBUS RETRY.	Asserted by the VME interface when a collision between a VME (Master) access to the DRAM and a VME (Slave) access by the M88000 is detected.
P_ERROR-	Forces MBUS ERROR.	Asserted by a peripheral in the VME interface memory map.
M_WAIT_MBUS-	Forces MBUS WAIT.	Asserted by the MBUS interface controller PLD **M_DECODE** to wait the MBUS if either the MV bus is not granted or the VME (slave) access has not responded with an acknowledge.
D_WAIT_MBUS-	Forces MBUS WAIT.	Asserted by the DRAM state machine during a MBUS DRAM access.

Table 3. Signals controlling the MBUS System Status Signals

MBUS to MV Interface

The MBUS to MV interface, shown in Figure 2 of Appendix A of AN447A/D, consists of two sections, which are detailed below.

MBUS DECODE

The MBUS decode is implemented in a single PLD **M_DECODE**, with the following memory map:

Access Type	Memory Range	Select Signal Generated
DRAM	0x00000000 - 0x1FFFFFFF	**M_D_BA-**
Peripheral (VME and registers)	0x20000000 - 0xCFFFFFFF	**P_CS-**
MC88200 Control	0xD0000000 - 0xFFFFFFFF	n/a

CPU NODE Memory Map

There are two bus grant signals used by **M_DECODE** to generate selects to DRAM or VME, and waits, **M_WAIT_MBUS-**, on the MBUS. The first is **M_P_BG-** allowing access to the VME (slave) interface. The second is **M_D_BG-** allowing access to the DRAM. These grants are pre-emptive in that they are given without a request. See the section on **DRAM ARBITER** for a full explanation.

ADDRESS and DATA LATCHES

The address latch consists of three 10-bit transparent latches (74FCT841B) to capture the address, **MV_A(31:2)**, during the address phase of an MBUS transaction. The data latch is made from four, 8-bit latch transceivers (74FCT652) to latch the data from, and pass data to the MBUS and MV bus **MV_D(31:0)**. These latches and transceivers are controlled by the PLD **M_LATCH**. A feature of the data latch is that the initial write from the MBUS is latched. If the MBUS transaction consists of a single data phase then the MBUS performs a zero wait state write cycle. The PLD **M_LATCH** also latches the transaction type, read/write, during the address phase of the MBUS transaction and generates **MV_WRITE-** from it. The byte strobes are latched from the initial data phase of the MBUS transaction by the PLD **M_ARB** to produce **MV_BYTE-(3:0)**. None of the signals are driven onto the MV bus until the bus has been granted to the MBUS interface.

DRAM

The DRAM consists of three sections, namely DRAM Controller, MV interface, and IOP interface.

DRAM Controller

The DRAM controller supports four configurations of DRAM (4MB, 8MB, 16MB, and 32MB) and two frequency ranges (20/25MHz and 33MHz). The controller is made up of seven PLDs, three of which are configuration dependent. These are shown in Figures 5 and 6 of Appendix A of AN447A/D. Table 4 lists the five non-configuration dependent PLDs and their functions, and Table 5 lists the configuration-dependent PLDs and their functions.

PLD Name	Function
A10	Generates A10 row and column from A24, A3 and A2. The row and column strobes for both the MV bus and IOP bus. The signal DRAM_BUSY.
B_MUX	Byte enable MUX (MV and IOP). IOP data buffer direction and output control.
CAS	Generates CASs for both banks using the byte strobes and CAS control signals from the DRAM state machine. NOTE: a 5ns PLD is required for the 33MHz version.
RAS	RAS generation for both banks. DRAM MV Address latch control. MBUS reset generation from system and IOP controlled reset lines.

Table 4. NON configuration-dependent DRAM PLDs

PLD Name	No. of Banks	Frequency	Description
D_25SM10	One	25MHz	DRAM state machine controlling CAS enables, VME/MBUS (MV) bus output enables and MBUS waits.
D_25SM20	Two	25MHz	As above.
D_33SM10	One	33MHz	As above.
D_33SM20	Two	33MHz	As above.
D_25SMP1	One/Two	25MHz	DRAM state machine controlling termination and MBUS data fetches.
D_33SMP1	One/Two	33MHz	As above.

Table 5. DRAM PLDs selection table for Frequency and Number of banks

The timing generated by the DRAM state machine for the DRAM interface for MBUS, VME, and IOP, for the different configurations is shown in Appendix C of AN447A/D. The DRAM address mapping used for each of the configurations is contained in Appendix D of AN447A/D.

MV Interface

The MBUS/VME DRAM interface, shown in Figure 3 of Appendix A of AN447A/D, consists of address latches and data buffers controlled by the DRAM state machine signals **MV_RAS_OE-**, **MV_CAS_OE-**,and **MV_ADDR_LAT-** for the address latches and **B0_BUFF_OE-**, **B0_BUFF_DIR**, **B1_BUFF_OE-**, and **B1_BUFF_DIR** for the data buffers.

Input/Output Processor (IOP) Interface

The Input/Output Processor interface, shown in Figure 7 of Appendix A of AN447A/D, consists of address and data latches similar to the MBUS interface but are ported directly into the DRAM. The IOP processor uses a 16-bit data bus and could be an MC68340 or MC68302 depending on the I/O requirements. The interface allows for 32-bit word building from the 16-bit IOP data bus, 16-bit straight-through modes, and posted writes. The DRAM controller has control of output from the data latches, via **IOP_DATA_OE-**, and address latches, via **IOP_RAS_OE-** and **IOP_CAS_OE-**, along with latch data into the data latches, via **IOP_DATA_LAT**, allowing for fast turn around of the data.

DRAM/MV ARBITER

The DRAM/MV bus arbiter is constructed in a single PLD **D_ARB**. The arbiter priority is:

1. Refresh
2. IOP
3. VME — Locked out if **HOST_RST** asserted
4. MBUS — Locked out if **HOST_RST** asserted.

The arbiter protocol works on a REQUEST, GRANT, and GRANT ACKNOWLEDGE, with a few exceptions. Tabled below are the controlling signals for each of the requestors.

Signal Name	Function
IOP_REF_DRAM-	Request for refresh cycle
REF_D_BA-	Refresh granted and acknowledged

Table 6. Refresh Arbitration signals

Signal Name	Function
IOP_DRAM-	Request for DRAM access
IOP_D_BA-	Access granted and acknowledged

Table 7. IOP Arbitration signals

Signal Name	Function
V_DRAM-	Request for DRAM access
V_D_BG-	Access granted
V_D_BA-	Access grant acknowledged

Table 8. VME Arbitration signals

Signal Name	Function
M_P_BG-	MV bus is granted to MBUS
M_D_BG-	MV and DRAM access granted
M_P_BA-	MV access grant acknowledged
M_D_BA-	DRAM access grant acknowledged

Table 9. MBUS Arbitration signals

ENHANCEMENTS

The above design was implemented with worst case timing considerations. That is, the PCB characteristics and layout, apart from the clock signals, will have little or no effect on the design. If the PCB layout and characteristics are considered, the design can be speeded up. There is also another way to improve the performance of the two bank version of the design. This consists of replacing the data buffers (74FCT245) fronting the DRAM banks with transceiver latches, like the 74FCT652, and adding another PLD to control them. By doing this, all writes in a burst transaction from the CPU NODE can be posted giving 2-1-1-1. Further, the 33MHz reads would be n-1-1-1.

REFERENCE

1. This Application Note has a companion document, Reference AN447A/D, which gives details of the Schemata, Programmable Logic Devices source code and Timing Diagrams, in the form of Appendices A, B and C. Reference AN447A/D may be obtained from any Motorola Distributor or from the European Literature Centre listed below.
2. For details of MC88100 operation and terminology, see the MC88100 RISC Microprocessor User's Manual. Reference MC88100UM/AD.
3. For details of MC88200 and MBUS operation and terminology, see the MC88200 Cache/Memory Management Unit User's Manual. Reference MC88200UM/AD.
4. For details of the MC88915, see 'Low Skew CMOS PLL Clock Driver' data sheet. Reference MC88915/D.
5. For details of the MC68340's operation, see the MC68340 User's Manual. Reference MC68340UM/AD.
6. For functional details of the MC68302, see the MC68302 User's Manual. Reference MC68302UM/AD.
7. Also see 'An MC68340-based Input/Output Processor' for a description of the MC68340 used as an IOP processor. Reference AN451/D.