AN948

# Data Multiplexing

## Using the Universal Digital Loop Transceiver and the Data Set Interface

### INTRODUCTION

Data multiplexers find applications where clusters of terminals are connected to a central computer and in systems where modems are pooled at a common location. Combining the signals from the various terminals onto one multiplexed data link simplifies wiring and reduces expenses. Sharing the cost of the multiplexer among the several terminals results in a lower net cost compared to installing and maintaining individual cables for each terminal. While present day multiplexers are economical, new ICs from Motorola make possible enhanced performance multiplexers for a fraction of the cost of existing devices.

This Application Note will describe the design of a short-haul multiplexer for asynchronous data at rates up to 9600 baud. The mux combines eight full-duplex data channels along with eight end-to-end RS-232 control signals onto a single pair of telephone wire for distances up to 2 km. Motorola's Universal Digital Loop Transceivers (MC145422/26 UDLTs) master/slave high-speed synchronous data transceivers and Data Set Interface (MC145428 DSI) full-duplex asynchronous to synchronous converter form the heart of this multiplexer. A few MSI CMOS ICs complete the design.

Figure 1 illustrates a typical system with the terminals in a departmental situation multiplexed onto one high-speed data link. RS-232 control signals are passed transparently through the multiplexer so the terminals have direct access to the controls of the modems. This multiplexer system transports one control signal bidirectionally for each data channel. As will be described below, other configurations may easily be constructed with simple wiring changes.

### CHARACTERISTICS OF THE UDLTs

The UDLTs are synchronous data transceivers capable of transporting 80 kbps of full-duplex data over ordinary twisted pair 26 to 19 gauge telephone wire at distances of up to 2 km. These devices utilize a 256 kilobaud MDPSK ping-pong burst modulation technique for transmission. Three logical data channels, one of 64 kbps and two of 8 kbps each are exchanged in bursts of 10 bits every 125 $\mu$s frame. MDPSK timing is shown in Figure 2. The master initiates a ping-pong frame by bursting 10 bits of data to the slave beginning on the rising edge of an externally generated Master Sync Input (MSI). The modulator's analog output signal (LO1, LO2) is shown referenced to MSI. Upon receiving the last bit from the master, the slave responds with a 10 bit burst of its own after a four baud delay. The slave's modulator output (LO1, LO2) is shown referenced to its own Transmit Enable 1 (TE1). Depending on the transmission line characteristics and length, the actual time of arrival of the slave's return burst at the master will vary due to the propagation time of the signal

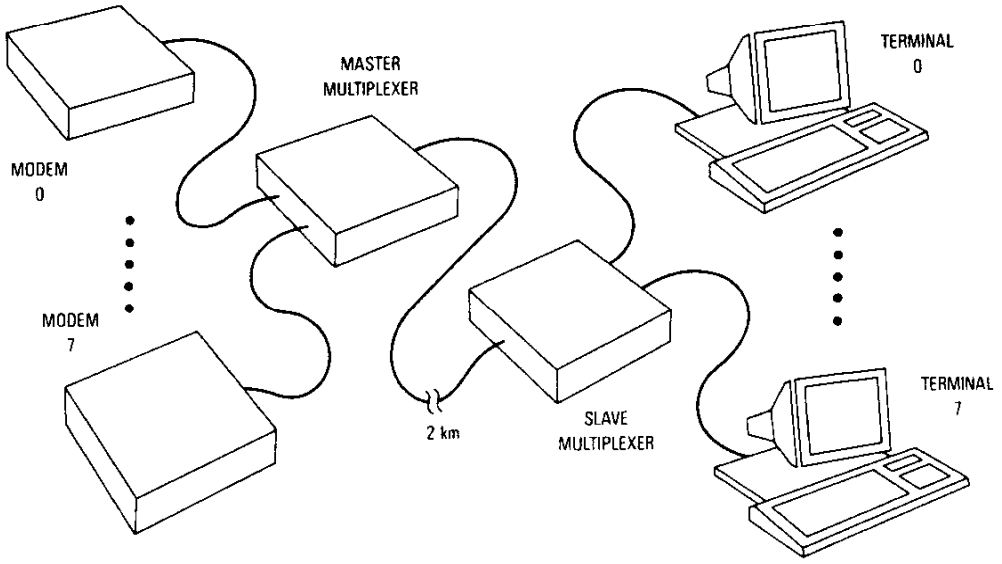



**Figure 1. Typical Multiplexer Application**

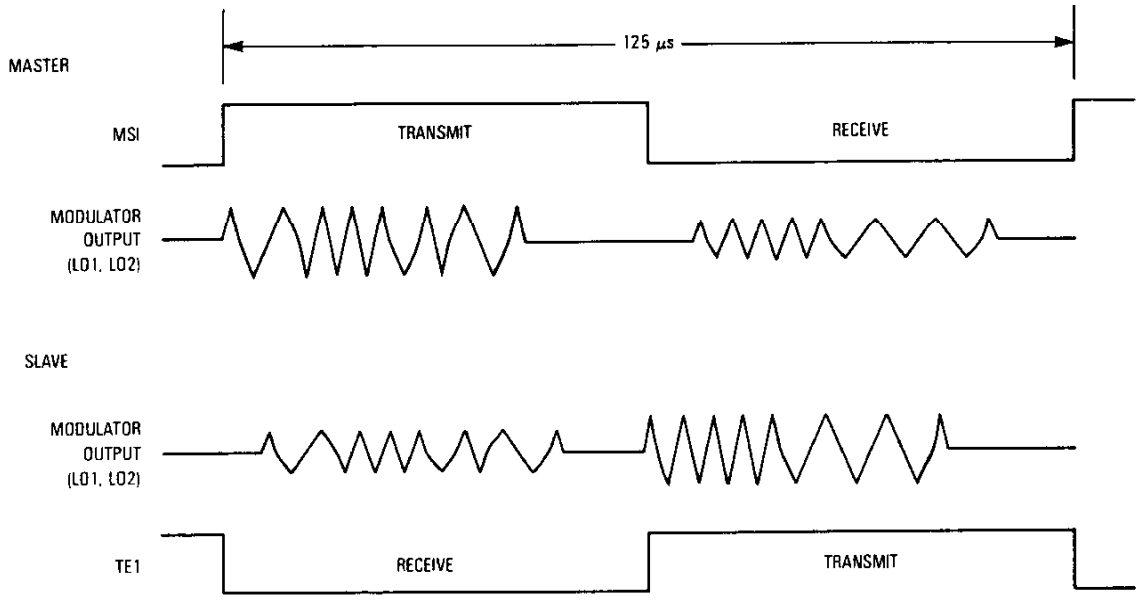



**Figure 2. UDLT Timing**

between UDLTs. On excessively long lines, propagation time down the transmission line results in collisions between the master and slave bursts so maximum line length is limited to 2 km with 26 gauge wire. The slave's TE1 is generated internally upon completion of demodulation of the burst from the master. TE1 remains high for eight data clock (128 kHz) periods and returns low until another burst is received. This process is repeated every 125 μs. Since both master and slave devices exchange data every frame in a half-duplex manner at a 256 kilobaud rate, an effective full-duplex rate of 80 kilobaud is accessible to the user.

The bursts of data on the transmission line use Modified DPSK signals to reduce EMI and susceptibility to crosstalk from other signals in telephone cables. The frequency spectrum consists of peaks at 128 kHz and 256 kHz and their odd harmonics. Only a small amount of energy is present in the frequency bands used by analog telephone service, so UDLT signals may be placed on adjacent pairs in cables with ordinary telephone signals with no degradation of performance. The power spectral density at 76 kHz is approximately 18 dBm and at 28 kHz the level is less than -30 dBm. Because there is no signal energy at very low frequencies, dc energy may be transported on the transmission line to power the remote multiplexer unit. Details of this feature will be described later.

The UDLTs have internal buffers to store and prepare synchronous data for transmission. Eight bits for the 64 kbps channel are serially input and output every 125 μs frame. The two 8 kbps channels each have one bit input and output every frame. The master and slave UDLTs synchronous timing is shown in Figures 3 and 4 respectively. Both figures illustrate the transmit and receive timing for the eight bit words on Tx and Rx, and the timing for the two signalling bits, both inputs (SI1, SI2) and outputs (SO1, SO2).

The master UDLT timing shown in Figure 3 requires external timing signals of 8 kHz for MSI, TE1, RE1, and 64 kHz up to 2.56 MHz may be used for the TDC/RDC pin. This application uses 128 kHz. Eight bits of the 64 kbps data channel received from the slave are output on the Tx pin on the first eight rising edges of TDC/RDC while TE1 is high. Data to be sent to the slave is input on the Rx pin on the first eight falling edges of TDC/RDC while RE1 is high. In this application TE1 and RE1 are connected together so data is input and output simultaneously. Data on the 8 kHz signalling channels are input on SI1 and SI2 pins and output on SO1 and SO2 pins on MSI's rising edge.

The slave UDLT timing (shown in Figure 4) is similar to the master except that the slave synchronizes to the master's bursts and generates its own clocks and enables. The eight bits of the 64 kbps data channel received from the master are presented on the Tx pin on the rising edges of CLK while TE1 is high. Data to be transmitted to the master is loaded in on the Rx pin on the falling edges of CLK while RE1 is high. Signalling bits on the 8 kbps channels to and from the master are input at SI1, SI2 and output at SO1, SO2 on TE1's rising edge.

The master UDLT has pin controlled Power-Down ($\overline{PD}$) and Loop-Back ($\overline{LB}$) features which can be used for system testing. Also available on the master is Signal Insert Enable (SIE) which enables the insertion and extraction of an 8 kbps channel into the LSB of the 64 kbps channel. In this application SIE is unused and held low. The signal enable pin (SE) is a three-state control pin which when held high enables $\overline{PD}$, $\overline{LB}$, and the two signalling bits (SO1 and SO2) allowing these signals to be bussed to a microprocessor.

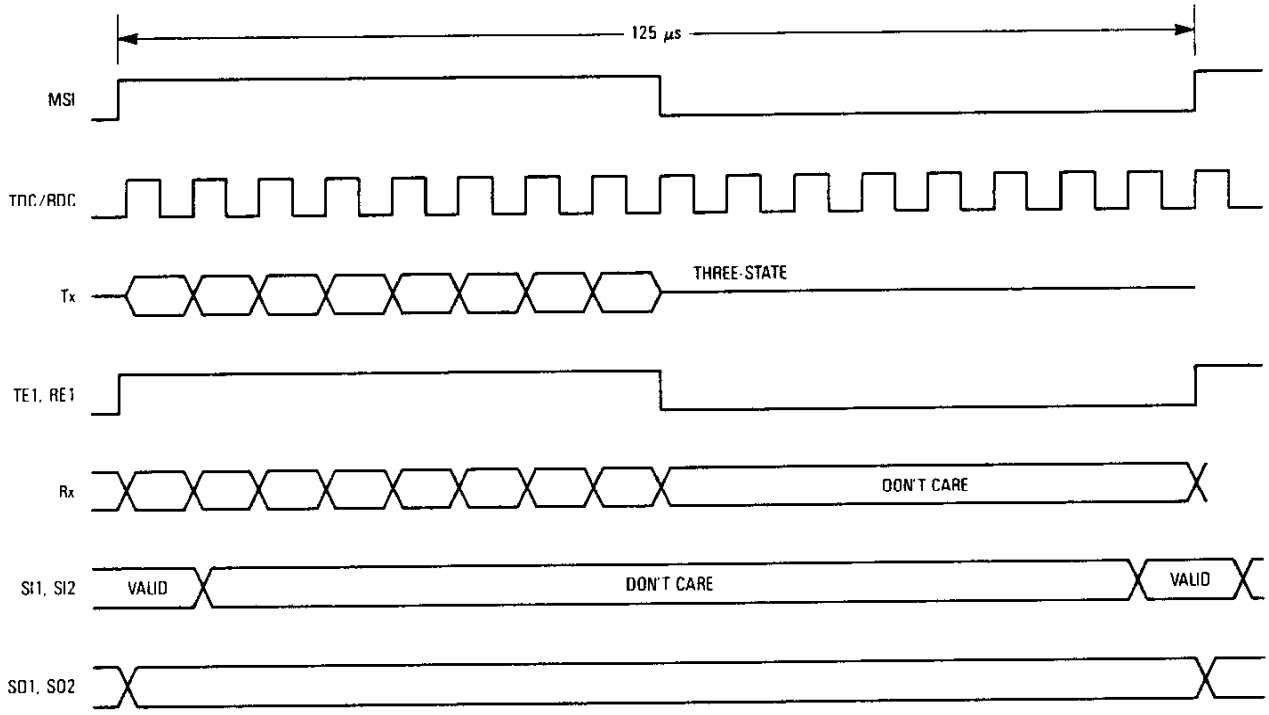



**Figure 3. Master Timing**

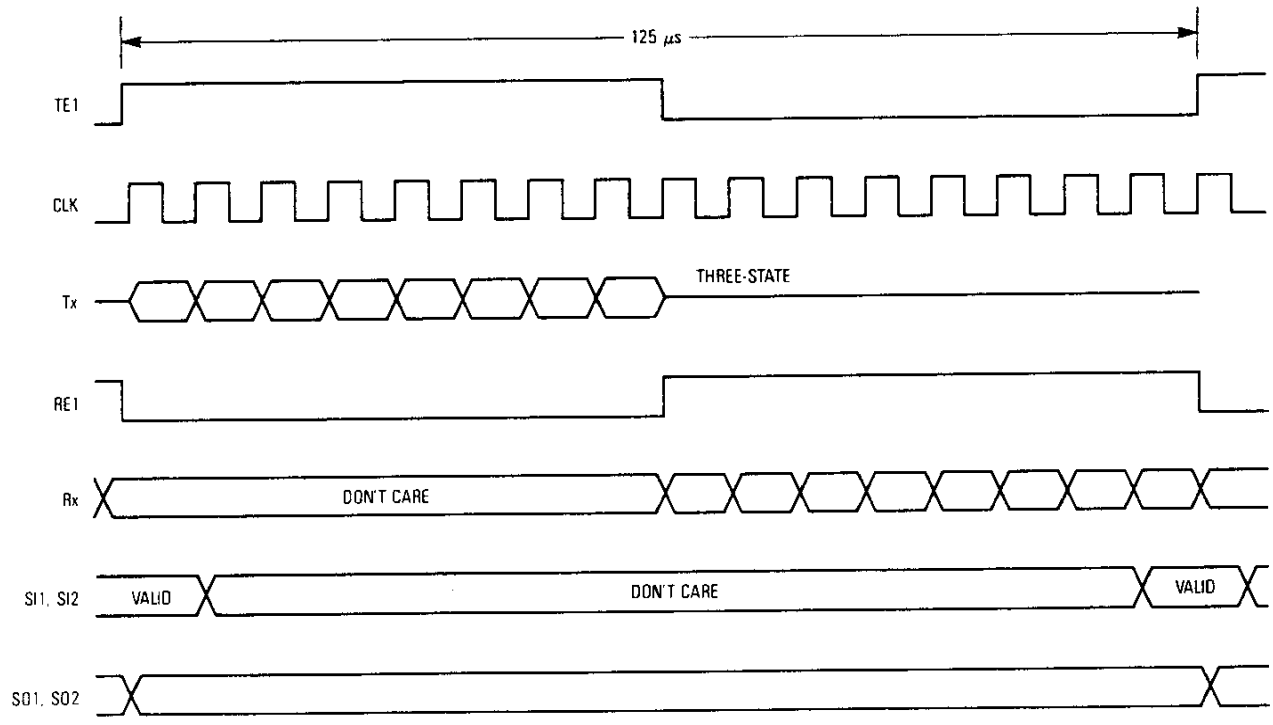
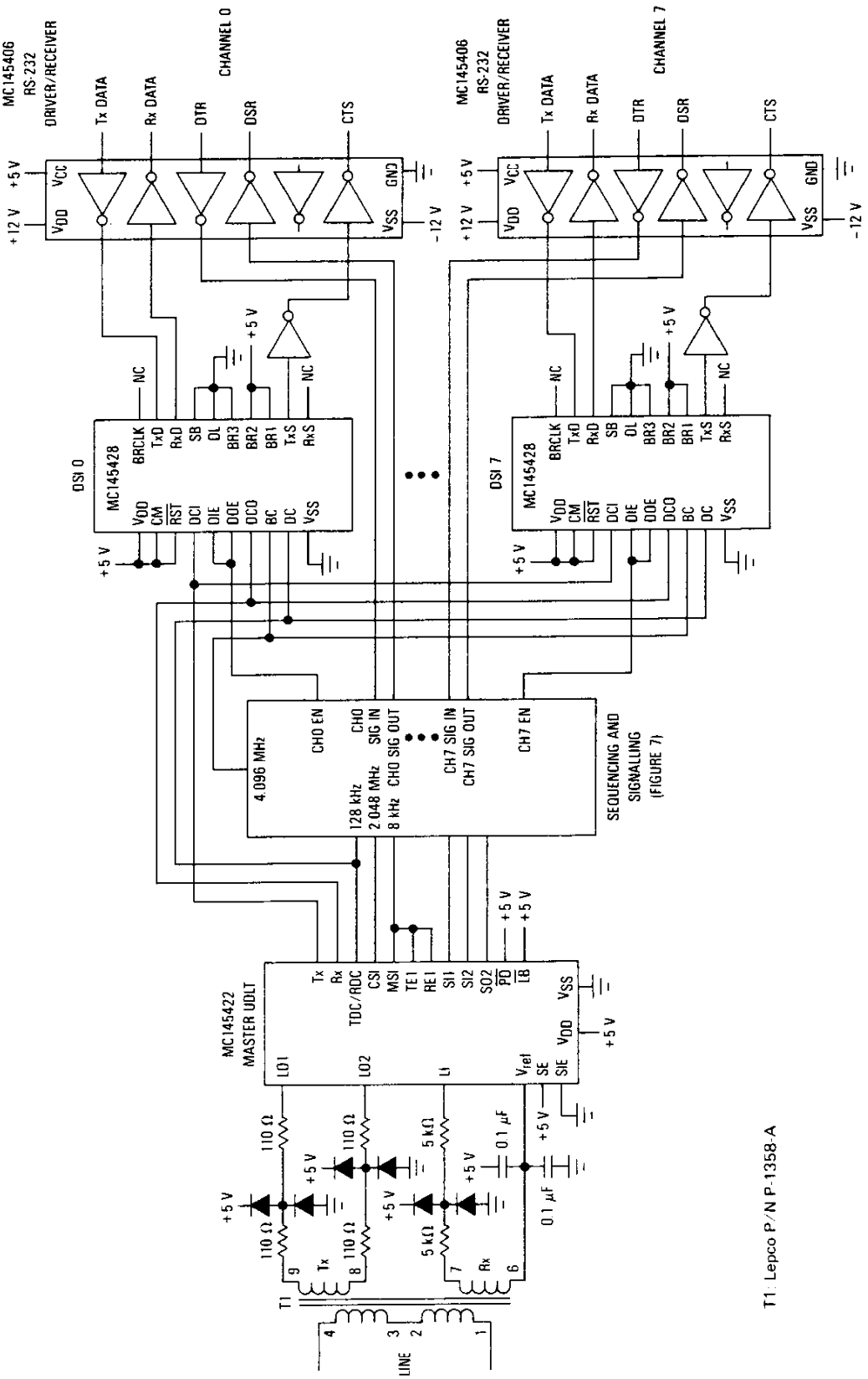
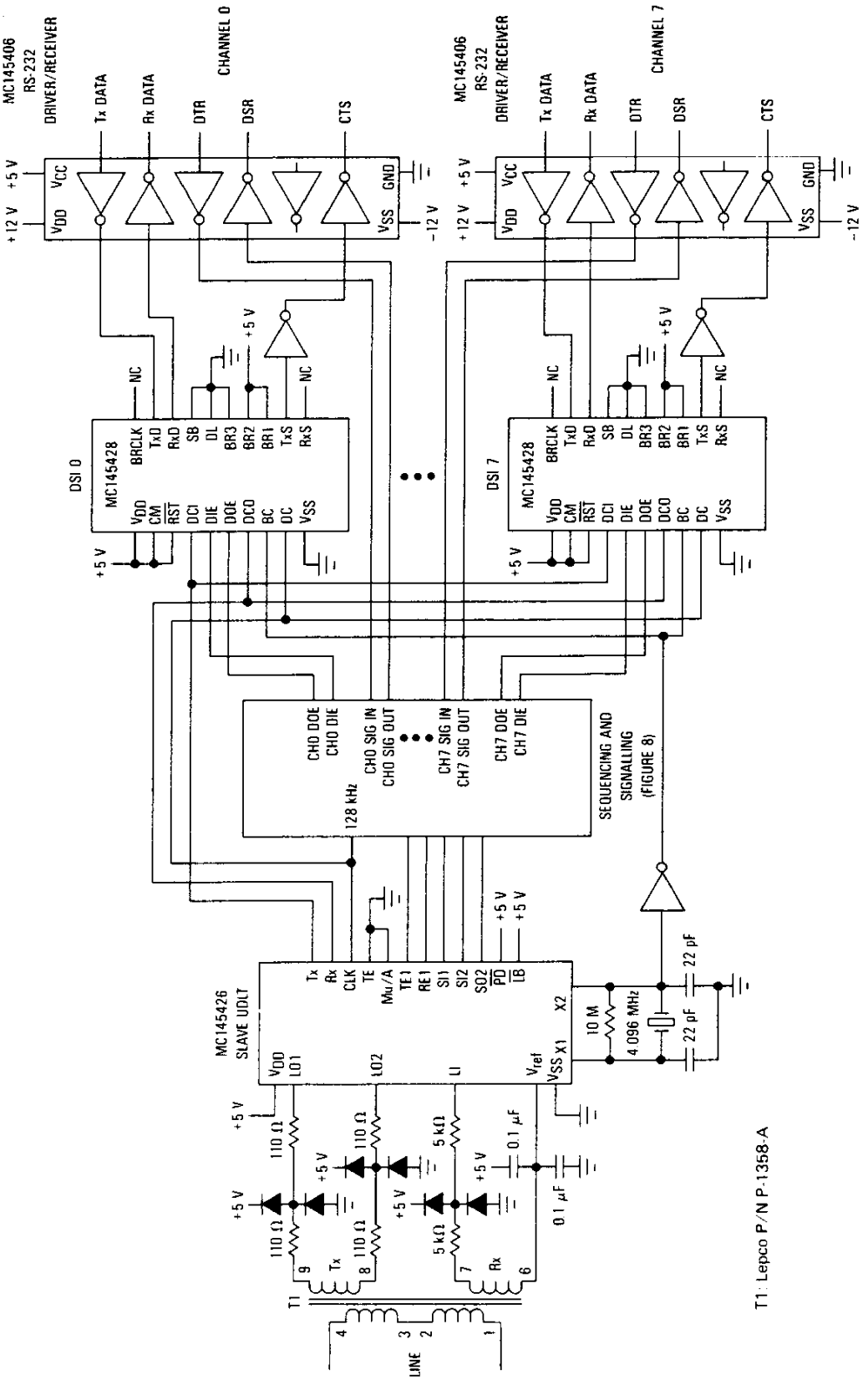



**Figure 4. Slave Timing**




T1: Lepco P/N P-1358-A

**Figure 5. Master Unit Interconnect**




T1: Lepco P/N P-1358-A

**Figure 6. Slave Unit Interconnect**

## TRANSFORMER INTERFACE

The duplexer function, separating transmit and receive bursts on a single twisted pair wire is automatic with UDLTs. The receiver input is blanked while the transmitter is active so the transmitted signal is ignored by the demodulator circuits. The receiver unblanks when the transmitter finishes its burst to search for the return burst from the other end. Automatic duplexer action allows a simple transformer to be used for the interface between the transmission media and UDLTs shown in Figures 5 and 6. The transformer Tx winding and the associated padding network match the transmitter output to the impedance of the transmission line. The Rx winding steps up the signal from the far end to compensate for the loss in the matching network. The characteristic impedance of twisted pair telephone wire in the frequency range used by the UDLTs is approximately 110 ohms. Matching this impedance requires resistors of 220 ohms in each leg of the Tx winding. The impedance of 440 ohms when transformed through a 2:1 turns ratio results in a match to 110 ohms. 12 dB of loss is also introduced. The 12 dB is made up in the Rx winding which has a 4:1 step-up from line to receiver input.

Protection of the UDLTs against transients induced onto the transmission line is accomplished by adding clamp diodes to the padding networks. It is convenient to split the 220 ohm resistors into two 110 ohm resistors and place the clamps at the junction of the resistors. The same technique is used at the receiver inputs.

## CHARACTERISTICS OF THE DSI

The DSI is a device which provides full-duplex asynchronous to synchronous conversion. It allows the user to select asynchronous data formats and baud rates. The synchronous port has selectable timing for easy interfacing to a variety of systems. The asynchronous port characteristics are controlled by the Stop Bit select (SB), Data Length select (DL), Baud Rate select (BR1-BR3) pins. Synchronous data is under the control of the Data Output Enable (DOE), Data Input Enable (DIE), Data Clock (DC), and Clock Mode (CM) pins. Asynchronous data is sampled at 16 times the selected baud rate. Logic circuits search the asynchronous data for a start bit, eight or nine data bits and one or two stop bits. When valid start and stop bits are found, they are removed from the character and the remaining eight or nine data bits are loaded into the transmit FIFO for transmission on the synchronous port. The Tx Status pin goes low when the transmit FIFO is more than half full. This signal may be used for a local Clear-To-Send indication to the data device on the asynchronous port. Special characters are generated and transmitted on the synchronous port to synchronize the receiver of the remote DSI to the character boundaries. At the remote DSI synchronous data is reassembled into eight or nine bit characters, start and stop bits are added and the data is transmitted out on the asynchronous port.

Since start and stop bits are removed from the asynchronous data before transmission on the synchronous port, some data compression is achieved. For example, asynchronous data at 9600 baud with eight data bits and one stop bit is compressed to 7680 baud on the synchronous channel. This makes possible the use of an 8 kbps synchronous channel to transport 9600 baud data. However, since sync and break characters consisting of data patterns 01111110 and 11111110 respectively are exchanged between DSIs every so often, the effective data compression is somewhat reduced. Zero bit insertion on the synchronous data between DSIs is used to eliminate the possibility of data imitating either of these characters (the inserted zeros are removed by the synchronous receiver). The multiplexer allocates the UDLTs 64 kbps synchronous channel to each DSI for one 125 $\mu$s ping-pong frame out of every 1 ms data frame. This results in an 8 kbps synchronous channel for each DSI. Under certain circumstances, with binary data, zero insertion may cause the transmit FIFO to overrun. If hex 'FF' characters are input to the DSI on the asynchronous port at 9600 baud with minimum time between characters, inserted zeros and sync characters cause the effective data rate to increase from 7680 baud to approximately 9400 baud. Since the synchronous channel supports only 8 kilobaud, an overrun of the Tx FIFO will occur. The TxS pin will go low approximately 5 ms before an overrun occurs and this indication may be used to stop the flow of new asynchronous data until the FIFO clears out. When ASCII data is used, only 6 characters (>(3E hex), ?(3F hex), |(7C hex), ~(7E hex), DEL(7F hex), and Blank(7D hex)) generate stuffed zeros. Fortunately, it is unlikely that these characters will be sent in large enough groups to cause FIFO overruns. In applications where ASCII data is transported, eight 9600 baud channels may be multiplexed onto this system's 64 kbps synchronous channel. If binary data is transported, a 16 kbps synchronous channel must be allocated for each DSI, resulting in a four channel multiplexer. This guarantees that even with maximum zero insertions, FIFO overruns will not occur.

## OCTAL MULTIPLEXER SYSTEM DESCRIPTION

This multiplexer system fully exploits the DSI chips and the UDLT transceiver pair. The UDLTs 64 kbps channel transports the synchronous data from the DSIs. One of the UDLTs 8 kbps channels is used to synchronize the multiplexing of the eight data channels, and the other 8 kbps channel is used to transport eight RS-232 control signals.

The multiplexer system consists of two units, a master and a slave. Figure 5 illustrates the interconnection of the various devices within the master unit. The transformer interface to the twisted pair is shown with the previously described impedance matching and protection circuitry. The master UDLT is shown with the Tx, Rx lines along with the 128 kHz and the 4.096 MHz clocks bussed to the eight DSIs. The data channel enables and signalling lines are shown connecting the DSIs and the RS-232 driver/receivers to the sequencing and signalling block. Each DSI is shown configured for 9600 baud with eight bit character lengths and one stop bit which may be made switch selectable, if desired.

Figure 6 shows the complementing slave unit. Protection circuitry and the transformer interface are the same as the master unit. The slave UDLT generates its own clocks derived from an on-chip crystal oscillator circuit. An inverter is used to drive the eight clock inputs to the DSIs. Also shown is the sequencing and signalling interconnect to the DSIs and the RS-232 driver/receivers.

Circuitry in the sequencing and signalling blocks is shown in Figures 7 and 8 for the master and slave units respectively. All pertinent timing of the multiplexer system is shown in Figure 9. Master timing is shown in the top section, master and slave bursts on the twisted pair are shown on the line

labeled 'Transmission Line'. Slave timing is illustrated on the bottom half of the figure.

Clocks for the master UDLT are created by a 12-stage ripple counter (MC74HC4040) which is driven by a 4.096 MHz crystal oscillator. Taps at Q1, Q5, and Q9 create the 2.048 MHz (CCI), 128 kHz (TDC/RDC) and 8 kHz (MSI,TE1,RE1) clocks respectively. Inverters are needed on each line so the rising edges coincide. A pulse which synchronizes the master and slave data channel sequencing circuitry is generated when a count of 0 is reached by Q10, Q11, and Q12 of the ripple counter. This pulse is shifted through the enable shift register (MC14015B) to create eight non-overlapping enables for the DSIs. A latch (MC14013B) is used to delay the pulse so that it can be properly input into SI1 of the UDLT on the next rising edge of MSI. The delayed pulse on SI1 and the data channel enables (CH0-CH7 DOE, DIE) are shown on the timing diagram. RS-232 control data is routed to a latch by an addressable data selector (MC14051B). RS-232 control data received from the slave unit is written into an addressable latch (MC14051B). Notice that the first Q0 of the shift register is the enable to the DSI of data channel 1. Since the sync pulse arrives at the input of the shift register slightly after the clock, a one-channel offset is used to address the proper channel. This offset is transparent to the system.

Data input on the Rx pin of the UDLT is buffered until the next rising edge of MSI, when it is burst out on the transmission line. Data on SI1 and SI2 are latched in on the rising edge of MSI and transmitted in the burst which was initiated by that MSI edge. The bursts from the master (boxes with M) and the return bursts from the slave (boxes with S) on the twisted pair wire are illustrated on the 'Transmission Line'. The numbers indicate which channel's data is transported in that burst.

The system sync pulse arrives at the slave unit on the SO1 pin of the UDLT (Figure 8). It is shifted through a shift register (MC14015B) which is clocked by the RE1 pin. The Q's from this shift register enable the transmission of data from the DSIs to the UDLT. The sync pulse is delayed and shifted through another shift register clocked by TE1. The Q's from this shift register enable the DSIs to accept data from the UDLT. RS-232 control data is handled in the slave unit in a similar manner as the master with a data selector and an addressable latch. Simply offsetting the connections to the RS-232 driver/receivers realigns the data to the proper

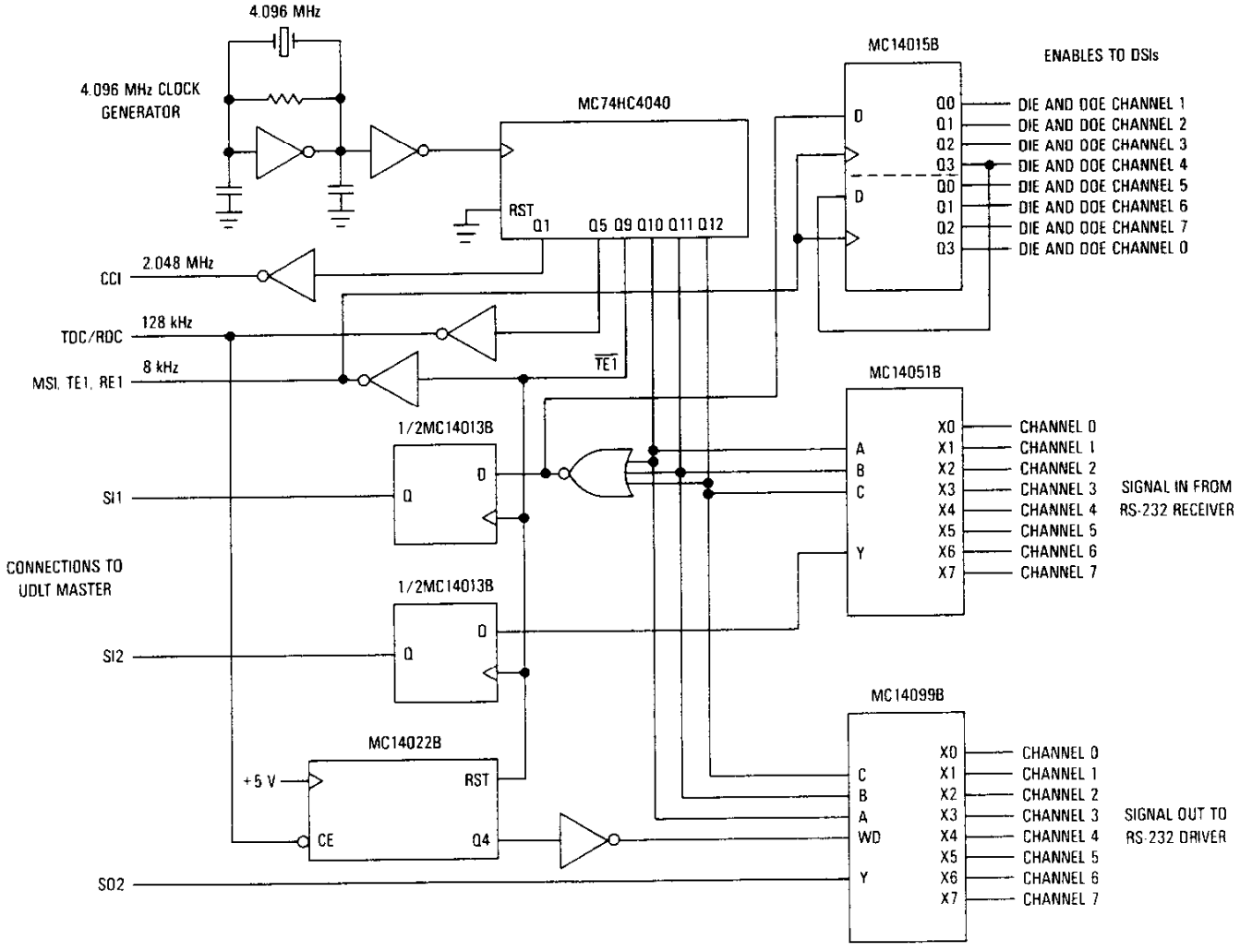



**Figure 7. Master Sequencing and Signalling**

channels eliminating any superfluous circuitry. Offsetting the connections to the data selector (MC14051B) similarly aligns the channels so that the data arrives at the master in the correct time slot. Following the channels on the timing diagram illustrates the concept.

## ADDITIONAL CONSIDERATIONS

This multiplexer design is quite modular. If RS-232 control signalling is not desired then the circuitry can be simplified by removing the write pulse generator (MC14022B), addressable latches (MC14099B) and data selectors (MC14051B) from both units. The address generator (MC14163B) on the slave unit may also be removed. In applications where data rates of less than 9600 baud are used, the Baud Rate select pins on the DSIs need simply be reconfigured. A DIP switch can be conveniently used to set the Baud Rate, Data Length and Stop Bit pins on the DSIs. Note that the DSIs must not be set for 19.2 or 38.4 kilobaud when eight channels are multiplexed. If data rates higher than 9600 baud are desired, the individual data channels must be serviced more often by the UDLT. Because the high-speed synchronous channel between UDLTs is 64 kbps, the total bandwidth required by all of the channels must be at or below 64 kbps. The multiplexer may also be converted into a single channel limited-distance modem where data rates of up to 56 kbps can be attained.

This multiplexer, because it is all CMOS, consumes only about 175 mW per unit. One of the units may be powered by dc energy transported on the transmission line itself eliminating a power cord. The line interface transformer is designed to pass dc energy by separating the two line windings and installing a 1 $\mu$F capacitor between pins 2 and 3. Now, dc current may be passed to the twisted pair. A switching power supply may be installed in the remote unit to convert the line power to voltage levels useable by the digital circuitry. Recall that the dc resistance of 2 km of 26 AWG wire is approximately 575 ohms. This necessitates a relatively high voltage on the sending side to keep the $I^2R$ losses in the twisted pair to a tolerable level. Usually 36 to 40 volts is satisfactory to furnish enough voltage to the remote unit. Since the transmission line is balanced, there is no ground reference between master and slave units. dc power to the twisted pair must be fed from an isolated winding on the mains transformer, so that a ground reference may be established at the remote unit. Connecting the ground references of the two units through the twisted pair will result in poor data performance due to longitudinal currents in the line.

### References

Motorola Telecommunications Device Data Book DL136, 1984.

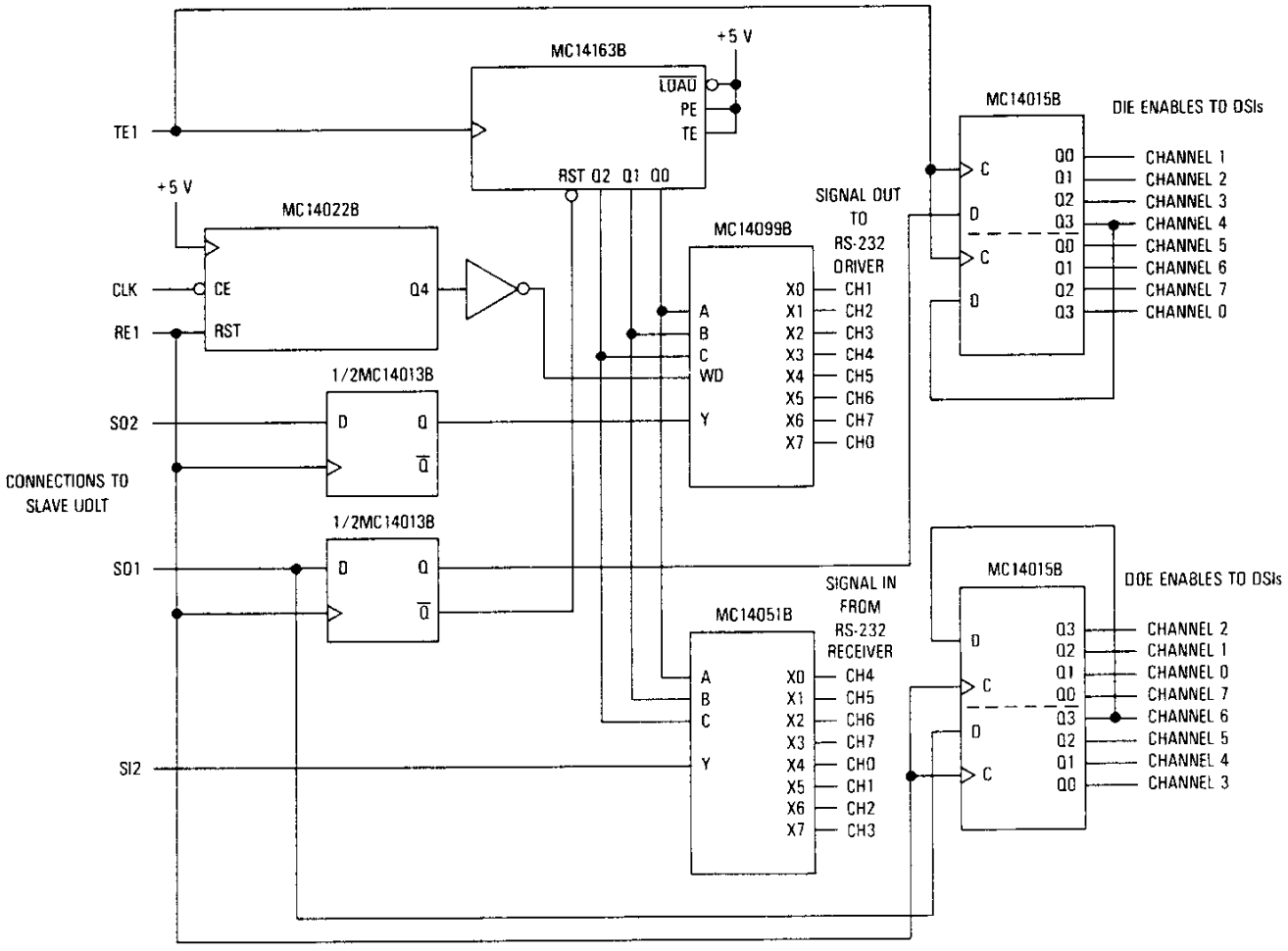



**Figure 8. Slave Sequencing and Signalling**

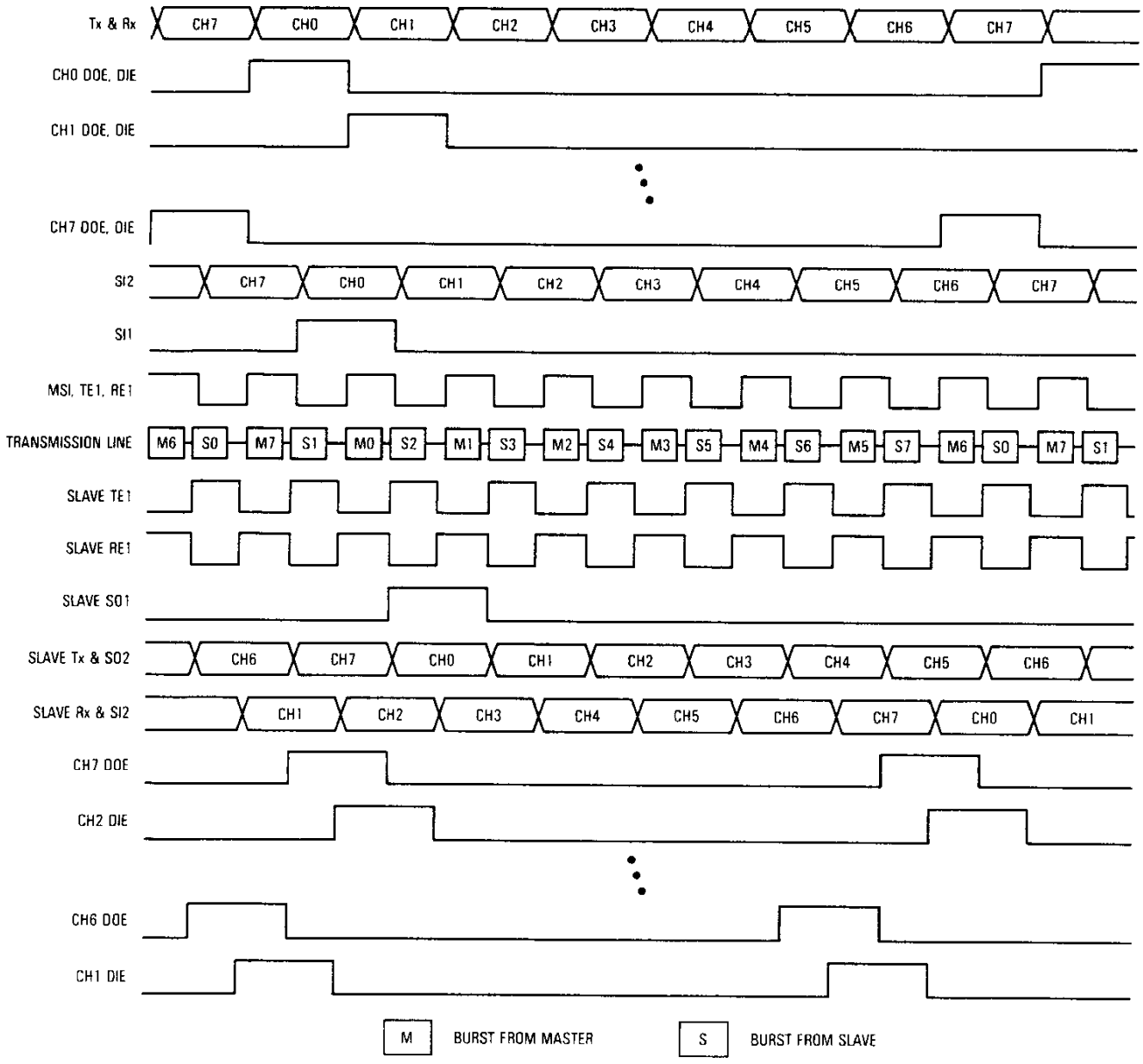



**Figure 9. System Timing**

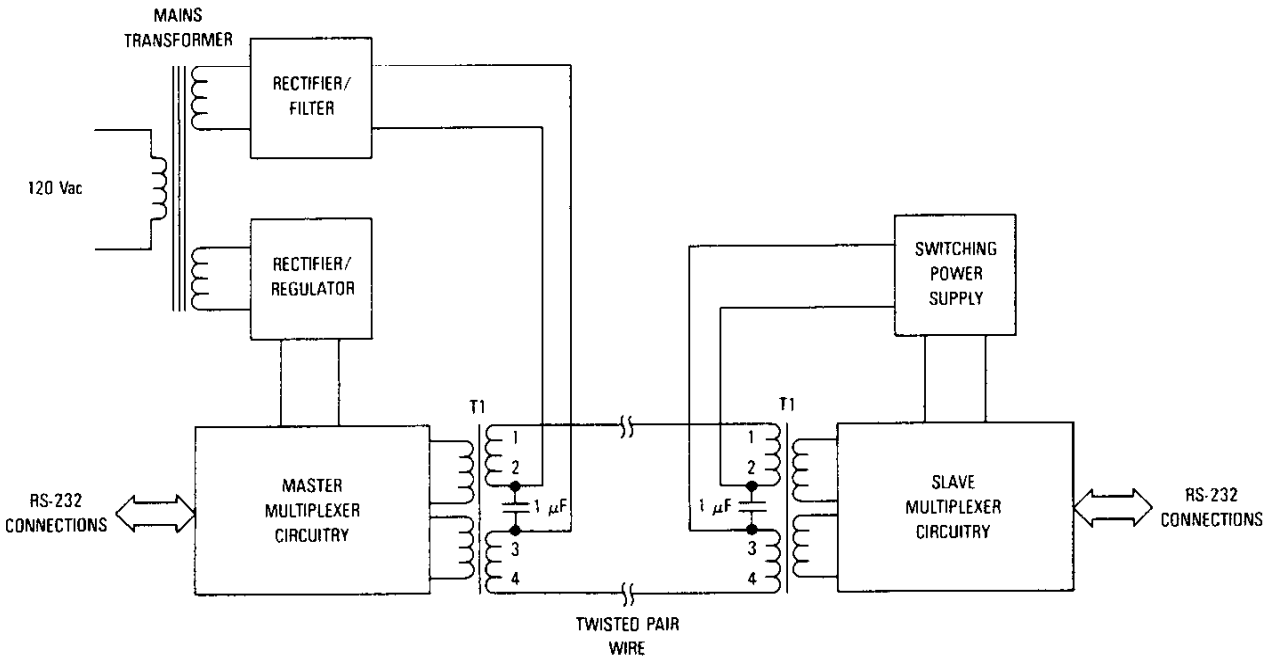



**Figure 10. Powering Slave Unit From the Twisted Pair**



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