MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

Order this document
by AN981/D

AN981

Building Counters with Motorola's Macrocell Arrays

Prepared by Bill Blood
Application Specific Integrated Circuits Division, Chandler, AZ

INTRODUCTION

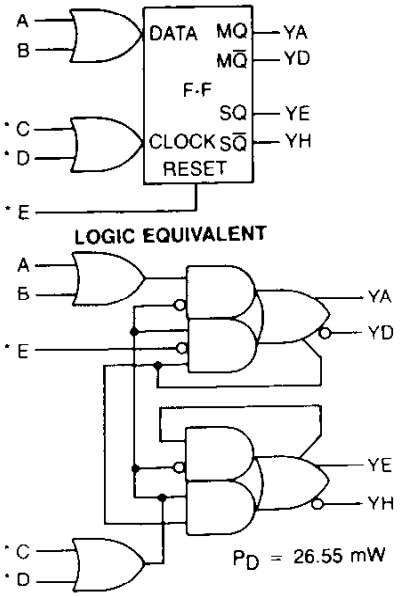
Counter circuits are one of the most commonly used logic blocks. For years, design engineers could go to a logic data book and select suitable counters such as the MC10H136 in ECL, 74LS161A in TTL, or MC14161B in CMOS. The movement to ASIC (Application Specific Integrated Circuits) has recreated the need to design efficient counter circuits. Engineers developing part types on semicustom arrays often have to build counters out of flip-flops and gates. This article examines techniques for building counters out of ASIC library elements. Various counter structures are covered including binary counters, BCD counters, programmable counters, up-down counters, ring counters, and dual modulus prescalers.

BASIC COUNTERS

D type flip-flops are the basic counter storage elements. Figure 1 shows the data sheet information for M291, a basic flip-flop in Motorola's MCA800ECL and MCA2500ECL macrocell array library. M291 features high speed (400 MHz worst-case toggle rates), gated CLOCK and DATA inputs, and both master and slave outputs. Master outputs are provided for specialized applications and are not used in the following counter designs.

Many possible counter output sequence patterns exist, with straight binary being the most common. The number of counts before the output pattern repeats is controlled by the number of flip-flops in the counter. The maximum count is 2 to the N power, with N being the number of flip-flops. A 4-bit binary counter would count

M291 — ½ CELL
D FLIP-FLOP W/RESET



TRUTH TABLE

RESET	DATA	CLOCK	MASTER Q	SLAVE Q
E	A+B	C+D	YA	YE
L	X	H	—	—
L	L	L	L	—
L	L	L→H	L	L
L	H	L	H	—
L	H	L→H	H	H
H	X	H	L	L
H	L	L	L	—
H	L	L→H	L	L
H	H	L	H	—
H	H	L→H	L	⌐

YD = $\overline{YA}$
YH = $\overline{YE}$

t_{d+}(A,B TO YA,YD) = 475 ps
t_{d-}(A,B TO YA,YD) = 575 ps
t_{d+}*(C,D TO YA,YD) = 575 ps
t_{d-}*(C,D TO YA,YD) = 800 ps
t_{d+}*(C,D TO YE,YH) = 525 ps
t_{d-}*(C,D TO YE,YH) = 600 ps
t_{d}*(E TO YA,YD) = 825 ps
t_{d}*(E TO YE,YH) = 1450 ps

SETUP TIME = 750 ps
HOLD TIME = 0.0 ps
MIN CLOCK PERIOD = 2500 ps
MIN POS CLOCK WIDTH = 1250 ps
MIN NEG CLOCK WIDTH = 1250 ps
MIN RESET PULSE WIDTH = 1350 ps

MIN RESET PULSE WIDTH = 2175 ps
IF E AND (C OR D)
ARE TIED TOGETHER

Figure 1. M291 is a High Speed Flip-Flop in Motorola's MCA II ECL Macrocell Array Library. A Lower Power, Lower Speed Version of the Same Macro is Available in the MCA II TTL Compatible Macrocell Array Library.

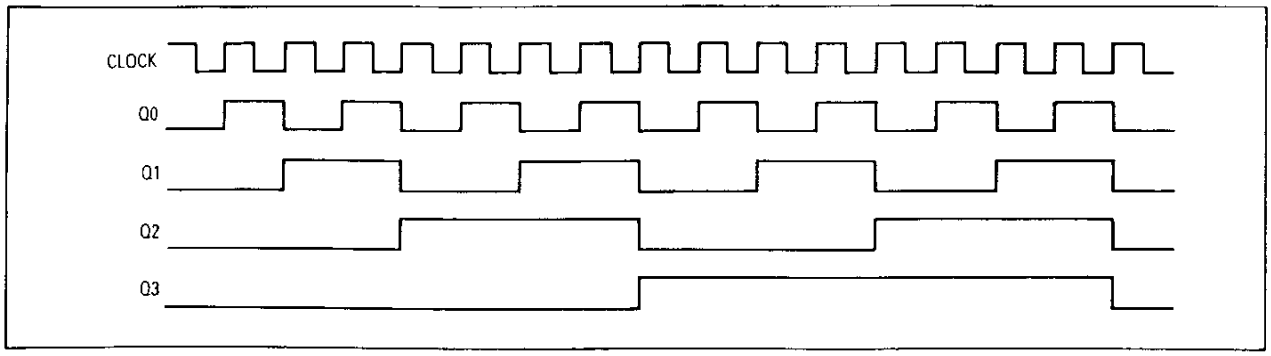


Figure 2. Clock and Output Waveforms Show the Count Sequence for a 4-Bit Divide by 16 Binary Counter.

0 to 15 and have waveforms as shown in Figure 2. Counter outputs can be expressed by the truth table in Figure 3.

The simplest frequency divider circuit is the ripple counter shown in Figure 4, where the output of one flip-flop drives the clock input of the next. This circuit has two advantages, speed and simplicity. Speed is limited by the toggle rate of the first flip-flop which would be 400 MHz for M291 or up to 770 MHz for faster flip-flops such as M376, also available in the MCA II ECL macrocell array library. No logic element is needed other than flip-flops and the circuit is easily expanded by adding additional flip-flops.

Ripple counters have a serious limitation for many applications because the flip-flops change state sequentially, rather than simultaneously. If the application requires decoding a particular count pattern, then performance is compromised by having to wait for the last stage to settle. Synchronous counters avoid the problem by having a clock line that is common to all flip-flops. Synchronous counters do require some gating logic and are more complex to design. One technique is to determine the logic signals that must be present on each flip-flop D input prior to the clock signal. Referring to Figure 3, the following D inputs will give the desired binary pattern.

$D0 = \overline{Q0}$
$D1 = Q1 \oplus Q0$
$D2 = Q2 \oplus Q0 \bullet Q1$
$D3 = Q3 \oplus Q0 \bullet Q1 \bullet Q2$

Count #	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

Figure 3. A Truth Table Shows the Patterns That Must Be Present on Flip-Flop D Inputs Prior to the Active Going Clock Edge.

A synchronous counter could be implemented as shown in Figure 5, or with macrocell library functions as shown in Figure 6. Notice the RESET line in Figure 6. It is a good ASIC design practice to provide a means such as reset to initialize all flip-flops after power up. Proper initialization will minimize any problems with circuit simulation during design or with circuit test during manufacturing. M291 has a clock gated reset that can be con-

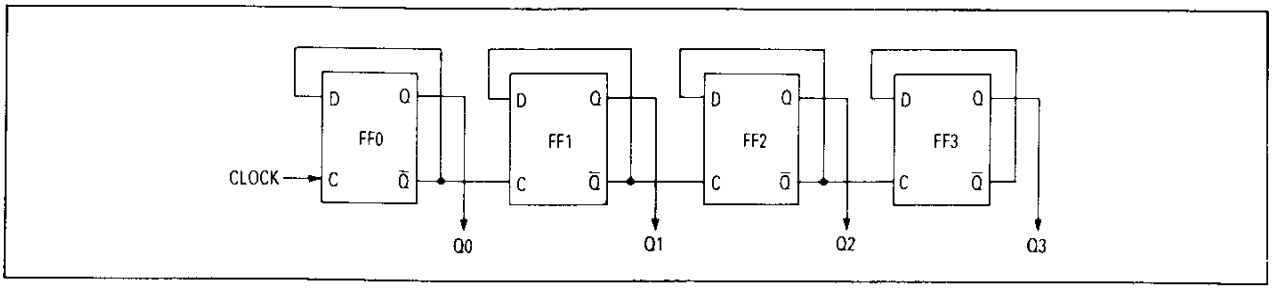


Figure 4. Ripple Counters Are Constructed by Operating Flip-Flops in a Toggle Mode with the Q Bar Outputs Fed Back to the Flip-Flop D Inputs. Most MCA Flip-Flops Trigger on the Positive Going Clock Edge. Q Bar Outputs Connected to the Following Clock Inputs Result in a Count Up Sequence.

verted into a full asynchronous reset by connecting the reset signal to both reset and the extra clock input.

BCD counters provide another common count sequence. Rather than counting in a binary sequence to 15, BCD counters count in a decimal pattern with four flip-flops counting 0 to 9. The BCD truth table is shown in Figure 7. BCD counters are designed in the same manner as binary, except the logic equations to flip-flop D inputs are modified as shown below.

$D0 = \overline{Q0}$

$D1 = Q1 \oplus Q0 \bullet \overline{Q3}$

$D2 = Q2 \oplus Q0 \bullet Q1$

$D3 = (\overline{Q3} \bullet Q0 \bullet Q1 \bullet Q2) + (Q3 \bullet \overline{Q0} \bullet \overline{Q1} \bullet \overline{Q2})$

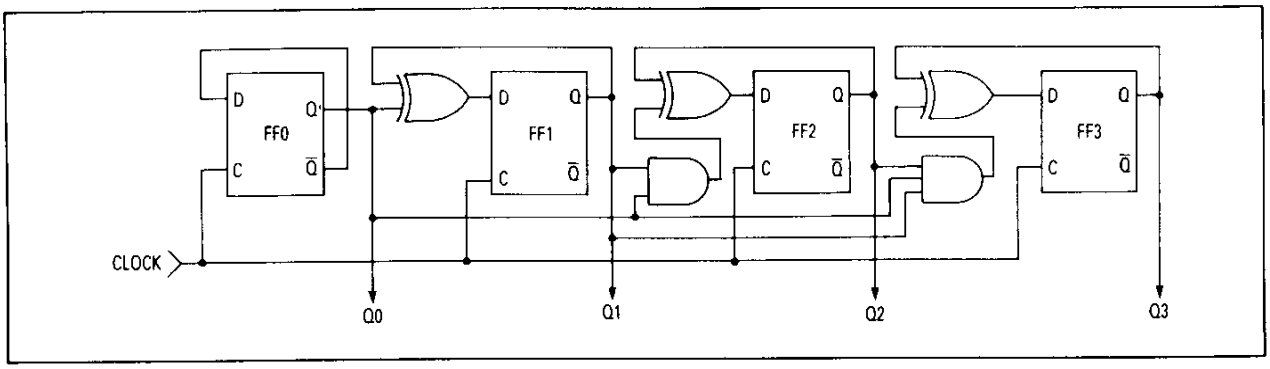


Figure 5. Synchronous Counters Provide Simultaneous Outputs from all Flip-Flop Stages. Gating on the Flip-Flop D Inputs Generates the Proper Count Pattern.

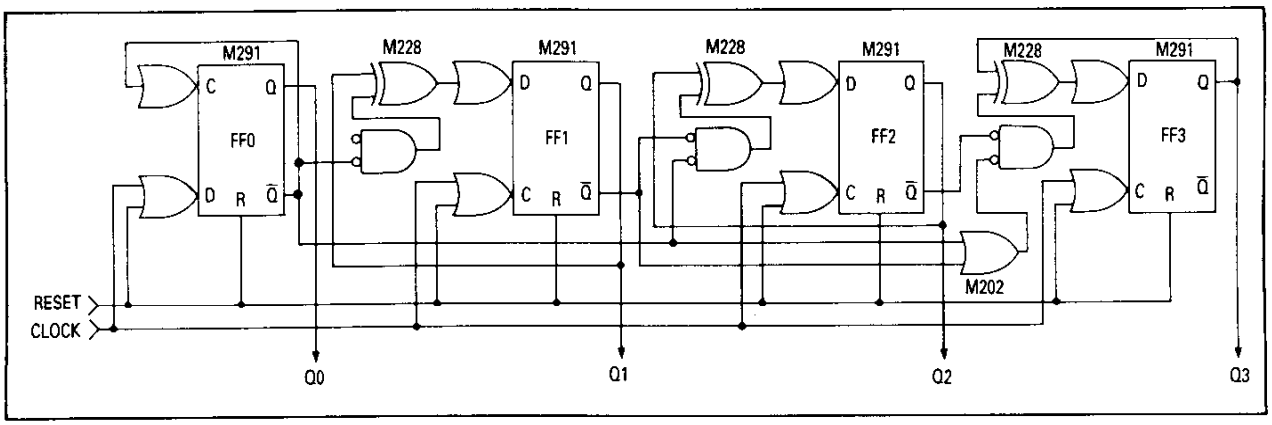


Figure 6. A Synchronous Binary Counter Implemented with MCA II Library Macrocell Functions.

Count #	Q3	Q2	Q1	Q0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	0	0	0	0

Figure 7. The BCD Counter Truth Table Shows Patterns That Must Be Present on Flip-Flop D Inputs Prior to the Active Going Clock Edge.

A BCD counter can be implemented with macrocell library functions as shown in Figure 8.

The BCD counter has six unused binary states, 10 through 15. It is important when developing any counter that uses less than the full binary count pattern to make sure unused states do not lock up the counter. Normally the counter will not see the unused states, but a power supply spike or other transient condition could false trigger a flip-flop. The counter should return to a normal count sequence from any possible binary bit combination. Figure 9 shows the complete count pattern for the BCD counter in Figure 8. All non-BCD binary numbers lead to the normal BCD loop.

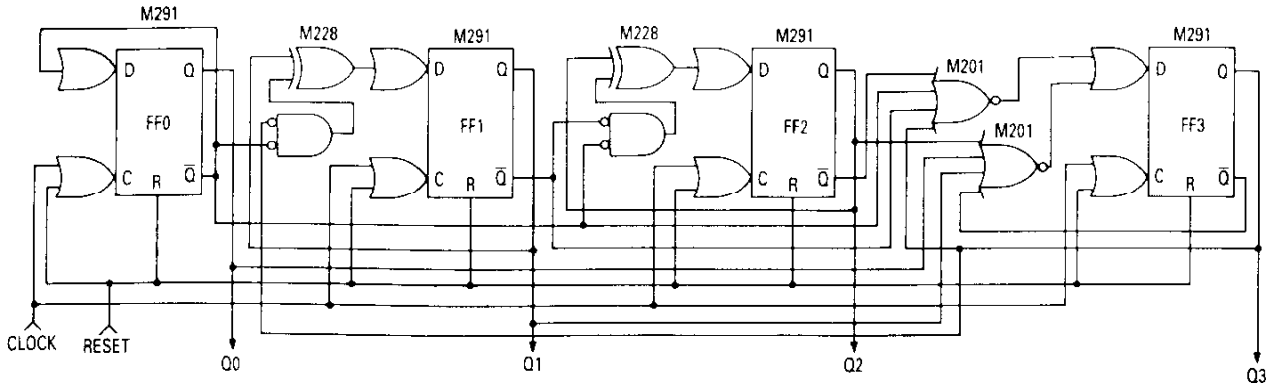


Figure 8. A Synchronous BCD Counter Implemented with MCA II Library Macros. Feedback Gating on the Flip-Flop D Inputs Generates the Proper BCD Count Sequence.

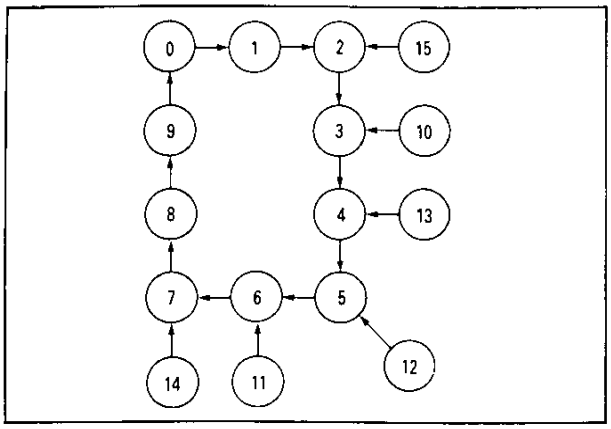


Figure 9. The Complete Counter Flow Diagram Shows a Normal BCD Count Pattern, Along with All Non-BCD Binary Numbers Feeding into the BCD Count Sequence.

PARALLEL LOAD COUNTERS

Presetting a counter by parallel loading a number is an important feature that can be added to the basic counter circuit. Parallel loading is accomplished by adding a 2 to 1 multiplexer in front of each flip-flop D input as shown for the binary counter in Figure 10. A single select line controls one of two operating modes. When the select line is a Logic "0," the circuit clocks in information from the parallel load P input lines. When the select line is a Logic "1," the circuit functions as a binary counter. Macrocell M292 in the Motorola MCA II library includes the multiplexer as part of the flip-flop. This simplifies building parallel load counters and minimizes delay times through the multiplexer.

Programmable counters are a special form of parallel load counters. They divide by a variable ratio as selected from a number on the parallel load inputs. Generally the counters are operated by parallel loading a number, then counting until a terminal number is reached. At that time the count number is reloaded and

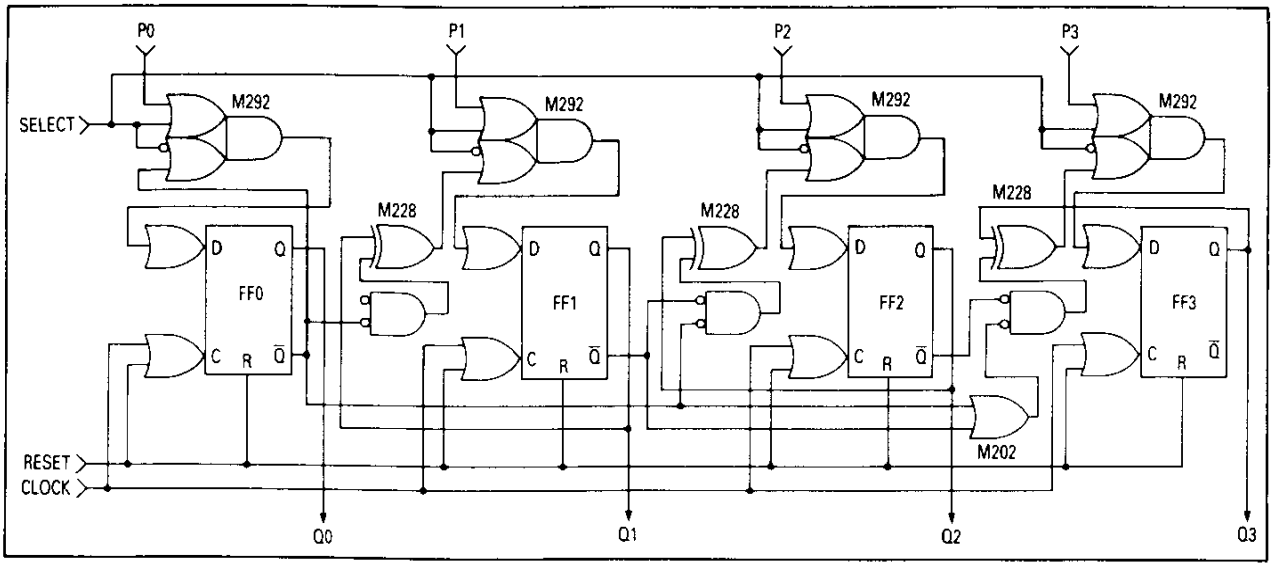


Figure 10. Multiplexers in Front of the Flip-Flop D Inputs Allow Selecting Between Parallel Load and Binary Counting. The Design Features a Synchronous Parallel Load Where Data on the P Inputs Enters the Counter on a Positive Going Clock Edge.

the sequence repeats. A problem occurs when the programmable counter operates in a count up sequence. The correct divide-by-number can only be achieved if the number placed on the parallel load inputs is a one's complement of the desired count number. This inconvenience is easily fixed by operating the programmable counter in a count down mode. Count down allows the true value of the number to be placed on parallel load inputs. After parallel loading, the circuit counts down until a terminal count value of 1 is reached. At terminal count, the parallel inputs are reloaded and the sequence continues. Figure 11 shows the macrocell logic for a 4-bit binary programmable counter. The count number is controlled by the binary value placed on P inputs. Count down is accomplished by changing logic equations to the flip-flop D inputs. Note: the circuit shown in Figure 11 does not give an output for divide-by-1. If needed, divide-by-1 can be achieved by gating TERMINAL COUNT and CLOCK with a 2-input OR gate.

Larger counter circuits can be built by increasing the number of flip-flops. However, for longer synchronous counters it can become difficult to control the number of terms that must be handled by D input logic gates. The problem is solved by periodically combining terms with intermediate stage gates. This technique is illustrated with M201 OR gates in the Figure 12 8-bit synchronous binary up counter. Synchronous counters can be extended to any reasonable length with the intermediate gates. Notice the logic required to combine terms will increase propagation delays between flip-flop outputs and the following D inputs, resulting in an associated decrease in maximum clock speed.

STANDARD COUNTER CIRCUITS

In some cases a person designing the logic for an ASIC array would like to duplicate a commercially available counter circuit. Some of the more popular counters are the 74LS161A, 74LS160A, 74LS169A, and the 74LS168A. The 74LS161A is a 4-bit binary presettable counter with inputs and outputs for cascading to longer counter chains. 74LS160A operates in a similar manner, but with a BCD count pattern. The 74LS169A is a more sophisticated 4-bit up/down binary presettable counter. 74LS168A also performs both count up and count down, but with a BCD pattern. Macrocell implementation of these four counters are shown in Figures 13, 14, 15, and 16.

Building standard integrated circuit logic parts out of macrocells has the advantage of designing with a known circuit function. It also simplifies any breadboarding. However, both counter performance and circuit density can generally be improved by custom designing the counter circuit for a specific application.

SPECIAL PURPOSE COUNTERS

Ring counters are formed by connecting flip-flops into a shift register, with the count number controlled by the number of flip-flops and by feedback paths. Advantages of the ring counter are high speed operation and simplicity, while disadvantages include a non-binary count pattern that may be difficult to decode, and extra flip-flops for larger count numbers. Figure 17 shows five ring counters with divide ratios of 3 through 7. Notice the divide-by-3, 5, and 7 counters take advantage of the flip-flop gated D inputs. An alternative design technique for

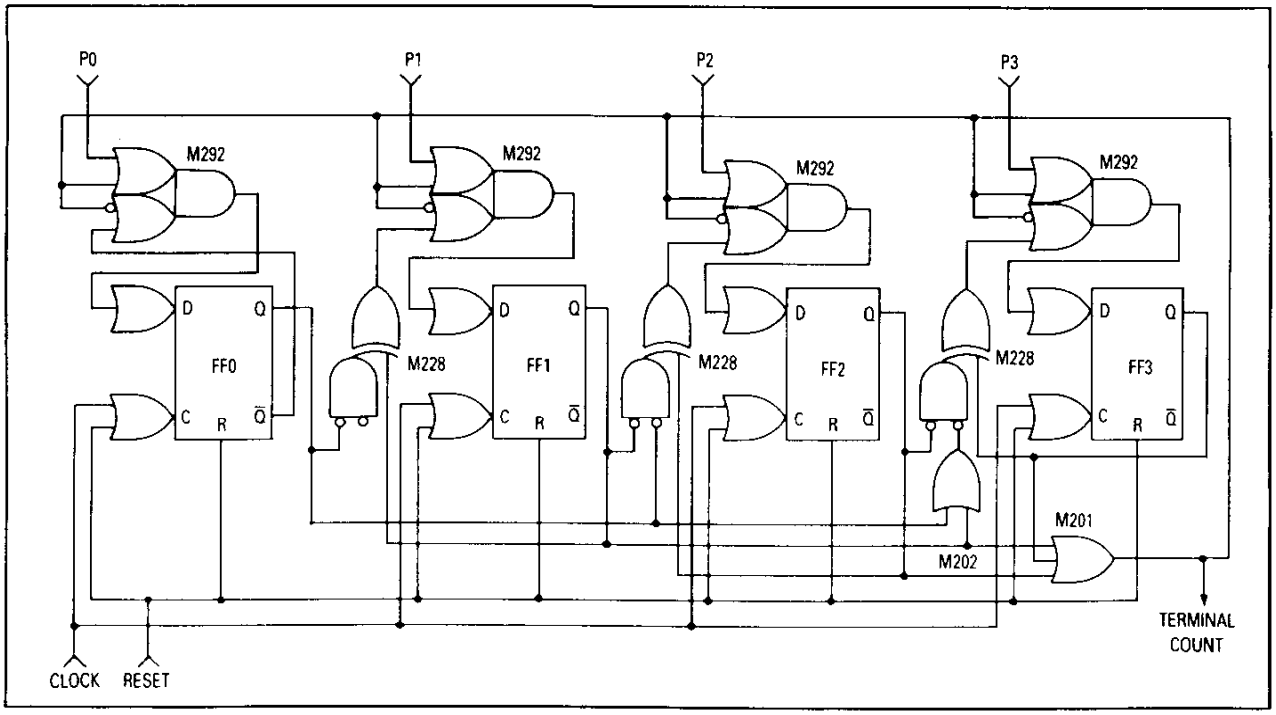


Figure 11. The Programmable Down Counter Accepts Binary Numbers on the P Inputs and Automatically Divides by the Input Number. Decoding Count 1 with the M201 OR Gate Generates the Correct Count Pattern. Count Down is Accomplished by Connecting Q Outputs to the M228 and M202 Inputs Rather Than Q Bar Outputs as in Figure 10.

bipolar ECL arrays is to tie the appropriate flip-flop outputs together in a wire-OR. In any case, for maximum performance it is important to minimize logic elements in the feedback paths.

Figure 17 illustrates two other features important to very high speed operation. M376 is a special high speed macro capable of 770 MHz operation in the MCA II ECL array library and 150 MHz in the MCA II ALS (TTL) array library with the additional feature of differential clock drive. Differential clock distribution has advantages at very high frequencies and is recommended above 400 MHz. M376 and most other very high speed flip-flops in the MCA II ECL macro library are designed for differential clock inputs.

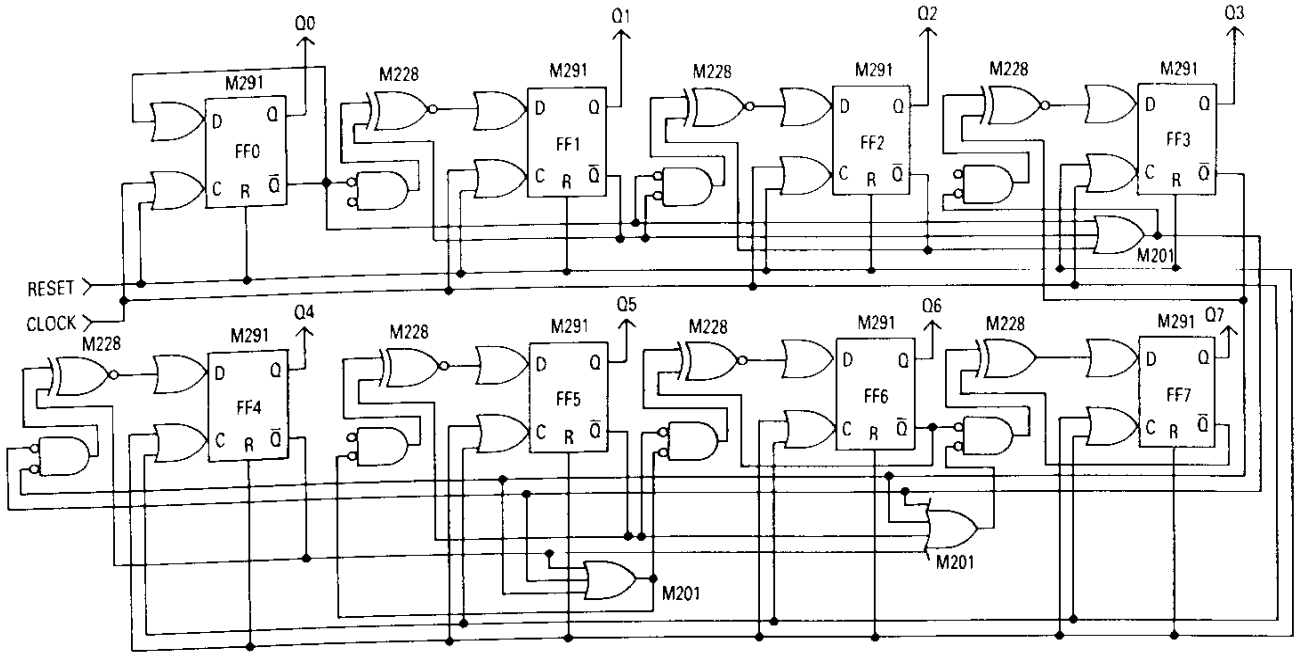


Figure 12. 8-Bit Binary Synchronous Counter with Reset

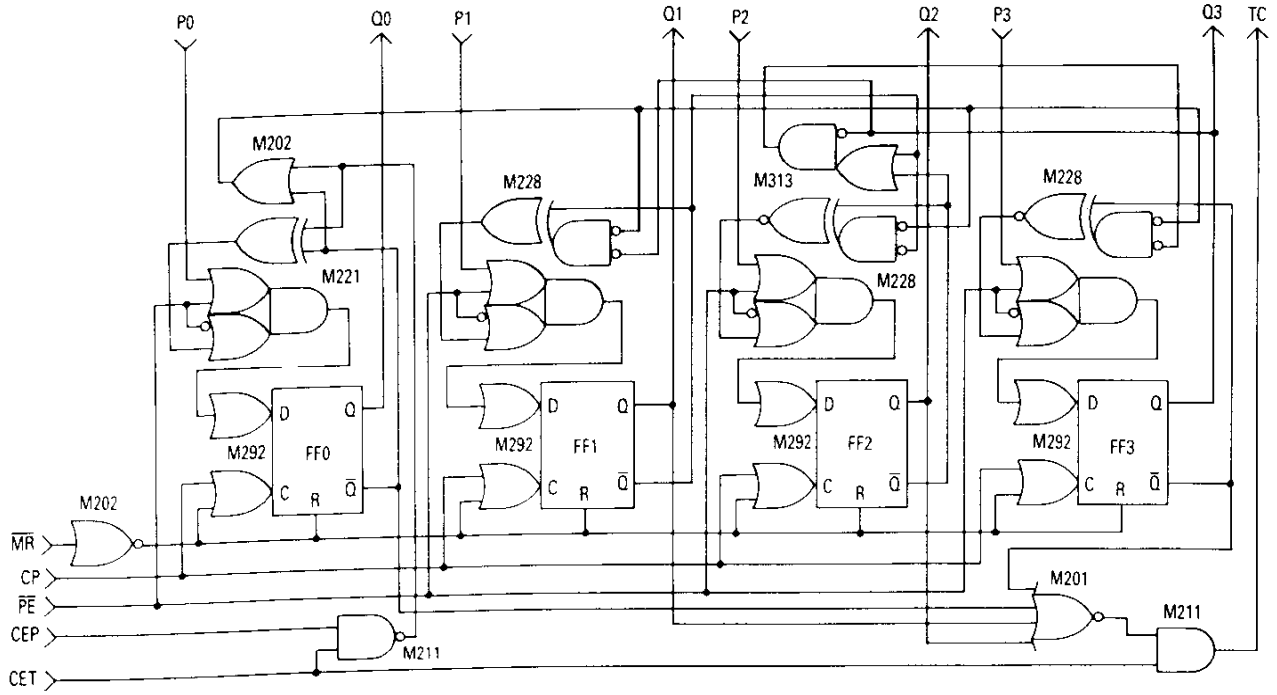


Figure 13. MCA II Series Macros Connected to Build a 74LS160A 4-Bit BCD Presettable Counter with Master Reset

A different special purpose counter is the two-modulus prescaler. Two-modulus is a variation of the full programmable counter and has wide use in phase lock loop applications. As the name implies, the two-modulus prescaler will divide by two different numbers, as selected by a control input. Common count numbers include 5/6, 8/9, 10/11, and 20/21, although standard products are available up to 128/129. Figure 18 shows the implementation of a divide-by-10/11 two-modulus prescaler. The figure shows M238 macros for high speed operation. A lower speed TTL compatible array could use all M376 macros to perform the same function.

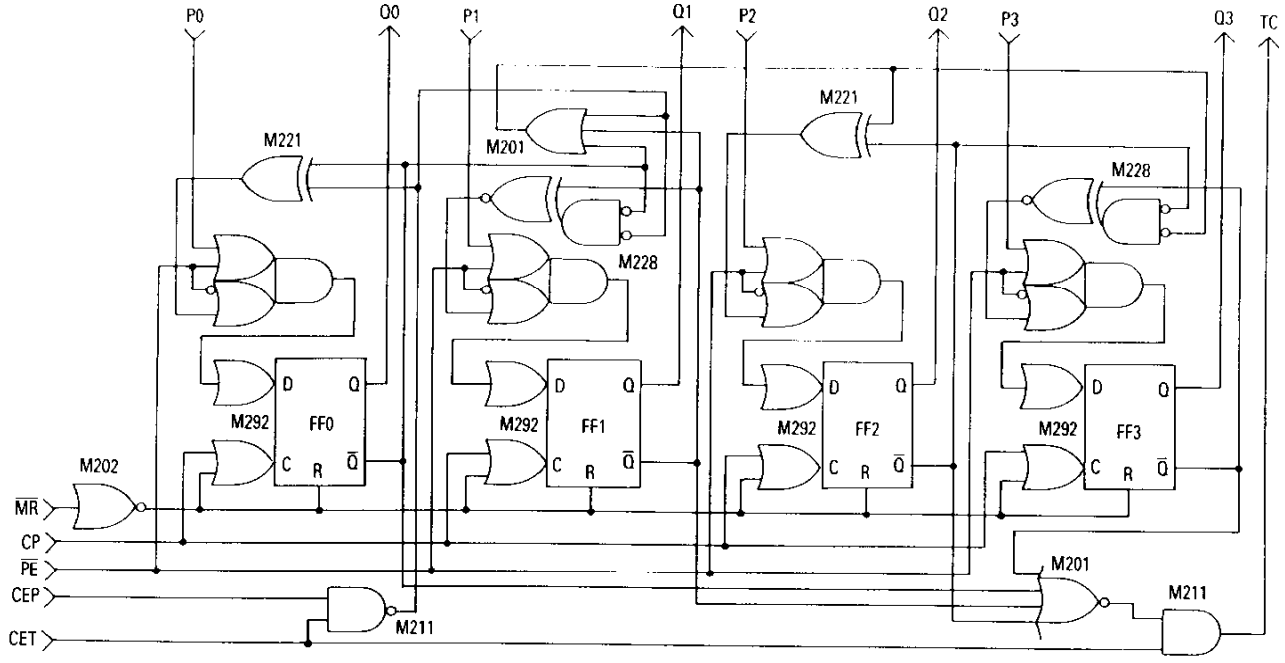


Figure 14. MCA II Series Macros Connected to Build a 74LS161A 4-Bit Binary Presettable Counter with Master Reset

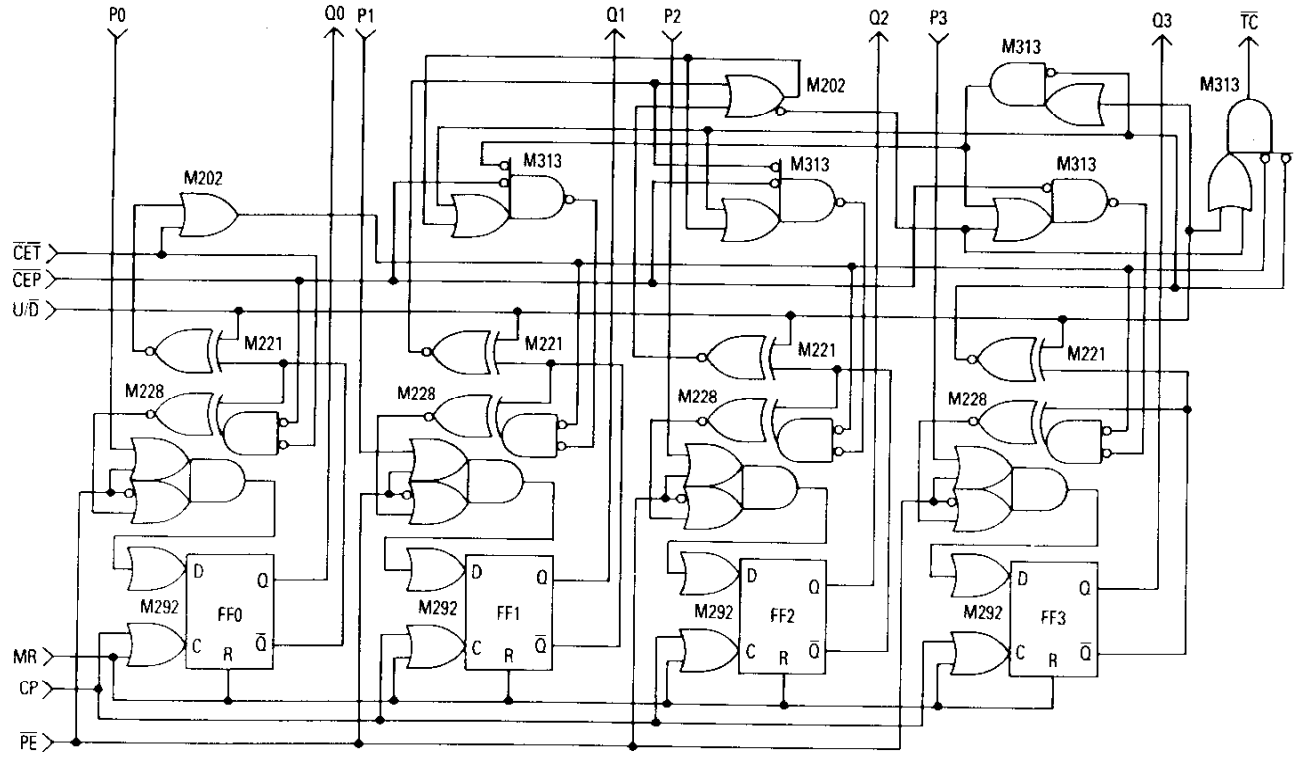


Figure 15. The 74LS168A 4-Bit Up/Down BCD Presettable Counter with Master Reset Added Illustrates Building a Complex Counter Function Out of Macrocells.

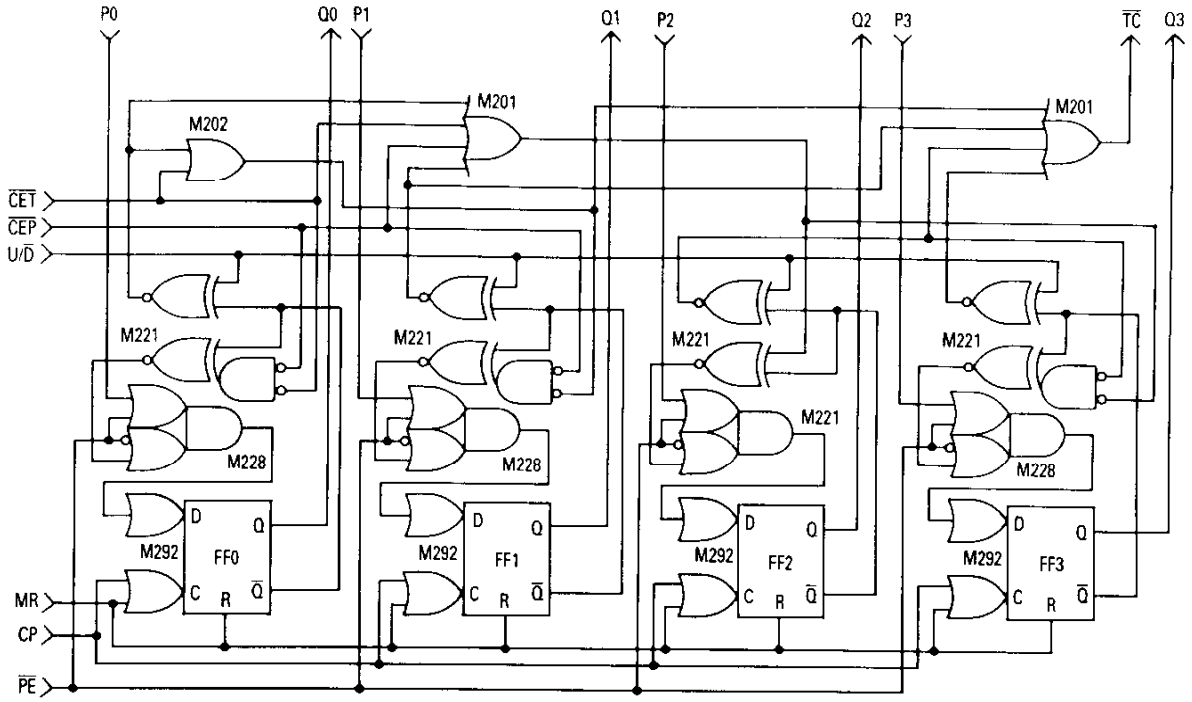


Figure 16. Macrocell Implementation of the 74LS169A Looks Complex, But Only Uses 5.75 Macrocell Locations. Master Reset Has Been Added Which is Not Part of the 74LS169A.

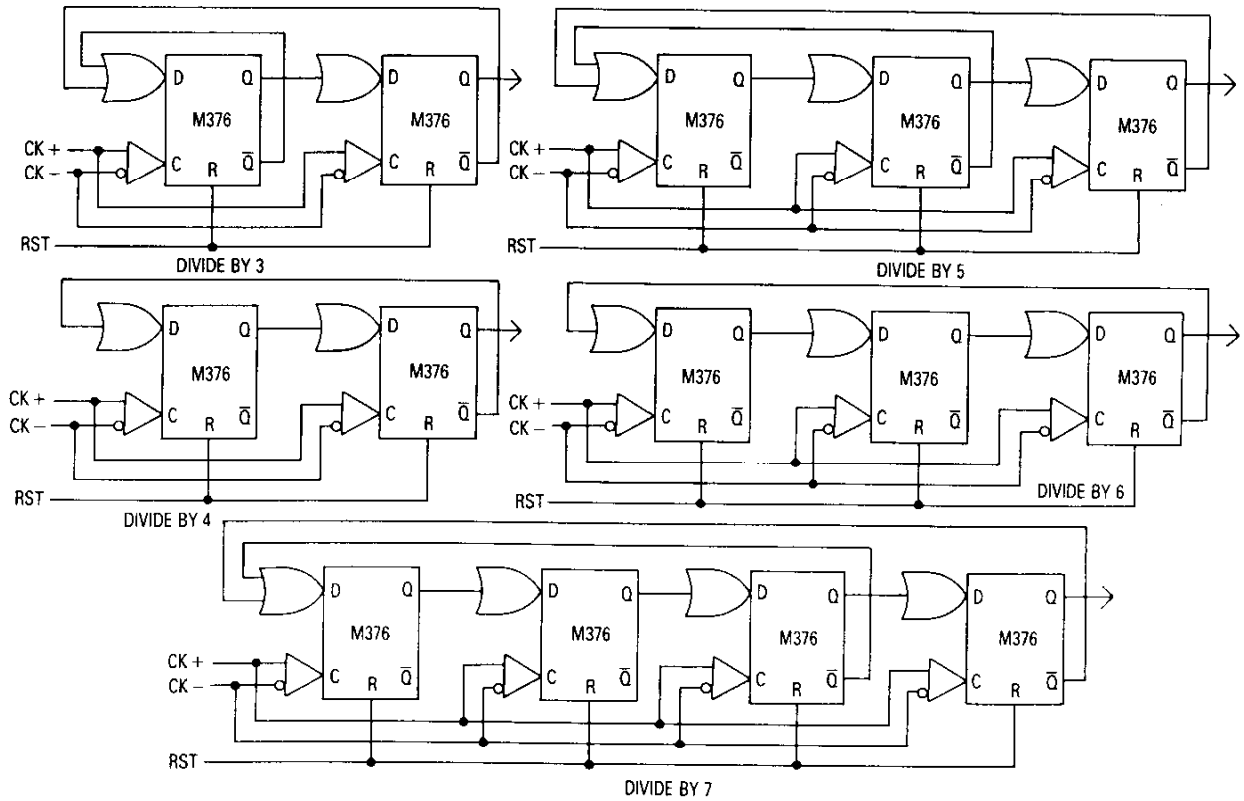


Figure 17. Shift Register Counter Circuits

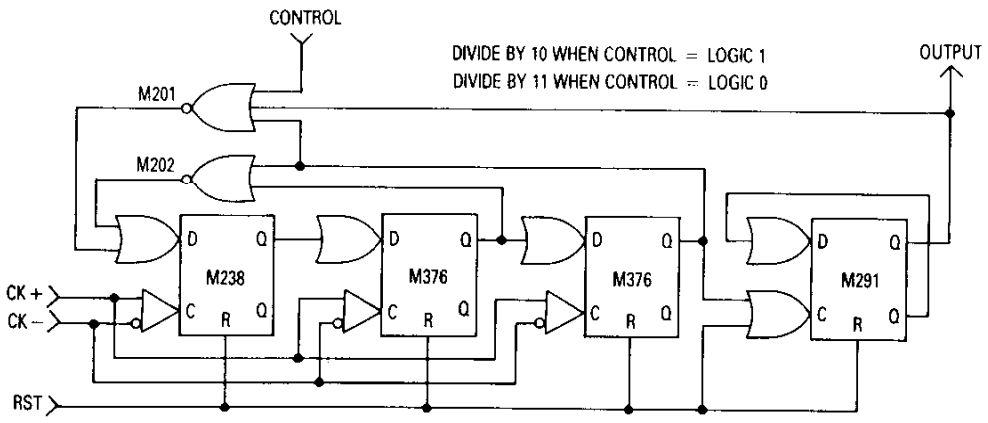


Figure 18. A Two-Modulus Prescaler Divides by Either 10 or 11 Depending on the Control Input.

COUNTER PERFORMANCE

Counter performance is usually measured by the fastest toggle frequency that is guaranteed over worst-case temperature, supply voltage and processing. It is a difficult term to name because it is not maximum frequency. Typically a given design will operate at higher frequencies than worst case. Similarly, it is not the minimum frequency because the circuits shown will operate at very low frequencies. The term worst-case frequency will be used to mean the maximum clock frequency that can be applied and meet all worst-case design conditions.

Table 1 shows worst-case frequencies for the counter circuits previously described. Motorola MCA II bipolar arrays have two performance levels. The faster, higher power ECL arrays have one set of performance limits while the lower power TTL compatible and mixed mode ECL/TTL arrays have slower performance limits. Both are shown in Table 1.

Worst-case frequencies shown are all based on computer simulations on the respective designs. In addition to macro delays, a metal loading of 20 mils per fanout has been added to more accurately reflect performance in a real world array environment. Figure 4 was modified to include actual MCA II library macros. Circuit speed was simulated with M376 macros in the first stage followed by M291s.

Table 1 shows that not all counters perform equally. The simplest counters are limited by flip-flop toggle rates while the more complex counters are limited by logic delays between the flip-flops. Counters, like most electronic circuits, offer a tradeoff between functionality and maximum performance.

Table 1. Worst-Case Toggle Frequencies Are Shown for the Various Counter Designs. Numbers Are Based on Computer Simulations for Each Circuit.

		MCA800ECL MCA2500ECL	MCA2800ALS MCA2900ETL
Circuit	**Figure**	**MHz**	**MHz**
Ripple Counter	4	770	153
Synchronous Counter	6	350	119
BCD Counter	8	400	133
Parallel Load	10	300	104
Programmable	11	312	107
8-Bit Binary	12	260	93
74LS160A	13	285	102
74LS161A	14	281	99
74LS168A	15	227	84
74LS169A	16	229	84
Ring Counters	17	770	153
Two-Modulus Prescaler	18	625	153

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Center; 88 Tanners Drive, Blakelands Milton Keynes, MK145BP, England.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; P.O. Box 80300; Cheung Sha Wan Post Office; Kowloon Hong Kong.

MOTOROLA

22226 PRINTED IN USA 11-87 IMPERIAL LITHO C52484 15,000 AN 981