MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN977

# Third Generation ECL Macrocell Arrays

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## THIRD GENERATION ECL MACROCELL ARRAYS LEAD THE ATTACK ON HIGH-PERFORMANCE SYSTEM DESIGN PROBLEMS

Armed with third-generation ECL macrocell array technology, designers prepare to assault the high-performance system design challenges of the 80's and 90's. Several competitive technologies, however, are bucking for ECL's leadership position in the attack. Presently, CMOS and mixed bipolar-MOS arrays sport integration levels as high as 50,000 gates with delays as low as 0.7 ns. For outright speed, gallium arsenide arrays, with gate propagation delays below 100 ps, still outflank ECL. Nevertheless, advances in bipolar ECL process technology combined with innovative macrocell array design yield a mix of speed and integration which guarantees that ECL arrays will continue to be the mainstay of the high-performance system designer's arsenal.

## INNOVATIVE INTERNAL ARRAY DESIGN

In order to meet the performance demands of the next generation of digital systems, designers require macrocell arrays exhibiting dramatic improvements in both speed and density. In an effort to meet these challenging requirements, Motorola's Bipolar Technology Center developed the MOSAIC III process. The key feature of the process is a smaller, higher-performance transistor structure with self-alligned polysilicon bases, emitters, and collectors. Figure 1 shows a performance comparison between Motorola's MOSAIC I and MOSAIC II processes and MOSAIC III.

Through the use of a clever "edge-defined" technique, the MOSAIC III process achieves submicron features (i.e. emitter widths) without submicron lithography. The polysilicon base electrode reduces the base resistance and capacitance thereby allowing greater switching speeds. Further speed enhancements include the use of polysilicon resistors in the current switches to reduce parasitic capacitance. The process is fast — exhibiting an $f_\tau$ greater than 10 GHz with typical gate delays in the 100 ps range.

Process improvements alone, however, will not push ECL array performance limits forward. Third-generation ECL arrays must employ innovative design features which take full advantage of the performance benefits offered by new process developments. Motorola's MCA10000ECL — a 10,000-gate ECL macrocell array — demonstrates a marriage between process innovations and design features which has produced an offspring capable of satisfying the growing needs of the high-performance design community. The MCA10000ECL is the first in a family of high-performance MOSAIC III arrays. Table 1 compares the features of the MCA10000ECL with macrocell arrays from Motorola's MCA1 and MCA2 array families. The array utilizes such features as speed-power programmability and three-level series-gated structures to realize the high-level of performance and density made possible by the MOSAIC III process while maintaining a high degree of versatility and overall array utilization.

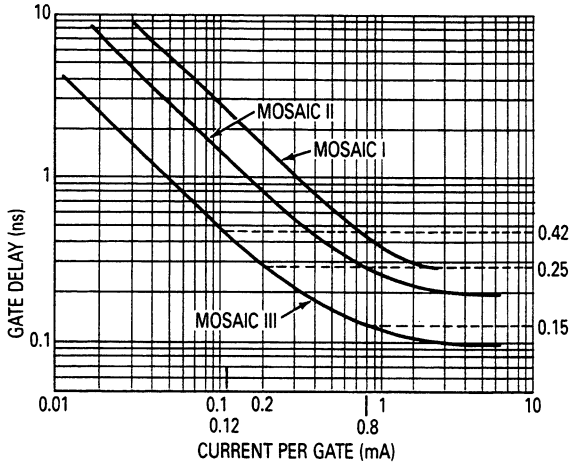



**Figure 1. Gate Delay Comparison: MOSAIC I, MOSAIC II, MOSAIC III**

MOSAIC I, MOSAIC II and MOSAIC III are trademarks of Motorola Inc.

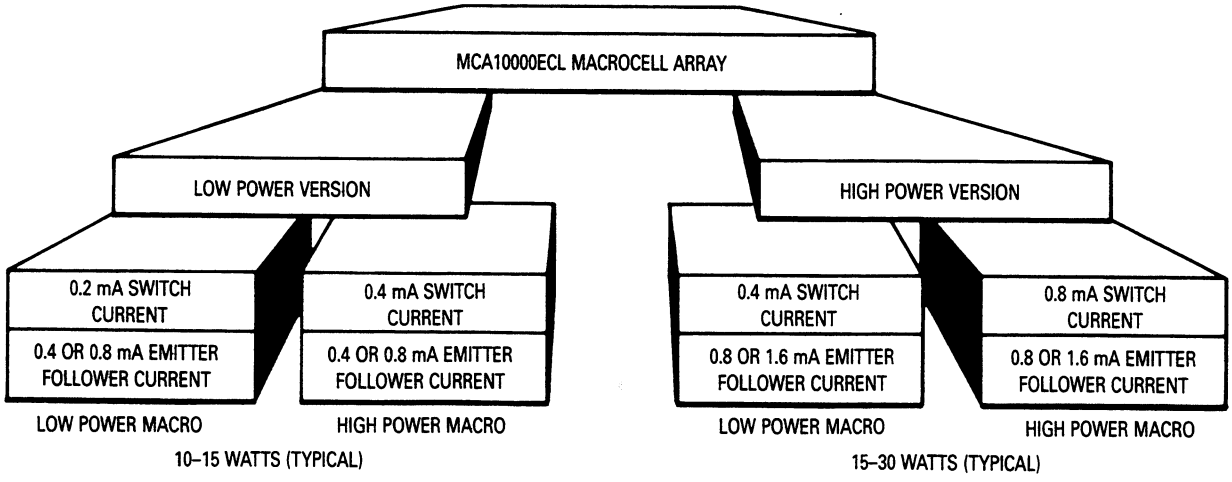
**Table 1. MCA1/MCA2/MCA3 Macrocell Array Comparison**

| Feature | MCA1200ECL | MCA2500ECL | MCA10000ECL |
|---|---|---|---|
| Equivalent Gates (Approx.) | 1200 | 2500 | 10000 |
| Interface Levels | MECL10K | 10KH/100K/10K | 10KH/100K/10K |
| I/O Ports | 60 | 120 | 180 to 256 depending on package |
| Major Cells (M) | 48 | 110 | 414 |
| Output Cells (O) | 26 | 68 | 200 |
| Interface Cells (I) | 32 | — | 224 |
| Clock Generators | 0 | 1 | 2 |
| Maximum Toggle Frequency | 250 MHz | 770 MHz | 1200 MHz |
| Basic Gate Delay (Typical) | 0.65 ns | 0.3 ns | 0.10 ns–0.25 ns |
| 4-Input OR/NOR | 1.2 ns Max | 0.5 ns Max | 0.17–0.28 ns Max depending on power selection |
| D Flip Flop (Clock) | 1.4 ns Max | 0.7 ns Max | 0.2–0.45 ns Max depending on power selection |
| Output OR Gate | 3.1 ns Max | 1 ns Max | 0.2–0.50 ns Max depending on power selection |
| Input Interface OR Gate | 1.1 ns Max | — | 0.15–0.25 ns Max depending on power selection |
| Power (Typical) | 4 Watts | 8 Watts | 10–30 Watts (Programmable) |
| Packages | 68 LCC, 72 PGA | 149-Pin Grid Array | 235 PGA, 289 PGA, 360 Lead TAB Tape |
| Bonding Technology | Wire Bond | Wire Bond | Wire Bond or TAB |
| Programmable Switch Current | NO | NO | YES |
| Routing Channels: | | | |
| Vertical | 84 | 220 | 552 |
| Horizontal | 104 | 426 | 920 |
| Process | MOSAIC I (2-Layer Metal) | MOSAIC II (3-Layer Metal) | MOSAIC III (3-Layer Metal) |
| Personalization Layers | 3 (2 Metal and 1 Via) | 3 (2 Metal and 1 Via) | 3 (2 Metal and 1 Via) |

The MCA10000ECL is offered with two mask-programmable power levels. In addition, the switch currents for most of the macrocells in the library are selectable between one of two values as shown in Table 2. These options allow for speed-power characteristics ranging from a typical gate delay of 100 ps at a switch current of 0.8 mA to a typical delay of 170 ps at a switch current of 0.2 mA. Programmable speed-power levels allow the designer to use maximum ECL speed where it is needed and trim down the power consumption where speed is not crucial in large, higher-powered arrays. The internal emitter follower pulldown current sources are connected to a separate power bus ($V_{EE2}$) which can be set as low as −3.3 Vdc to conserve power or tied to $V_{EE1}$ if only a single supply is to be used.

As the complexity of digital systems increases and the physical size decreases, designers demand greater functional density from high-performance macrocell arrays. Towards this end, Motorola utilizes three-level series gating in many of its MCA10000ECL macrocells. Several previous gate array designs have employed only two levels of series gating, thereby limiting the complexity of functions which can be designed within one current switch. The extra level of series gating used in the internal and output cells, however, provides an additional "and" (product) gate function at very high speed within one switch delay. Three-level series-gating in the design of a multiplexed D latch (see Figure 2) allows this function to be squeezed into one quarter of an internal cell. By com-

**Table 2. Power Programmability**



parison, a "vanilla" D latch (without the input MUX) built using two-level series gating occupies the same space. A multiplexed D latch implemented with two-level series gating would occupy twice the area (one half of an internal cell) and require two current sources. Thus, three-level series gating offers the designer the ability to multiplex latch inputs without the cost of additional cell usage and power — a valuable feature in designing circuits for scan-path testability.

The layout of the chip sports several features which make the MCA10000ECL a flexible yet highly routable array. Figure 3 shows the floor plan of the array. The MCA10000ECL is comprised of a central core of 414 major (M) cells (each divisible into quarter cell functions) arranged in an array of 20 rows and 21 columns. For maximum performance and density, the array core uses MECL 10KH circuitry. To further increase the internal speed of the array, the core logic uses a reduced ECL logic swing. Because of this reduced internal logic swing and the fact that the internal levels vary with temperature, all inputs to the array must pass through interface (I) cells. Although these buffers do add a small delay to the signal, the delay is insignificant compared to the overall chip delay. Six of the possible 420 internal cell sites are occupied by master bias generators and special clock generator circuits. A ring of 200 output (O) cells, used for interfacing up to 256 output pins, is interspersed by 224 input interface (I) cells surrounding the central array core. Because third-layer metal layer is used solely for power and ground distribution, on-chip supply voltage drops are virtually non-existent, thus allowing high-powered macrocells to be placed at any location on the array.

Motorola's previous MOSAIC II family of arrays has a proven track record of 100% automatic routability via CAD. The MCA10000ECL promises to carry on this tradition. Over each major cell, there are 46 horizontal (2nd metal) free routing channels along with 16 channels for power distribution. Overall, the macrocell array contains 552 vertical and 920 horizontal free routing channels in the core section alone.

## THIRD-GENERATION I/O FEATURES

The new wave of ECL arrays must provide new I/O capabilities to satisfy the demands imposed by increasing circuit board complexity and multi-chip (hybrid) packages. The MCA10000ECL gives the designer a broad choice of ECL I/O configurations with full 10KH and 100K ECL compatibility. Any of the 256 I/O pads can be designated as an input or output. Series-terminated ECL (STECL) outputs are available at the periphery of the array (see Figure 4). Programmable current-source pulldowns (6 or 11 mA) and series-terminating resistors (0, 20, or 40 ohms) allow the designer to perform output impedance matching on-chip, thus eliminating the need for external line terminations. This feature is especially important in tightly-spaced, multi-chip packages where external parallel line termination may be difficult. The designer can also select standard ECL outputs capable of driving 50 or 60 ohm lines. The STECL output can also be configured and used as an input termination when conventional ECL die are used in multi-chip modules, therefore eliminating the need for external terminating resistors. 25 ohm drivers and 50 ohm cutoff drivers are also offered on the array — the latter being available for the true outputs of all output functions.

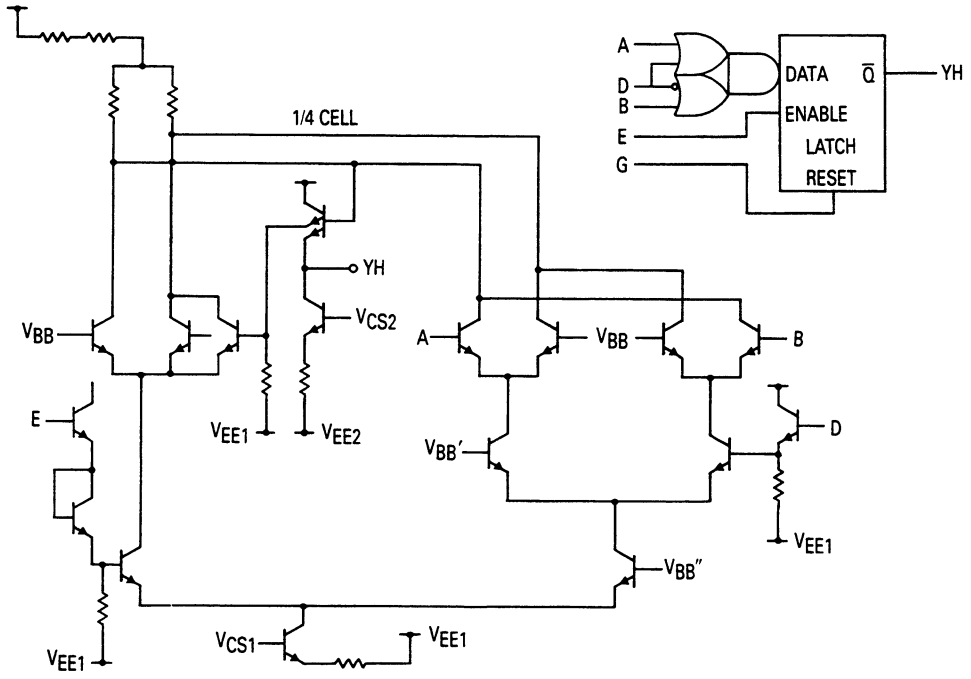
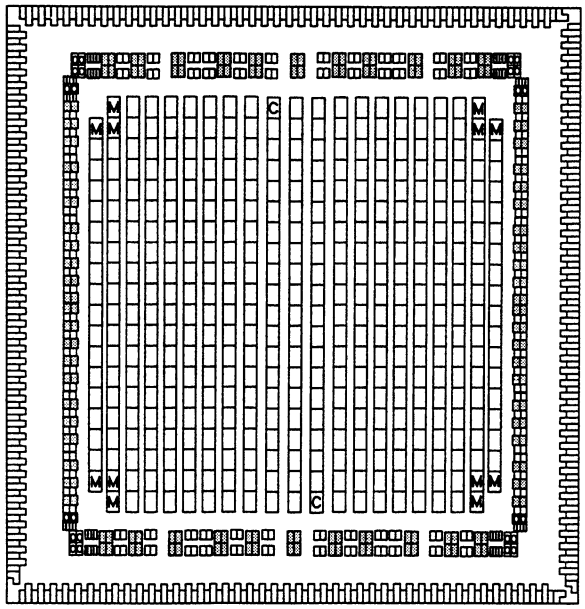



**Figure 2. Series-Gated Multiplexed D Latch**



M — MAJOR (INTERNAL) CELLS
DIVISIBLE INTO FOUR 1/4 C
414 TOTAL
I — INPUT INTERFACE CELLS
224 TOTAL
O — OUTPUT CELLS
200 TOTAL
C — CLOCK GENERATORS
2 TOTAL

OVER 1400 ROUTING CHANNELS

**Figure 3. MCA10000ECL Array Floorplan**

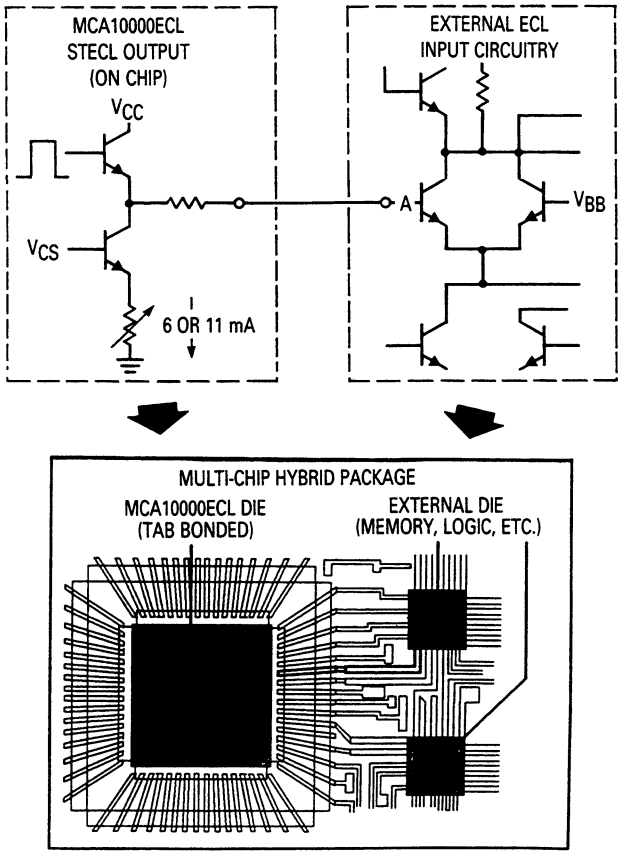



**Figure 4. Series Terminated ECL (STECL) for Multi-Chip Applications**

## PACKAGING

The higher pin counts, increased power dissipation, and tighter pad tolerances which are characteristic of third-generation ECL macrocell array technology have spurred several innovations in IC package design. Motorola's MCA10000ECL is offered in a 235 pin-grid array package with 180 I/O pins which uses conventional wire-bonding and a larger 289-pin grid array package. The 289 PGA package features standard 100 mil pin spacing and will utilize state-of-the-art Tape Automated Bonding (TAB) technology. The TAB process uses special bumps on the die which are mass-bonded to a flexible double layer metal tape consisting of 1.0 ounce copper leads attached to a polyimide dielectric substrate. Customers can also elect to receive the die bonded to a 35 mm TAB tape in a custom carrier.

Continuing process improvements in conjunction with innovative array design techniques are sure to keep the cutting edge of ECL macrocell array technology sharp and true. Using third-generation ECL macrocell arrays, such as Motorola's MCA10000ECL and future arrays built from the MOSAIC III process, the ability to implement LSI systems on a single, high-performance chip is finally within the designer's grasp.

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20846-1 PRINTED IN USA (1994) MPS/POD YNAR00

AN977/D