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Calculating Timing Requirements of External SRAM for the 24-bit DSP56000 Family

MOTOROLA

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SECTION 1

Introduction

Interfacing the DSP56000 family digital signal processors (DSPs) to external SRAM involves timing parameters that are dependant on the DSP's configuration. The external clock and the configuration of the phase-locked loop (PLL) affect the internal clock's behavior which in turn determines the necessary speed of external SRAM. Timing parameters are also affected by the configuration of signals that the DSP uses to access the SRAM.

This application note is a tutorial on calculating timing requirements for interfacing members of the DSP56000 family to external SRAM. While the examples and discussion center around the DSP56002, the approaches presented may also be applied to other members of the DSP56000 family that have an external bus.

Note: Specifications herein are based on preliminary data sheets. Any designs of a system using a member of the DSP56000 family should be based on the latest revision of the appropriate Technical Data Sheet. (See the REFERENCES section for a listing of relevant manuals and data sheets.) ■

SECTION 2

SRAM Interface

2.1 System Description

The interface between the DSP56002 and external SRAM can vary greatly depending on external memory needs of the system. Some systems will need only a limited amount of external program memory while others will require 64k each of X data memory, Y data memory, and program memory.

Consider a DSP56002 system that requires 16k each of external X data memory and external Y memory. The two data memory spaces are to be implemented with one bank of memory; 32k x 24 bits. A very straightforward implementation of such a system is shown in Figure 2-1. SRAM locations $0000-$3FFF contain the Y data memory, and locations $4000-$7FFF contain X data memory. Because the $\overline{CE}$ pin of the SRAM is connected to the upper address pin A15 of the DSP, the bank of memory is enabled only when the DSP has accessed external RAM at addresses less than $8000.

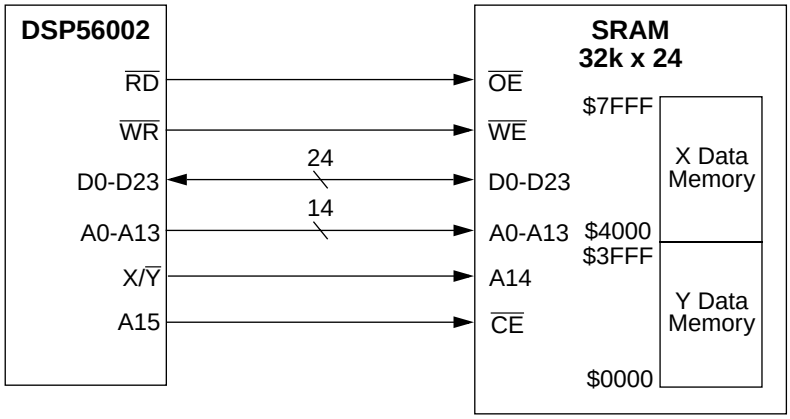

Figure 2-1 DSP56002 Interface to External SRAM

2.2 Read Timing

When reading external memory (see Figure 2-2), the DSP56002 first asserts the memory address (A0-A15, $\overline{DS}$, $\overline{PS}$, and X/$\overline{Y}$.) After a delay of t_{AR}, the DSP asserts the read enable signal ($\overline{RD}$) which enables the SRAM's output. The SRAM in turn puts valid data on the data bus after an access time of t_{AA}. The DSP then latches this data when it pulls $\overline{RD}$ high again.

The data access time t_{AA} is typically the critical timing specification and must be less than the maximum allowed by specification #130 (Address Valid to Input Data Valid) of the *DSP56002 Technical Data Sheet*. The 66 MHz version of the DSP56002 requires that the SRAM places valid data on the bus no later than $T_C + T_L - 7$ ns after the DSP asserts an address, where T_C and T_L are the cycle time and the low time of the internal clock, respectively.

$$t_{AA} \leq T_C + T_L - 7ns \qquad \text{Eqn. 2-1}$$

The time (t_{OHZ}) from a rising edge of $\overline{OE}$ high to a high impedance output of the SRAM must be greater than or equal to that allowed by specification #128 (Input Data Hold Time to $\overline{RD}$ Deassertion) of the *DSP56002 Technical Data Sheet*. Because the hold time of the DSP (specification 128) need only be greater than or equal to 0, any positive value of t_{OHZ} will work, and the specification need not be a concern.

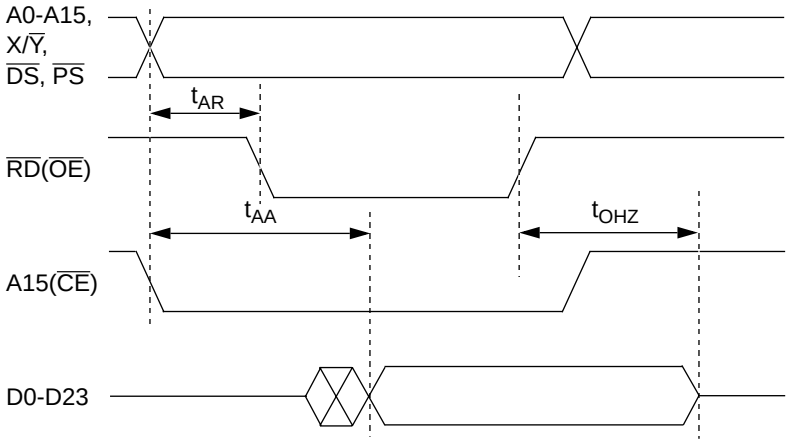

Figure 2-2 Read Cycle Timing Diagram

2.3 Write Timing

When writing to external memory (see Figure 2-3), the DSP56002 again first asserts the memory address, and after a delay of t_{AW} asserts write enable ($\overline{WR}$). The DSP then puts valid data on the data bus. After a delay of t_{DW} the DSP pulls $\overline{WR}$ high, and then de-asserts the address after t_{WR} while holding the data for t_{DH}.

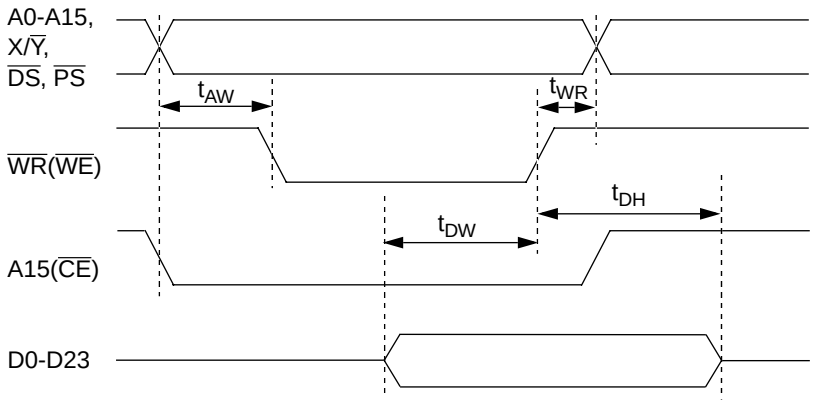

Figure 2-3 Write Cycle Timing Diagram

With a write cycle, the data setup time t_{DW} of the SRAM is typically the critical timing specification. The SRAM requires a minimum setup time of the data from the DSP56002 before $\overline{WE}$ goes high and latches data into the SRAM. This minimum data setup time must be less than or equal to the minimum guaranteed by specification #125 (Data Out Setup Time to $\overline{WR}$ Deassertion) of the *DSP56002 Technical Data Sheet*. Hence, t_{DW} must be less than or equal to T_L - 0.4 ns (for the 66 MHz part).

$$t_{DW} \leq T_L - 0.4\text{ns} \qquad \text{Eqn. 2-2}$$

2.4 Calculating T_C and T_L

The two critical specifications (numbers #125 and #130 of the *DSP56002 Technical Data Sheet*) rely on the values of T_C and T_L, the internal clock cycle time and low time, respectively. These two values along with that of the internal clock's high time, T_H, depend on the external clock's cycle time, ET_C, high time, ET_H, and low time, ET_L, and the PLL's multiplication factor, MF, and division factor, DF. If the PLL is not used, the internal cycle time, high time, and low time simply equal the external cycle time, high time, and low time. If the PLL is used, the values are calculated as specified in Table 2-1. (These values are also listed in the "AC Electrical Characteristics - Internal Clocks" section of the *DSP56002 Technical Data Sheet*.)

Table 2-1 Formulas for T_H, T_L, and T_C

Characteristics	Symbol	Expression
Internal Clock High Period	T_H	
-with PLL enabled and MF ≤ 4		(Min) $0.480 \times ET_C \times DF/MF$
		(Max) $0.520 \times ET_C \times DF/MF$
-with PLL enabled and MF > 4		(Min) $0.467 \times ET_C \times DF/MF$
		(Max) $0.533 \times ET_C \times DF/MF$
Internal Clock Low Period	T_L	
-with PLL enabled and MF ≤ 4		(Min) $0.480 \times ET_C \times DF/MF$
		(Max) $0.520 \times ET_C \times DF/MF$
-with PLL enabled and MF > 4		(Min) $0.467 \times ET_C \times DF/MF$
		(Max) $0.533 \times ET_C \times DF/MF$
Internal Clock Cycle Time	T_C	$ET_C \times DF/MF$

2.4.2 Example 1

Assume the system presented in Section 2.1 and Figure 2-1 has a DSP56002 internal clock of 50 MHz. The internal clock is generated by inputting a 10 MHz clock into the PLL which is programmed with a multiplication factor of 5 and a division factor of unity. These system specifications provide enough information to specify what SRAM will suffice for zero wait state memory accesses.

Since the part will be run faster than 40 MHz, a 66 MHz part is required. Therefore, the 66 MHz version of the timing specification is appropriate for calculations. Because the restrictions of both Eqn. 2-1 and Eqn. 2-2 specify maximum values permitted by the DSP56002, the lowest of each of these maximum values should be used. Examination of Eqn. 2-1 and Eqn. 2-2 shows that the minimum values of T_C and T_L should be used. The minimum values are calculated by substituting the given values into the appropriate expressions from Table 2-1. Finally, these values are plugged into Eqn. 2-1 and Eqn. 2-2 to yield the maximum t_{AA} and t_{DW}.

$$t_{AA} \le T_C + T_{L(min)} - 7ns \;=\; ET_C \times \frac{DF}{MF} + 0.467 \times ET_C \times \frac{DF}{MF} - 7ns$$

$$t_{AA} \le 100 \times \frac{1}{5}(1.467) - 7ns$$

Eqn. 2-3

$$t_{AA} \le 22.3ns$$

$$t_{DW} \le T_L - 0.4ns \;=\; 0.467 \times ET_C \times \frac{DF}{MF} - 7ns$$

Eqn. 2-4

$$t_{DW} \le 100 \times \frac{1}{5}(0.467) - 0.4ns$$

$$t_{DW} \le 8.9ns$$

The MCM6206D is a 32k x 8 bit fast SRAM made by Motorola and available in speeds of 15 ns, 17 ns, 20 ns, 25 ns, 30 ns, and 35 ns. Examination of the MCM6206D's specifications for the different speeds shows that the 20 ns part works well, guaranteeing a maximum address access time of 20 ns and requiring a minimum data access time of 8 ns.

2.4.3 Example 2

Consider the system described above in Example 1 being driven by an external clock of 45 MHz with a duty cycle (high time) of 46.7% - 53.3% (the exact requirements of specifications #1 and #2 in the *DSP56002 Technical Data Sheet*). The desired internal clock is now 45 MHz. In determining what speed SRAM to use in this system, the system designer has the option of either using the external clock directly as the internal clock or inputting the external clock to the PLL and using the PLL's output as the internal clock. These two clock implementations result in two different sets of timing requirements which should both be calculated before the system designer selects the SRAM to be used.

Since the DSP will be run faster than 40 MHz, the system must again use a 66 MHz part. With the PLL disabled, the values to use for Eqn. 2-1 and Eqn. 2-2 are:

$$T_C = \frac{1}{45MHz} = 22.2ns \qquad \text{Eqn. 2-5}$$

$$T_L = \frac{1}{45MHz} \times 0.467 = 10.38ns \qquad \text{Eqn. 2-6}$$

Hence the restrictions for t_{AA} and t_{DW} become:

$$t_{AA} \leq T_C + T_{L(min)} - 7ns = 25.6ns \qquad \text{Eqn. 2-7}$$

$$t_{DW} \leq T_L - 0.4ns = 9.98ns \qquad \text{Eqn. 2-8}$$

The restriction from t_{AA} requires a 25 ns version of the MCM6206D, but the restriction for t_{DW} is tighter, requiring a 20 ns version.

According to Table 2-1, the minimum values to use for Eqn. 2-1 and Eqn. 2-2 at 45 MHz with the PLL enabled are:

$$T_C = \frac{1}{45MHz} = 22.2ns \qquad \text{Eqn. 2-9}$$

$$T_L = \frac{1}{45MHz} \times 0.48 = 10.7ns \qquad \text{Eqn. 2-10}$$

and the restrictions for t_{AA} and t_{DW} become:

$$t_{AA} \leq T_C + T_{L(min)} - 7ns = 25.9ns \qquad \text{Eqn. 2-11}$$

$$t_{DW} \leq T_L - 0.4ns = 10.3ns \qquad \text{Eqn. 2-12}$$

The 25 ns version of the MCM6206D meets the above two requirements. Using the PLL to clean up the clock signal in this example enables the designer to use a slower SRAM which consequently lowers the system cost.

Unlike the DSP56002, the DSP56000 and DSP56001 do not have a PLL. ■

SECTION 3

Additional Considerations

3.1 Glue Logic

Any glue logic that interfaces between the DSP56002 and the external SRAM will introduce additional delays to the system which must be considered when calculating timing requirements. For example, if a PLD with a propagation delay is added as an address decoder between the DSP and the SRAM, the propagation delay of the PLD must be added to the address access time in Eqn. 2-3. Thus the SRAM must be that much faster than without such an address decode.

3.2 Maximum and Minimum Specifications

In the calculation of timing requirements, adding a maximum value of one specification and a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation in process parameters in one direction, and a minimum specification is calculated using the worst case of the same parameters in the opposite direction. Therefore "maximum" values of a specification will never occur on the same device that has a "minimum" value of another specification, and adding a maximum to a minimum results in an unrealizable condition. The obvious exception to this rule is a clock's high time and low time. Clearly a clock with a maximum high time must have a minimum low time for a given period.

3.3 Additional Specifications to Meet

Specifications #125 and #130 (listed in DSP Technical Data Sheets) are typically the critical specifications and will be the most useful in selecting a suitable SRAM for a given system. However, other timing requirements must also be met. After selecting an SRAM based on specifications #125 and #130, the designer should ensure that each of the other timing specifications given in the data sheet (and only

these specifications) are met. If only a minimum value is given, only the minimum needs to be met. If only a maximum value is given, only the maximum needs to be met. As with specification #124 (Data Out Hold Time from $\overline{WR}$ Deassertion) if both maximum and minimum values are given, both conditions must be met.

3.4 Different Timing Specifications

The DSP56002 is available in different versions based on the speed of the part. One version is specified for a maximum speed of 40 MHz and tested at 40 MHz. A second version is specified for a maximum speed of 66 MHz and is tested at 66 MHz. Many of the timing specifications for these two different versions of the chip are distinct from one another. For example, specification #130 has a maximum value of $T_C + T_L - 9.5$ ns for the 40 MHz part and $T_C + T_L - 7$ ns for the 66 MHz part. Limiting selection to these two versions of the part requires that for speeds above 40 MHz, a 66 MHz chip should be used, and timing requirements should be calculated with 66 MHz specifications.

3.5 Wait States

Wait states affect the timing requirements of both specifications #125 and #130 and hence may offer the appropriate timing for a given memory. Specification #130 is increased by T_C times the number of wait states. Hence Eqn. 2-1 becomes:

$$t_{AA} \leq (WS + 1)T_C + T_L - 7ns \qquad \text{Eqn. 3-1}$$

where: WS = the number of wait states

Similarly, specification #125 is increased by T_C times the number of wait states, and Eqn. 2-2 becomes:

$$t_{DW} \leq WS \times T_C + T_L - 0.4ns \qquad \text{Eqn. 3-2}$$

3.6 Asynchronous vs. Synchronous Timing

Asynchronous timing specifications were used in the calculations in this application note and are the appropriate specifications to be used. Since asynchronous timing specifications permit greater timing margins for external devices, they should be used for peripheral devices that do not use the system clock. For example, external SRAM has no need for the system clock but needs only address, read, and write signals.

Since the synchronous timing specifications are referenced to the external clock signal of the DSP56002, they must accommodate any skew between the external and the internal clock signals. Therefore, synchronous specifications allow less timing margin for a peripheral device. Peripherals that make use of the DSP's clock (i.e. external data latches) must meet the synchronous timing specifications. ■

SECTION 4

Summary

When interfacing members of the 24-bit DSP56000-family to external SRAM, the systems designer can typically base the selection of an appropriate SRAM on the data access time t_{AA} and the data setup time t_{DW} specifications (#130 and #125 of the appropriate Technical Data Sheet). While each timing specification of the Technical Data Sheet must be met, specifications #125 and #130 usually impose the critical constraints. Glue logic, address decode, clock signals, and PLL configuration all affect the timing constraints of the system, and all can be manipulated to implement the best system for a given application. ■

REFERENCES

1. Motorola DSP56000 Technical Data Sheet (DSP56000/D), Motorola, 1992.
2. Motorola DSP56001 Technical Data Sheet (DSP56001/D), Motorola, 1992.
3. Motorola DSP56002 Technical Data Sheet (DSP56002/D), Motorola, 1992.
4. *DSP56000 Digital Signal Processor Family Manual* (DSP56KFAMUM/AD), Motorola, 1992.
5. *DSP56000/DSP56001 Digital Signal Processor User's Manual* (DSP56000UM/AD), Motorola, 1990.
6. *DSP56002 Digital Signal Processor User's Manual* (DSP56002UM/AD), Motorola, 1993. ■