ENGINEERING BULLETIN

Procedures for Prototyping Motorola CMOS Gate Arrays via Chip Express

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Introduction

Situations have occurred when an Application Specific Integrated Circuit (ASIC) was manufactured to the documented specifications, only to discover that the specification was not fully understood and all board level system dynamics were not defined. Unfortunately, many of these dynamics are unknown until the ASIC is plugged into the system. Designers now have a new weapon to improve cycle time and assure that the ASIC does interplay with the board level system, as specified. Motorola's ASIC IC division in Chandler, Arizona has worked with Chip Express of Santa Clara, California to provide a one-day prototype cycle time on designs which use a limited macro content. Designers can now perform system level testing of critical gate array functions by prototyping those functions in silicon in a single day. The Chip Express gate array prototyping service can be used to help designers obtain early functional prototypes of Motorola's HDC, H4C, and H4CPlus Series arrays to debug their device, function, or system.

With the help of Chip Express, designers can convert a target design or function from the Motorola design environment to a Chip Express prototype definition. This is accomplished in one of three ways: 1) Netlist conversion by Chip Express, 2) Design translation using Synopsys, or 3) Design compilation using Synopsys from source HDL. Each of these methods is described in the following sections.

Method #1 - Netlist Conversion by Chip Express

The Chip Express netlist conversion method retains Motorola's netlist structure and names. Designers provide Chip Express with the items defined in Table 10 and Chip Express converts the design description from Motorola to Chip Express formats. This approach is useful when the designer needs to maintain functionality while allowing system speed to be changed. The designer has full control over the netlist, since the structure and names are preserved. This type of conversion will be done at Chip Express with the limitations defined in the following pages.

Core Macros

Chip Express supports most of Motorola's core macros with the following exclusions: metallized RAM, diffused RAM, JTAG, RAM BIST, and PLL macros. A list of unsupported macros in each of the CMOS Series libraries is provided in Table 1, Table 2, and Table 3.

Table 1. Unsupported HDC Series Memory Macros

RDA8X9	RDA16X9	RDA32X9	RDA8X18	RDA16X18	RDA32X18
RDA8X36	RDA16X36	RDA32X36	RDA8X72	RDA16X72	RDA32X72
RQ16X18	RQ32X18	RQ16X36	RQ32X36	RSA32X08	RSA8X18
RSA16X18	RSA32X18	RSA64X18	RSA16X36	RSA32X36	RSA64X36

Table 2. Unsupported H4C Series Core Macros

RDA8X9	RDA8X18	RDA8X36	RDA8X72	RDA16X9	RDA16X18
RDA16X36	RDA16X72	RDA32X9	RDA32X18	RDA32X36	RDA32X72
RQ16X18	RQ16X36	RQ32X18	RQ32X36	RSB8X18	RSB16X18
RSB16X36	RSB32X8	RSB32X18	RSB32X36	RSB64X18	RSB64X36
BPREG	ENSCANI	IDREG	MC_IREG	MC_IREG4	FMC_TAPC
ADDR_CELL	DATA_CELL	COMPACELL	COMPDCELL	COMPBISTCNTL	
DLYLN6	DLYLN7	PHSDET	PLLCTR7		

Table 3. Unsupported H4CPlus Series Core Macros

RDA8X9	RDA8X18	RDA8X36	RDA8X72	RDA16X9	RDA16X18
RDA16X36	RDA16X72	RDA32X9	RDA32X18	RDA32X36	RDA32X72
RQ16X18	RQ16X36	RQ32X18	RQ32X36	RSB8X8	RSB8X18
RSB16X8	RSB16X18	RSB16X36	RSB32X8	RSB32X18	RSB32X36
RSB64X18	RSB64X36	BPREG	ENSCANI	IDREG	MC_IREG
MC_IREG4	FMC_TAPC	ADDR_CELL	DATA_CELL	COMPACELL	COMPDCELL
COMPBISTCNTL					

Input Macros

Chip Express supports Motorola's input macros with the following exclusions: 3V, 3V-to-5V translation, 5V-to-3V translation, CMTL, GTL, PECL, PCI, and JTAG inputs. All HDC Series input macros are supported. Due to the large number of unsupported H4C and H4CPlus Series macros, Table 4 and Table 5 show only the *supported* macros.

Table 4. Supported H4C Series Input Macros

ICI	ICIH	ICN	ICNH	ISN	ISNH
ITN	ITNH	ITSN	ITSNH		

Table 5. Supported H4CPlus Series Input Macros

ICI	ICN	ICNH	ISN	ISNH	ITN
ITNH	ITSN	ITSNH			

Output Macros

Chip Express supports Motorola's output macros with the following exclusions: 3V, 3V-to-5V translation, 5V-to-3V translation, CMTL, GTL, PECL, PCI, and JTAG outputs. All HDC Series output macros are supported. Due to the large number of unsupported H4C and H4CPlus Series macros, Table 6 and Table 7 show only the *supported* macros.

Table 6. Supported H4C Series Output Macros

ON2	ON4	ON8	ON4S2	ON8S2	ON4S4
ON8S4	ON2T	ON4T	ON8T	ON4TS2	ON8TS2
ON4TS4	ON8TS4	ON2OD	ON4OD	ON8OD	ON4ODS2
ON8ODS2	ON4ODS4	ON8ODS4			

Table 7. Supported H4CPlus Series Output Macros

ON2	ON4	ON8	ON16	ON32	ON4S2
ON8S2	ON16S2	ON32S2	ON2T	ON4T	ON8T
ON16T	ON32T	ON4TS2	ON8TS2	ON16TS2	ON32TS2
ON2OD	ON4OD	ON8OD	ON16OD	ON32OD	

Bidirectional Macros

Chip Express supports Motorola's bidirectional macros with the following exclusions: 3V, 3V-to-5V translation, 5V-to-3V translation, CMTL, GTL, PECL, PCI, and JTAG. All HDC Series bidirectional macros are supported. Due to the large number of unsupported H4C and H4CPlus Series macros, Table 8 and Table 9 show only the *supported* macros.

Table 8. Supported H4C Series Bidirectional Macros

BICI	BICN	BISN	BITN	BITSN	BON2T
BON4T	BON8T	BON4TS2	BON8TS2	BON4TS4	BON8TS4
BON2OD	BON4OD	BON8OD	BON4ODS2	BON8ODS2	BON4ODS4
BON8ODS4					

Table 9. Supported H4CPlus Series Bidirectional Macros

BICI	BICN	BISN	BITN	BITSN	BONT2
BON4T	BON8T	BON16T	BON32T	BON4TS2	BON8TS2
BON16TS2	BON32TS2	BON8OD	BON16OD	BON32OD	

Deliverables for Netlist Conversion

To successfully convert the design and provide a prototype, Chip Express expects the designer to provide the items listed in Table 10.

Table 10. Deliverables for Netlist Conversion by Chip Express

FILE	DESCRIPTION
Netlist	Verilog netlist describing the design using the supported Motorola macros.
Pinout	Table matching signal names to package pins and identifying power/ground pin locations. This file can be in any format.
Vectors	Test vector file in the CTV or YTV (Chip Express Test Vector) formats created from verilog simulation using a Chip Express PLI utility. Please refer to the *Quick® Verilog Design Kit* available from Chip Express.

Method #2 - Design Translation Using Synopsys

Design translation using Synopsys does not keep the netlist structure and names. The design will be converted using the Synopsys tool set. This approach is useful when the designer needs to maintain functionality, while system speed can be changed. This type of conversion can be done by the designer or by Chip Express with the macro limitations listed in Tables 1 through 9.

Deliverables for Design Translation

To successfully convert the design for the designer and/or provide a prototype, Chip Express expects the designer to provide the items listed in Table 11.

Table 11. Deliverables for Design Translation Using Synopsys

FILE	DESCRIPTION
Netlist	If the translation is to be done by Chip Express, a verilog netlist describing the design using the supported Motorola macros. If the designer chooses to perform the Synopsys translation in house, a verilog netlist describing the design using the Chip Express library.
Pinout	Table matching signal names to package pins and identifying power/ground pin locations. This file can be in any format.
Vectors	Test vector file in CTV (Chip Express Test Vector) format created from verilog simulation using a Chip Express PLI utility. Please refer to the *Quick® Verilog Design Kit* available from Chip Express.

Method #3 - Design Compilation Using Synopsys From Source HDL

Design compilation using Synopsys from source HDL does not keep the netlist structure and names since the design is synthesized by Synopsys from the source HDL directly to the Chip Express technology. This approach is useful when the designer needs to maintain control over the system speed. This type of conversion is done only by the designer. Before going to production, the designer must recompile the design in the appropriate Motorola technology.

Deliverables for Design Compilation

To successfully provide a prototype for the designer, Chip Express expects the designer to provide the items listed in Table 12.

Table 12. Deliverables for Design Compilation Using Synopsys

FILE	DESCRIPTION
Netlist	Verilog netlist describing the design using the Chip Express library.
Pinout	Table matching signal names to package pins and identifying power/ground pin locations. This file must be in the Chip Express format defined in the *Quick® Verilog Design Kit* available from Chip Express.
Vectors	Test vector file in CTV (Chip Express Test Vector) format created from verilog simulation using a Chip Express PLI utility. Please refer to the *Quick® Verilog Design Kit* available from Chip Express.

Supported Package Types and Pin Counts

Chip Express supports several standard Motorola QFP packages. The supported Motorola QFP packages are listed in Table 13. Be aware that not all packages are available for all gate array sizes or power levels. Please refer to the appropriate Motorola *Design Reference Guide* or Chip Express for guidance.

Table 13. Supported Motorola QFP Packages

80 QFP	100 QFP	128 QFP
160 QFP	208 QFP	240 QFP

For More Information about prototyping a Motorola CMOS gate array with Chip Express, please contact Chip Express at:

Chip Express Corporation
2903 Bunker Hill Lane, Suite 105
Santa Clara, California 95054
(408)-988-2445, EMail: moreinfo@chipx.com

	References	Order Numbers	Source
[1]	*HDC Series Design Reference Guide*	HDCDM/D REV. 2	Motorola
[2]	*H4C Series Design Reference Guide*	H4CDM/D REV. 1	Motorola
[3]	*H4CPlus Series Design Reference Guide*	H4CPDM/D REV. 1	Motorola
[4]	*QYH400 Macro Cell Library*		Chip Express
[5]	*QYH500 Macro Cell Library*		Chip Express
[6]	*Quick® Verilog Design Kit*		Chip Express
[7]	*Quick® Synopsys Design Kit*		Chip Express

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