

Mounting Method for RF Power Leadless Surface Mount Transistors

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INTRODUCTION

The use of leadless surface mount RF power devices in wireless systems has challenged typical assembly techniques and thermal management methods that have been well-accepted for decades in the industry. In mounting these devices, key attention must be given to Coefficient of Thermal Expansion (CTE) properties of the device (particularly in the z-axis), the terminals, the heat sink, and the board as well as to the solder hierarchy within the system. This application note describes issues, concerns, and solutions for RF Power Transistor mounting of leadless surface mount components in the range of 1–20 watts dissipated power. The MRF1507 device is used in this discussion for illustration purposes. The MRF1507 is an 8 watt power transistor and is packaged as a plastic, leadless, surface mount component.

THERMO-MECHANICAL STRESS ISSUES

When considering how to attach surface mount devices to the system in a power application, one's first inclination might be to solder attach the device backside to some type of heatsink which protrudes through the board and is mounted in some way to a chassis. Copper or brass are typically the chosen heatsinks in this scenario. These are chosen for optimum thermal performance, ensuring that there is a direct path from the heat generated in the die itself, through the leadframe, solder, heatsink, to the chassis. A typical depiction of this scheme can be seen in Figure 1.

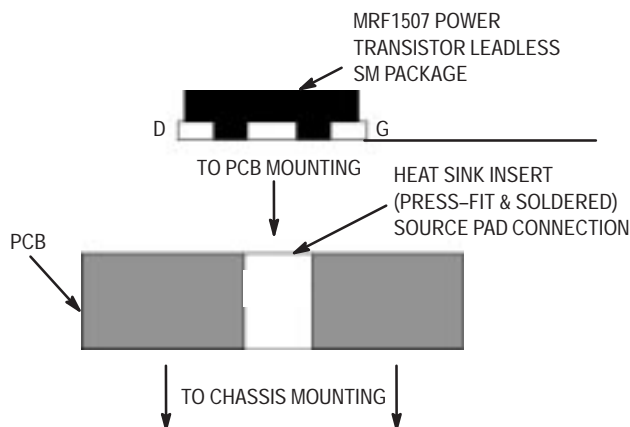


Figure 1. Initial Mounting Technique for Surface Mount RF Power Devices

The terminals of the device are attached using solder to an FR-4 or epoxy glass board. Meanwhile, the backside of the device is simultaneously attached to the copper or brass heat-

sink which is press fit and soldered to the FR-4 printed circuit board (PCB).

A finite element model immediately points out the deficiencies of such a mounting scheme.

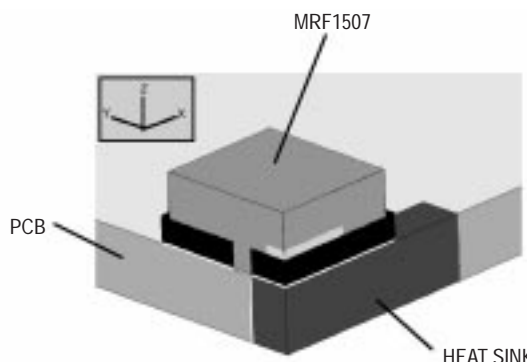


Figure 2. MRF5007 Solid Model (1/4 Symmetry)



Figure 3. MRF1507 Device

A thermo-mechanical stress model, shown in Figure 2, was developed for the MRF1507 device mounted as previously described. A picture of the MRF1507 device is shown in Figure 3. The model was developed using 3D Ansys FEA (Finite Element Analysis) software. It was quickly apparent that, due to the differences in z-axis CTE between the PCB, the package, the copper heatsink, and the leadframe, differential deformation of materials during thermal excursions will cause high stress on the device. This may result in separation of the plastic from the copper leadframe or could also result in solder fatigue failures of the device to board attachment.

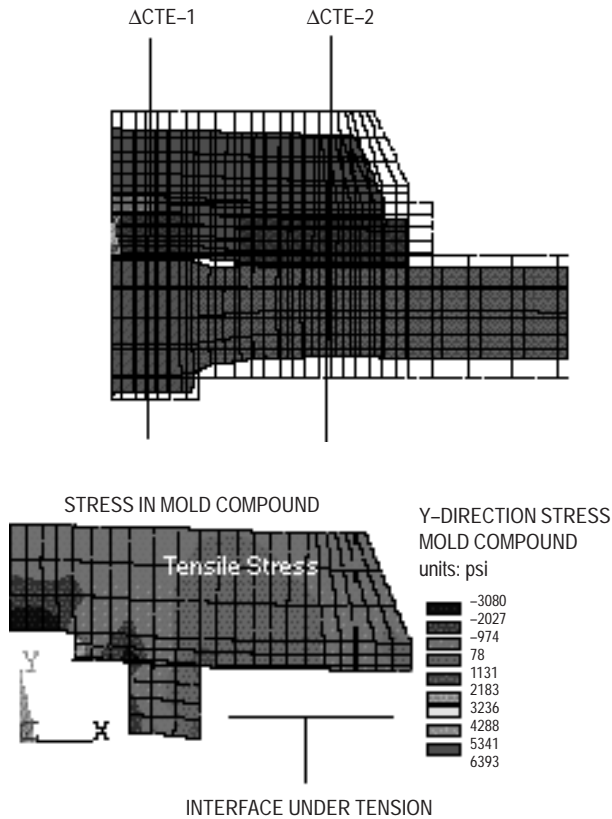


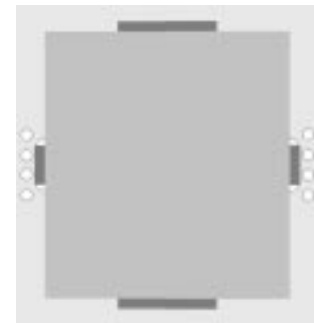
Figure 4. Deformation and Stress Occurring Following Solder Reflow Cycle

In this configuration, the MRF1507, the PCB, and heat sink are coupled together as a constrained assembly. The compliance of this assembly when placed under thermo mechanical load is very limited as was found in the two dimensional FEA results shown in Figure 4. Figure 4 provides the displacements overlayed with the undisplaced structure after cooling from reflow conditions (200°C) to room temperature. Once the solder solidifies below the liquidus temperature, the entire structure is constrained and thermal mechanical stress is induced in the structure as a result of the differing aggregate or effective CTE about the package.

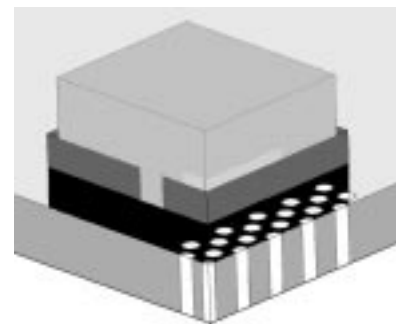
The PCB material shrinkage in the z-direction is much higher than shrinkage of the other materials. From the perspective at a vertical line drawn through the source lead, the CTE difference (i.e. $\Delta\text{CTE}-1$) is small since the materials making up the source terminal, epoxy overmold, and heat sink have approximately the same CTE. This is in contrast to the CTE mismatch for $\Delta\text{CTE}-2$ where the mismatch between the package and PCB is considerable. Such differences induce bending in the structure which, in turn, creates a tensile load between the epoxy overmold and gate (or drain) terminal, which tends to pry open this interface. Another potential failure mode for this mounting scheme would eventually be fatigue failure of the solder joints where the device terminals are attached to the PCB. The solder fatigue failure mode has been seen with other types of surface mount devices, such as the MRF5007 ceramic device, placed under the same set of stress conditions.

Via Board Mounting: The Motorola Recommended Approach

Several alternative mounting approaches were evaluated to reduce thermo-mechanical stress while also providing the necessary thermal management for optimum power conditions. Via board mounting is the proposed solution for meeting the thermal, mechanical, and electrical requirements while also providing the best cost alternative for high volume production. A variety of via configurations have been studied and for purposes of illustration the via layout in this study is shown in Figures 5 and 6. Figure 5 provides a close-up of the MRF1507 mounted on the PCB via perforated board. As shown, the vias go directly through the PCB and are 12 mils in diameter arranged in a staggered pitch of 15 x 30 mils (see Figure 6). Each via hole is copper plated and filled with solder. This particular via layout is fairly dense but it was confirmed that it is manufacturable and cost effective since it eliminates the heat sink piece part and added assembly costs and processes. Other via layout configurations of higher pitch (fewer holes) were also found to meet the performance targets for the MRF1507. However, thermal and mechanical testing is recommended for the user specific pattern adopted if different from here.



Top View



1/4 Expanded Solid Model View

Figure 5. MRF1507 Mounted on PCB With Vias

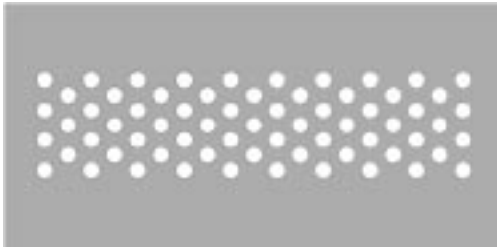


Figure 6. Closeup of the Solder Filled Via Layout, 12 mil Diameter Centers, 15 x 30 mil Pitch

The thermal mechanical aspects of the via board mounting was investigated to determine the thermal stress imparted due to reflow assembly of the package with the PCB. Since the via configuration is a composite of the PCB, solder, and copper, the effective $\Delta CTE-1$ is significantly closer to that of $\Delta CTE-2$. Consequently, the thermal stress induced bending should be reduced considerably. It should be noted that as the via pattern density decreases, less thermal stress will be imparted to the leadless structure.

Figure 7 provides the package out-of-plane displacements corresponding to the via mounting of the PLD1507 shown in Figures 5 and 6. Package bending is seen with the non-uniformity of the displacements along any plane in the z-direction of the package. Had no bending been present, the displacements along the z-axis at any X-Y plane would be uniform. But the bending is considerably reduced from the results shown in Figure 4 as indicated by the order of magnitude reduction in force between the lead and the mold compound. The reduction in bending was found to eliminate delamination issues between the mold compound and the gate (or drain) lead. It also significantly increased the solder life.

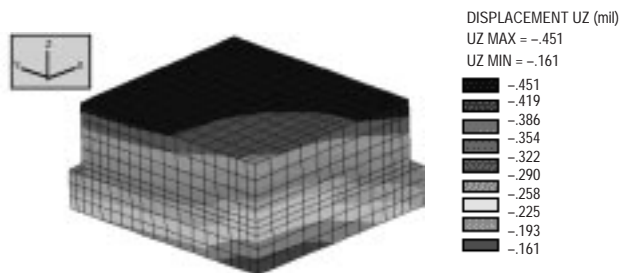


Figure 7. Out-of-Plane Displacements of the Leadless MRF1507 Using Via Mounting

THERMAL MANAGEMENT

Once all aspects of thermo-mechanical stress have been analyzed, the investigation was completed by examining thermal performance of the device under the particular mounting conditions. In the case of the MRF1507, this was done through both modeling and actual thermal measurements taken with thermocouples and IR scans.

The MRF1507 was mounted on the thermal via PCB and screw mounted to a large aluminum heatsink with a thermal grease interface between the board and the heatsink. A power dissipation of 12.3 watts DC was applied to the device, and the heatsink was maintained at 26.1°C. Once the device reached a steady state condition, measurements were taken with an IR scan system. The die junction temperature cannot be

measured directly; however, the maximum temperature at the top of the mold compound was noted to be at 65°C. From that, an estimate of junction temperature was made based upon the die to mold compound thermal resistance obtained from the finite element models described earlier. Based upon this thermal resistance of 1.0°C/W, from the die junction to the top side of the mold compound, the junction temperature was estimated to be 77.3°C. After obtaining the junction temperature, the thermal resistance for the entire structure was calculated to be:

$$\theta_{JS} = (T_J - T_S) / P_D$$

where T_J is the junction temperature (°C)

T_S is the heatsink temperature (°C)

P_D is the dissipated power (W)

θ_{JS} is the junction to heatsink thermal resistance (°C/W)

then, $\theta_{JS} = (77.3^\circ\text{C} - 26.1^\circ\text{C}) / 12.3 \text{ W}$

$$\theta_{JS} = 4.2^\circ\text{C/W}$$

This empirically derived value of 4.2°C/W correlates very well with the 3.9°C/W predicted by the finite element model as shown in Figure 8.

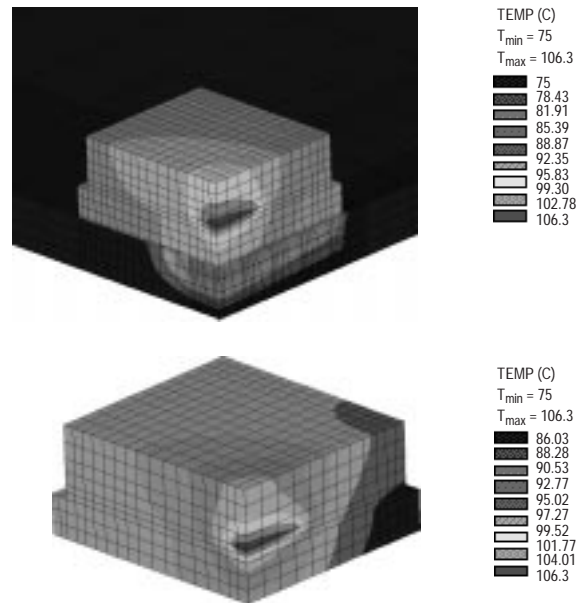


Figure 8. Thermal Modeling Results for MRF1507 Mounted on Via PCB (Power Dissipation = 8 W, 75°C Applied to Bottom of Heat Sink. Die Junction is 106.3°C (Via Layout Shown in Figure 5) $\theta_{JS} = (106.3^\circ\text{C} - 75^\circ\text{C}) / 8 \text{ W} = 3.9^\circ\text{C/W}$

Using engineering margin, the junction to heatsink thermal resistance is specified to be 6.25°C/W. The maximum power dissipation for this device at a heatsink temperature of 25°C was calculated to be:

$$P_D = (T_{Jmax} - T_S) / \theta_{JS}$$

$$P_D = (150^\circ\text{C} - 25^\circ\text{C}) / 6.25^\circ\text{C}$$

$$P_D = 20 \text{ W}$$

Since it is typically impractical to maintain the heatsink temperature at 25°C, a calculation of the maximum heatsink temperature is of importance to the radio designer, especially

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for portable units in which space is extremely limited. The following calculations are based upon 8 watts of RF output power @ 50% efficiency and sufficient gain such that the input power is negligible. The dissipated power is then 8 watts.

$$T_S = T_{Jmax} - P_D * \theta_{JS}$$

$$T_S = 150^{\circ}\text{C} - (8 \text{ W} * 6.25^{\circ}\text{C/W})$$

$$T_S = 100^{\circ}\text{C}$$

Thus, the maximum heatsink temperature with the MRF1507 and a thermal via board of the dimensions and construction described in Figure 5 is 100°C.

MATERIALS AND MANUFACTURABILITY

Board material tested for the MRF1507 mounting schemes was standard printed circuit board — epoxy glass. Also tested was a newer multifunction composition, Nelco N4000-6, typically being used now in the PCB industry, which was 0.040 inches thick. These new compositions show slightly less expansion in the “z” direction. The via pattern described is also standard for the PCB industry, and the vias can be filled with solder during the fabrication cycle of board manufacturing. They could also be filled and reflowed as a separate step prior to component mount and reflow. Some of the solder will exit the vias during the component mount reflow; however, since the vias are relatively small in diameter, the solder mound, or “doming”, which then forms on the backside remains very small. The recommended via solution is producible and manufacturable for both plastic and for ceramic surface mount component attachment schemes.

POWER CYCLING

In order to determine the viability of this heatsinking method over the long term, a set of test conditions were defined for the MRF1507 mounted on the PCBs with thermal management through the vias as described earlier. Thirty-six PCBs were screw mounted to an aluminum plate. The devices were DC biased to insure that the component was operating at 8 watts dissipated power. The PCBs were programmed to operate at a 20% duty cycle. At the same time, the plate, with mounted boards, was placed within a thermal chamber and subjected

to 11 hours of 100°C followed by 11 hours of -40°C temperatures. This accelerates expected lifetime conditions beyond what is typically experienced in field conditions. Changes in the current were monitored to identify potential failure conditions after which individual boards were then tested to eliminate and analyze the failed unit. After 12,000 power cycles, or 1000 full hours of operation, none of the via'd boards experienced any failures. Additionally, via'd boards with their surface mounted components were subjected to temperature cycling of -65°C to +150°C; no failures were experienced after 1000 temperature cycles and no solder fatigue issues or failures were noted.


CONCLUSIONS

A low-stress technique for reliable mounting of surface mount components for power applications has been identified. The recommended solution utilizes filled thermal vias for heat transfer away from the device to the system heatsink. Using the MRF1507, 8 watt RF output power device, as an example, all the necessary steps toward definition of the system mounting method have been defined and described. These steps include thermo-mechanical modeling and design, thermal modeling and empirical testing, and, finally, long term reliability evaluations. For this device, tensile load after solder mounting has been reduced to an insignificant level. Thermal tests have shown that there is adequate margin for the recommended 8 watt RF output power performance level of this device. And, finally, temperature cycling as well as cycling under power conditions have demonstrated that the recommended mounting method is reliable for long-term applications.

For more details on the MRF1507 package please reference the Motorola RF Device Data Book, DL110/D. Additionally you can access RF information directly on the Internet by using the following URL: <http://motorola.com/sps/ff/>.

REFERENCES

Runton, David W., C.M. Swanson. “Design Heat Sinks to Ensure Power-Device Reliability.” *MICROWAVES & RF*. July 1996.

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