

# Motorola Semiconductor Engineering Bulletin

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## EB257

## Detecting Loss of Clock on Modular Microcontrollers

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### General Information

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On modular microcontrollers, when the MODCLK pin is held low at the release of RESET and an external clock signal is applied to the EXTAL pin, the clock synthesizer is bypassed. Also, the bits in the synthesizer control register (SYNCR) have no effect on the operation of the clock.


Thus, a loss of clock cannot be detected when an external oscillator is used. This means that the external oscillator can be stopped and later restarted.

When MODCLK is held high at the release of RESET and the voltage-controlled oscillator (VCO) generates the system clock signal, the clock logic can detect a reference failure, or loss of clock.

In this case, the limp status bit (SLIMP) in the SYNCR is set when a reference failure is detected. The state of the reset enable (RSTEN) bit in the SYNCR determines clock synthesizer operation.

If RSTEN is cleared, then the clock synthesizer will operate in a special mode called limp mode. Limp mode frequency may vary, depending on the device. Maximum limp mode frequency will not exceed half of the maximum system clock when the frequency control bit X in the SYNCR is 0 or maximum system clock frequency when X = 1. If RSTEN is set, then a loss of clock will cause a reset.



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