Order this document
by EB258/D

Motorola Semiconductor Engineering Bulletin

EB258

Sources of Reset on Modular Microcontrollers

By Sharon Darley
Austin, Texas

Introduction

Motorola modular microcontrollers have several sources of reset which are listed here. Resets can be both synchronous and asynchronous. Synchronous reset signals are asserted at the end of the current bus cycle, while asynchronous reset signals cause an immediate reset of the system.

To see which type of reset last occurred, read the reset status register to see which bit has been set.

General Information

External Reset

An external reset affects the clock module and all internal circuits. An external reset is a synchronous reset caused by a logic 0 signal applied to the RESET pin. After the RESET is driven low, the CPU reset control logic asserts RESET internally until the release of RESET. Then, the reset control logic drives RESET low for an additional 512 clock cycles. Because a conflict will occur if the RESET line is held low at the same time that the CPU32 executes a RESET instruction, the RESET line

must be held for at least 520 cycles to guarantee that the external reset is recognized by the external bus interface.

Power-On Reset

Power-on reset is an asynchronous reset generated by the external bus interface. A modular microcontroller goes into reset when V_{DD} drops below approximately 2.5 volts, and it stays in reset until V_{DD} rises above this threshold. The duration for which V_{DD} must remain below the threshold to trigger power-on reset has not been measured, but it is typically on the order of nanoseconds. The power-on reset should not be relied upon to monitor V_{DD} voltage since parts of the device logic can fail at a higher V_{DD} than the power-on reset threshold. To monitor V_{DD}, use an external low voltage inhibit circuit such as the MC34064.

Software Reset

The software reset is an asynchronous reset caused by a timeout of the software watchdog timer. Although software reset is enabled at power-on, it can be disabled by setting the software watchdog enable bit (SWE[7]) in the system protection control register (SYPCR).

When the software reset is enabled, the bit pattern $55 followed by $AA must be written into the software service register (SWSR) within a specified amount of time to prevent a software reset. This feature is typically used to stop a runaway program that has branched to the wrong location.

Double Bus Fault Reset

A double bus fault reset is an asynchronous reset caused by the double bus fault monitor (also called the halt monitor). A double bus fault is a special case of a bus error which can abort exception processing.

After two bus error signals (BERR) are asserted, the MCU halts, drives the HALT line low, and then can be restarted only by a reset. When the HALT line is driven low internally, the double bus fault monitor will immediately cause a reset if it is enabled.

If the double bus fault monitor has been disabled by writing a 0 to the halt monitor enable (HME) bit in SYPCR, then nothing happens and the MCU remains in the halted state indefinitely and must be reset externally.

Loss of Clock Reset

A loss of clock reset is a synchronous reset that occurs when the frequency reference to the clock submodule is lost. For this reset to be enabled, the RSTEN bit in the synthesizer control register (SYNCR) must be set and the voltage-controlled oscillator (VCO) must be enabled.

System Reset

A system reset drives the RESET pin low, but does not reset the CPU or system integration module (SIM). A system reset is an asynchronous reset caused when the CPU32 executes a RESET instruction.

This is the only reset that does not allow the CPU to regain the ability to write once to write-once-only bits, such as the software watchdog enable bits.

The CPU16 does not have a RESET instruction.

Test Reset

A test reset drives the external RESET pin low and resets all internal circuits other than the clock module. A test reset is a synchronous reset caused by the SIM test submodule when the MCU exits from special test mode.

The test submodule is used for factory production testing of the MCU and is not recommended for user applications.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution, P.O. Box 5405, Denver, Colorado 80217, 1-800-441-2447 or 1-303-675-2140. Customer Focus Center, 1-800-521-6274

JAPAN: Motorola Japan Ltd.: SPD, Strategic Planning Office, 141, 4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan, 03-5487-8488

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd., Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, New Territories, Hong Kong, 852-26629298

Mfax™, Motorola Fax Back System: RMFAX0@email.sps.mot.com; http://sps.motorola.com/mfax/; TOUCHTONE, 1-602-244-6609; US and Canada ONLY, 1-800-774-1848

HOME PAGE: http://motorola.com/sps/

MOTOROLA